A5975D

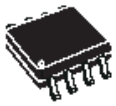
Up to 3 A step-down switching regulator for automotive applications

Features

- Qualified following the AEC-Q100 requirements (see PPAP for more details)
- 3 A DC output current
- Operating input voltage from 4 V to 36 V
- 3.3 V / (±2%) reference voltage
- Output voltage adjustable from 1.235 V to 35 V
- Low dropout operation: 100% duty cycle
- 250 kHz internally fixed frequency
- Voltage feed-forward
- Zero load current operation
- Internal current limiting
- Inhibit for zero current consumption
- Synchronization
- Protection against feedback disconnection
- Thermal shutdown

Application

- Dedicated to automotive applications

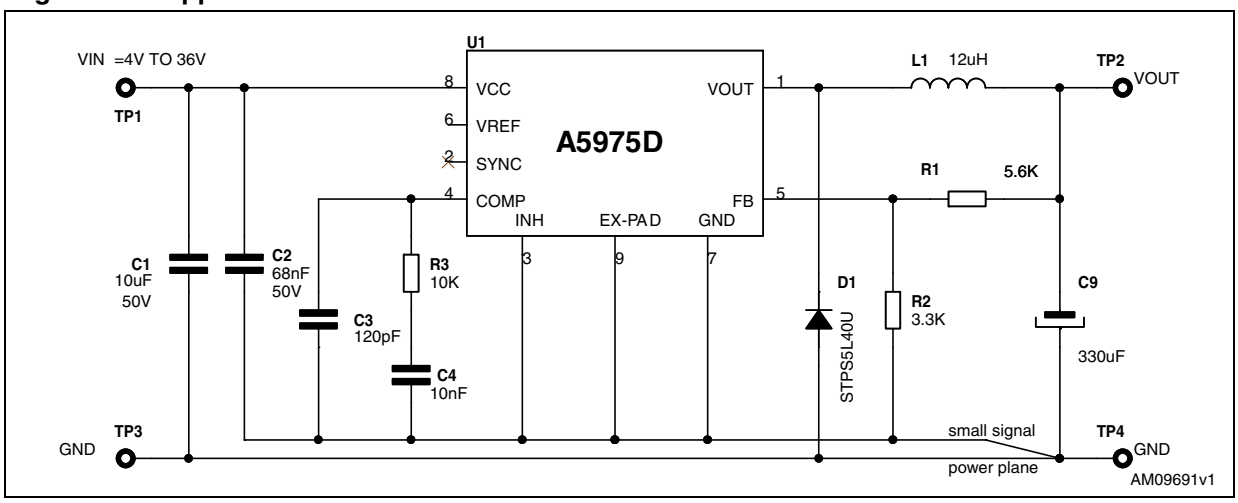


HSOP8 - exposed pad

Description

The A5975D is a step-down monolithic power switching regulator with a minimum switch current limit of 3.75 A, it is therefore able to deliver up to 3 A DC current to the load depending on the application conditions. The output voltage can be set from 1.235 V to 35 V. The high current level is also achieved thanks to a HSOP8 package with exposed frame, that allows to reduce the R_{THJ-A} down to approximately 40 °C/W. The device uses an internal P-channel DMOS transistor (with a typical $R_{DS(on)}$ of 250 mΩ) as switching element to minimize the size of the external components. An internal oscillator fixes the switching frequency at 250 kHz. Having a minimum input voltage of only 4 V, it fits automotive applications requiring device operation even in cold crank conditions. Pulse-by-pulse current limit with the internal frequency modulation offers an effective constant current short-circuit protection.

Figure 1. Application schematic



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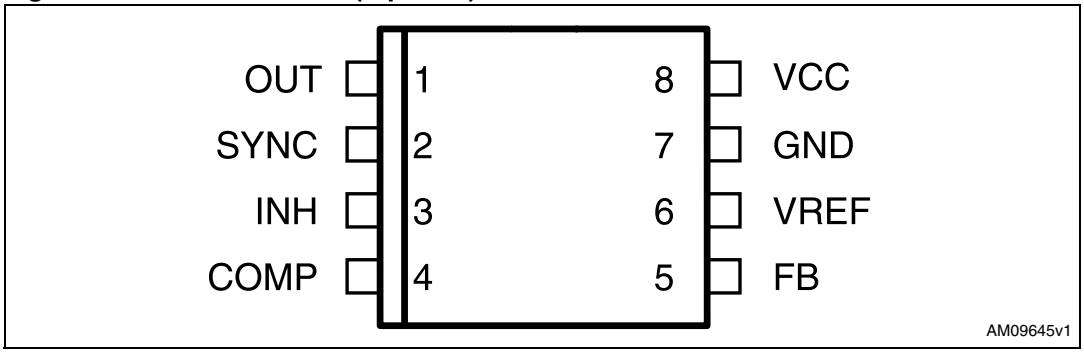
1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

N	Pin	Description
1	OUT	Regulator output.
2	SYNCH	Master/slave synchronization.
3	INH	A logical signal (active high) disables the device. If INH is not used, the pin must be grounded. When it is open an internal pull-up disables the device.
4	COMP	E/A output for frequency compensation.
5	FB	Feedback input. Connecting directly to this pin results in an output voltage of 1.23 V. An external resistive divider is required for higher output voltages.
6	V_{REF}	3.3 V V_{REF}. No cap is requested for stability.
7	GND	Ground.
8	V_{CC}	Unregulated DC input voltage.

2 Electrical data

2.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_8	Input voltage	40	V
V_1	OUT pin DC voltage OUT pin peak voltage at Δt = 0.1 µs	-1 to 40 -5 to 40	V V
I_1	Maximum output current	Int. limit.	
V_4, V_5	Analog pins	4	V
V_3	INH	-0.3 to V_{CC}	V
V_2	SYNCH	-0.3 to 4	V
P_{TOT}	Power dissipation at $T_A \leq 60$ °C	2.25	W
T_J	Operating junction temperature range	-40 to 150	°C
T_{STG}	Storage temperature range	-55 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{THJ-A}	Maximum thermal resistance junction-ambient	40 (1)	°C/W

1. Package mounted on demonstration board.

3 Electrical characteristics

T_J = -40 °C to 125 °C, V_{CC} = 12 V, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CC}	Operating input voltage range	V_0 = 1.235 V; I_0 = 2 A	4		36	V
$R_{DS(on)}$	MOSFET on-resistance			0.250	0.5	Ω
I_L	Maximum limiting current	V_{CC} = 5 V	3.75	4.5	5.25	A
f_{SW}	Switching frequency		212	250	280	kHz
	Duty cycle		0		100	%
Dynamic characteristics (see test circuit)						
V_5	Voltage feedback	4.4 V < V_{CC} < 36 V, 20 mA < I_0 < 2 A	1.198	1.235	1.272	V
DC characteristics						
I_{qop}	Total operating quiescent current			3	5	mA
I_q	Quiescent current	Duty cycle = 0; V_{FB} = 1.5 V			2.5	mA
$I_{qst\text{-}by}$	Total standby quiescent current	V_{INH} > 2.2 V		50	100	µA
		V_{CC} = 36 V; V_{INH} > 2.2 V		50	100	µA
Inhibit						
	INH threshold voltage	Device ON			0.8	V
		Device OFF	2.2			V
Error amplifier						
V_{OH}	High level output voltage	V_{FB} = 1 V	3.5			V
V_{OL}	Low level output voltage	V_{FB} = 1.5 V			0.4	V
$I_{o\ source}$	Source output current	V_{COMP} = 1.9 V; V_{FB} = 1 V	190	300		µA
$I_{o\ sink}$	Sink output current	V_{COMP} = 1.9 V; V_{FB} = 1.5 V	1	1.5		mA
I_b	Source bias current			2.5	4	µA
	DC open loop gain	R_L = ∞	50	65		dB
gm	Transconductance	I_{COMP} = -0.1 mA to 0.1 mA; V_{COMP} = 1.9 V		2.3		mS
Synch function						

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
	High input voltage	V_{CC} = 4.4 to 36 V	2.5		V_{REF}	V
	Low input voltage	V_{CC} = 4.4 to 36 V			0.74	V
	Slave synch current(1)	V_{synch} = 0.74 V V_{synch} = 2.33 V	0.11 0.21		0.25 0.45	mA
	Master output amplitude	I_{source} = 3 mA	2.75	3		V
	Output pulse width	No load, V_{synch} = 1.65 V	0.20	0.35		µs
Reference section						
	Reference voltage	I_{REF} = 0 to 5 mA V_{CC} = 4.4 V to 36 V	3.2	3.3	3.399	V
	Line regulation	I_{REF} = 0 mA V_{CC} = 4.4 V to 36 V		5	10	mV
	Load regulation	I_{REF} = 0 mA		8	15	mV
	Short-circuit current		5	18	35	mA

1. Guaranteed by design.

4 Datasheet parameters over the temperature range

100% of the population in the production flow is tested at three different ambient temperatures (-40 °C, +25 °C, and +125 °C) to guarantee the datasheet parameters inside the junction temperature range (-40 °C, +125 °C).

The device operation is guaranteed when the junction temperature is inside the (-40 °C; +150 °C) temperature range. The user can estimate the silicon temperature increase with respect to the ambient temperature evaluating the internal power losses generated during device operation (please refer to *Section 2.2*).

However, the embedded thermal protection disables the switching activity to protect the device in case the junction temperature reaches the T_{SHTDWN} (+150 °C ±10 °C) temperature.

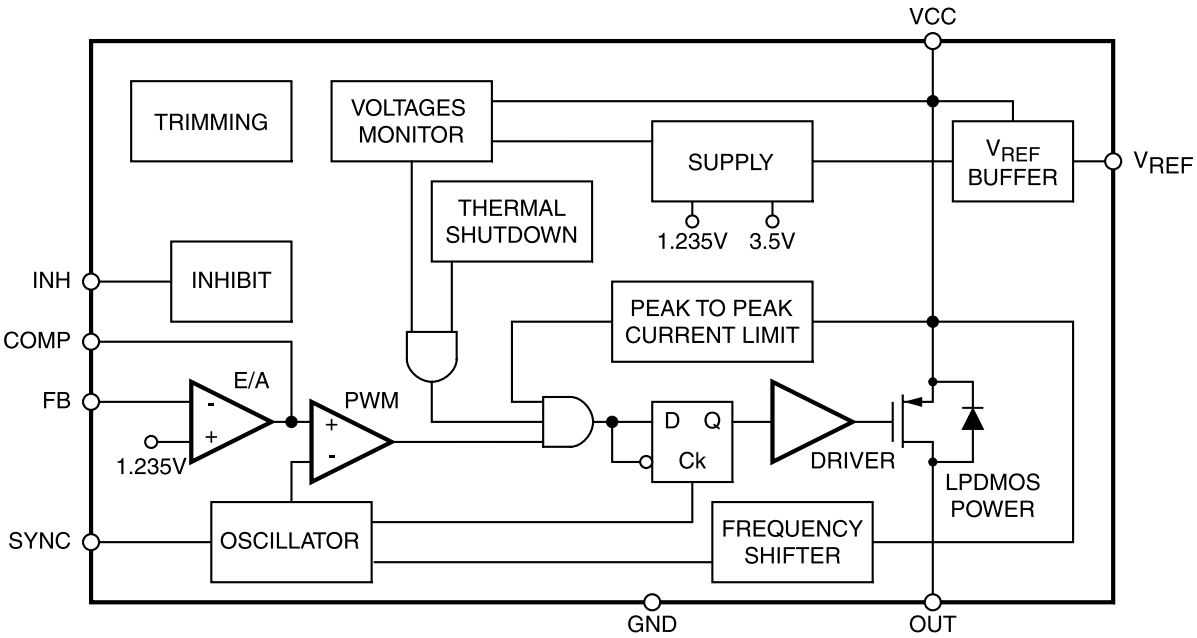
All the datasheet parameters can be guaranteed to a maximum junction temperature of +125 °C, to avoid triggering the thermal shutdown protection during the testing phase due to self heating.

5 Functional description

The main internal blocks are shown in the device block diagram in *Figure 3*. They are:

- A voltage regulator supplying the internal circuitry. From this regulator, a 3.3 V reference voltage is externally available
- A voltage monitor circuit which checks the input and the internal voltages
- A fully integrated sawtooth oscillator with a frequency of 250 kHz ± 15%, including also the voltage feed-forward function and an input/output synchronization pin
- Two embedded current limitation circuits which control the current that flows through the power switch. The pulse-by-pulse current limit forces the power switch OFF cycle-by-cycle, if the current reaches an internal threshold, while the frequency shifter reduces the switching frequency in order to significantly reduce the duty cycle
- A transconductance error amplifier
- A pulse width modulator (PWM) comparator and the relative logic circuitry necessary to drive the internal power
- A high side driver for the internal P-MOS switch
- An inhibit block for standby operation
- A circuit to implement the thermal protection function

Figure 3. Block diagram



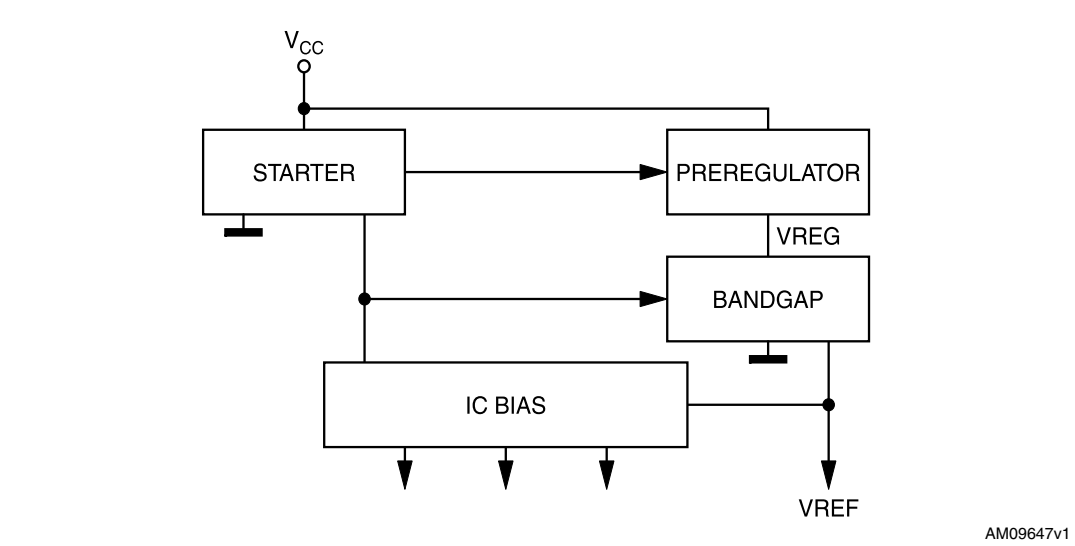
5.1 Power supply and voltage reference

The internal regulator circuit (shown in *Figure 4*) consists of a start-up circuit, an internal voltage pre-regulator, the bandgap voltage reference and the bias block that provides current to all the blocks. The starter supplies the start-up currents to the entire device when the input voltage goes high and the device is enabled (inhibit pin connected to ground). The pre-regulator block supplies the bandgap cell with a pre-regulated voltage, V_{REG}, that has a very low supply voltage noise sensitivity.

5.2 Voltage monitor

An internal block continuously senses the V_{CC}, V_{REF} and V_{BG}. If the voltages go higher than their thresholds, the regulator begins operating. There is also a hysteresis on the V_{CC} (UVLO).

Figure 4. Internal circuit



5.3 Oscillator and synchronization

Figure 5 shows the block diagram of the oscillator circuit.

The clock generator provides the switching frequency of the device, which is internally fixed at 250 kHz. The frequency shifter block acts to reduce the switching frequency in case of strong overcurrent or short-circuit. The clock signal is then used in the internal logic circuitry and is the input of the ramp generator and synchronizer blocks.

The ramp generator circuit provides the sawtooth signal, used for PWM control and the internal voltage feed-forward, while the synchronizer circuit generates the synchronization signal. The device also has a synchronization pin which can work as both master and slave.

Beating frequency noise is an issue when more than one voltage rail is on the same board. A simple way to avoid this issue is to operate all the regulators at the same switching frequency.

The synchronization feature, of a set of the A5975D, is simply obtained by connecting together their SYNCH pins. The device with highest switching frequency is the master,

which provides the synchronization signal to the others. Therefore the SYNCH is an I/O pin to deliver or recognize a frequency signal. The synchronization circuitry is powered by the internal reference (V_{REF}), so a small filtering capacitor (≥ 100 nF) connected between the V_{REF} pin and the signal ground of the master device is recommended for its proper operation. However, when a set of synchronized devices populate a board it is not possible to know in advance which is working as master, so the filtering capacitor must be designed for a whole set of devices.

When one or more devices are synchronized to an external signal, its amplitude must be in compliance with specifications given in *Table 4*. The frequency of the synchronization signal must be, at a minimum, higher than the maximum guaranteed natural switching frequency of the device (275 kHz, see *Table 4*) while the duty cycle of the synchronization signal can vary from approximately 10% to 90%. The small capacitor under the V_{REF} pin is required for this operation.

Figure 5. Oscillator circuit block diagram

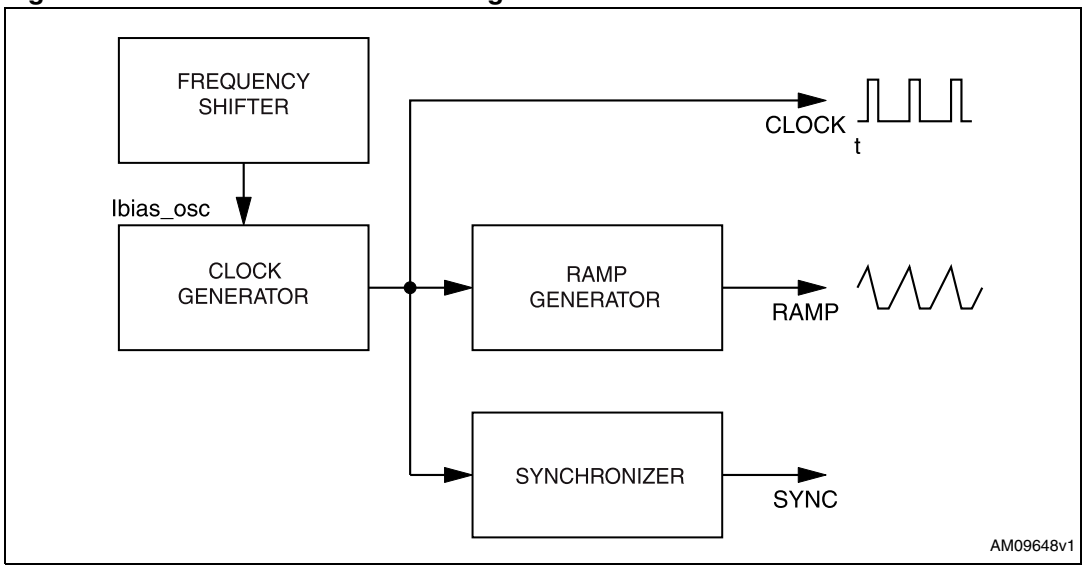
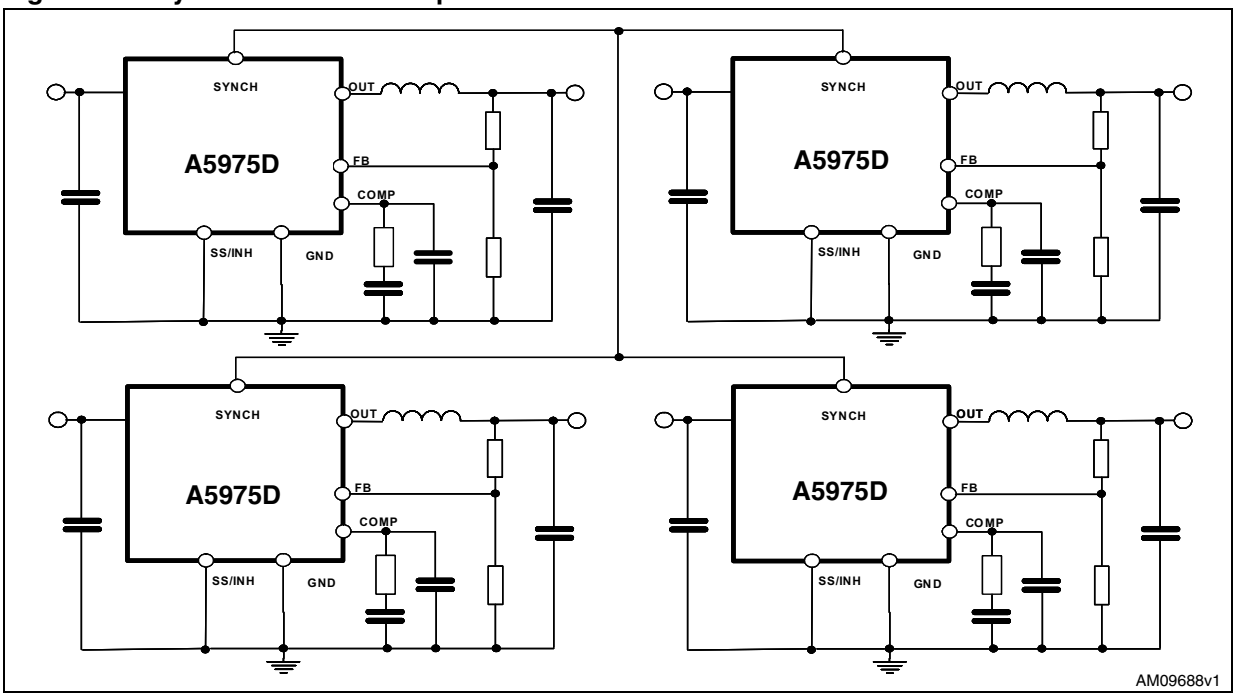


Figure 6. Synchronization example

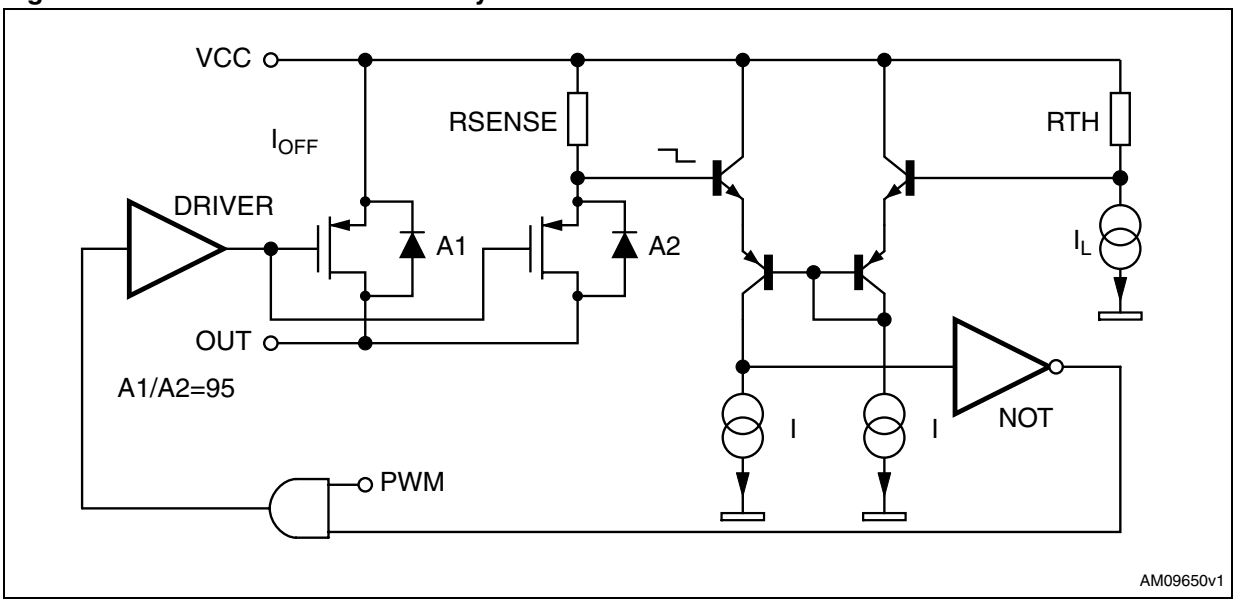


5.4 Current protection

The A5975D features two types of current limit protection; pulse-by-pulse and frequency foldback.

The schematic of the current limitation circuitry for the pulse-by-pulse protection is shown in *Figure 7*. The output power PDMOS transistor is split into two parallel PDMOS transistors. The smallest one includes a resistor in series, R_{SENSE}. The current is sensed through R_{SENSE} and, if it reaches the threshold, the mirror becomes unbalanced and the PDMOS is switched off until the next falling edge of the internal clock pulse. Due to this reduction of the ON time, the output voltage decreases. As the minimum switch-on time necessary to sense the current, in order to avoid a false overcurrent signal, is too short to obtain a sufficiently low duty cycle at 250 kHz (see *Section 8.5*), the output current in strong overcurrent or short-circuit conditions may not be properly limited. For this reason, the switching frequency is also reduced, therefore keeping the inductor current under its maximum threshold. The frequency shifter (*Figure 5*) functions based on the feedback voltage. As the feedback voltage decreases (due to the reduced duty cycle), the switching frequency decreases also.

Figure 7. Current limitation circuitry



5.5 Error amplifier

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (1.235 V), while the inverting input (FB) is connected to the external divider or directly to the output voltage. The output (COMP) is connected to the external compensation network. The uncompensated error amplifier has the following characteristics:

Table 5. Uncompensated error amplifier characteristics

Description	Values
Transconductance	2300 µS
Low frequency gain	65 dB
Minimum sink/source voltage	1500 µA/300 µA
Output voltage swing	0.4 V/3.65 V
Input bias current	2.5 µA

The error amplifier output is compared to the oscillator sawtooth to perform PWM control.

5.6 PWM comparator and power stage

This block compares the oscillator sawtooth and the error amplifier output signals to generate the PWM signal for the driving stage.

The power stage is a highly critical block, as it functions to guarantee a correct turn-on and turn-off of the PDMOS. The turn-on of the power element, or more accurately, the rise time of the current at turn-on, is a very critical parameter. At the first approach, it appears that the faster the rise time, the lower the turn-on losses.

However, there is a limit introduced by the recovery time of the recirculation diode.

In fact, when the current of the power element is equal to the inductor current, the diode turns off and the drain of the power is able to go high. But, during its recovery time, the diode can be considered a high value capacitor and this produces a very high peak current, responsible for numerous problems:

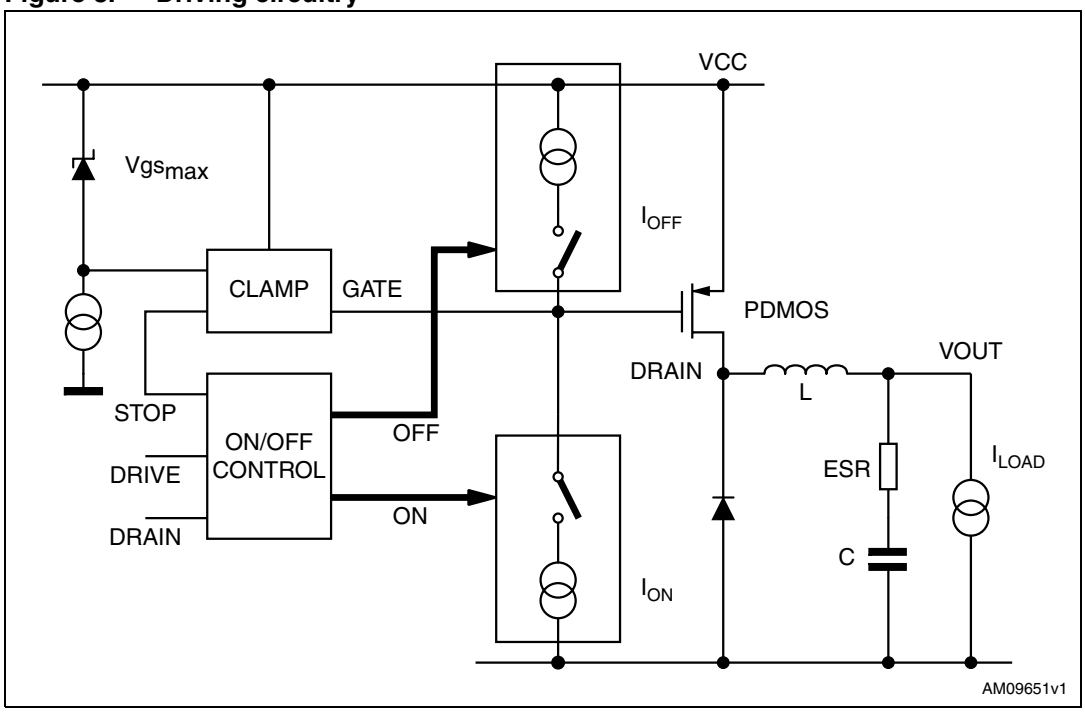
- Spikes on the device supply voltage that cause oscillations (and therefore noise) due to the board parasites
- Turn-on overcurrent leads to a decrease in the efficiency and system reliability
- Major EMI problems
- Shorter free-wheeling diode life

The fall time of the current during turn-off is also critical, as it produces voltage spikes (due to the parasitic elements of the board) that increase the voltage drop across the PDMOS.

In order to minimize these problems, a new driving circuit topology has been used (the block diagram is shown in *Figure 8*). The basic idea is to change the current levels used to turn the power switch on and off, based on the PDMOS and the gate clamp status.

This circuitry allows the power switch to be turned off and on quickly and addresses the free-wheeling diode recovery time problem. The gate clamp is necessary to ensure that V_{GS} of the internal switch does not go higher than V_{GSmax}. The on/off control block protects against any cross conduction between the supply line and ground.

Figure 8. Driving circuitry



5.7 Inhibit function

The inhibit feature is used to put the device in standby mode. With the INH pin higher than 2.2 V, the device is disabled and the power consumption is reduced to less than 100 µA. With the INH pin lower than 0.8 V, the device is enabled. If the INH pin is left floating, an internal pull-up ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also V_{CC} compatible.

5.8 Thermal shutdown

The shutdown block generates a signal that turns off the power stage if the temperature of the chip goes higher than a fixed internal threshold (150±10 °C). The sensing element of the chip is very close to the PDMOS area, ensuring fast and accurate temperature detection. A hysteresis of approximately 20 °C keeps the device from turning on and off continuously.

6 Additional features and protection

6.1 Feedback disconnection

If the feedback is disconnected, the duty cycle increases towards the maximum allowed value, bringing the output voltage close to the input supply. This condition could destroy the load.

To avoid this hazardous condition, the device is turned off if the feedback pin is left floating.

6.2 Output overvoltage protection

Overvoltage protection, or OVP, is achieved by using an internal comparator connected to the feedback, which turns off the power stage when the OVP threshold is reached. This threshold is typically 30% higher than the feedback voltage.

When a voltage divider is required to adjust the output voltage (*Figure 19*), the OVP intervention is set at:

Equation 1

$$V_{OVP} = 1.3 \cdot \frac{R_1 + R_2}{R_2} \cdot V_{FB}$$

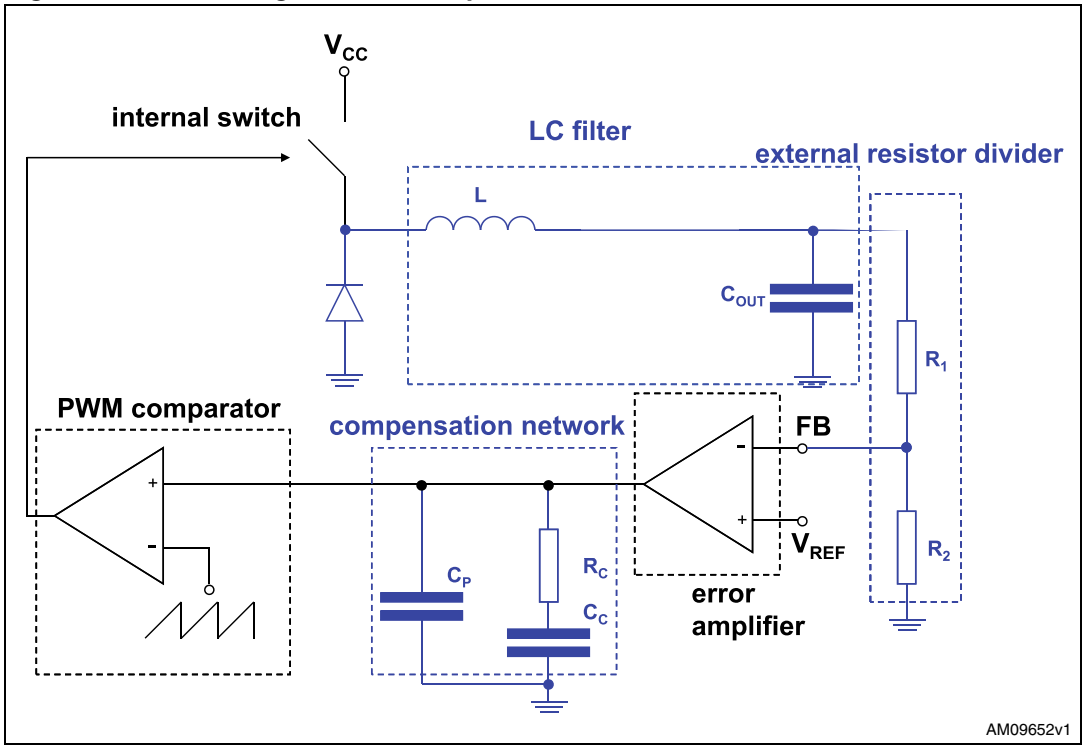
where R_1 is the resistor connected between the output voltage and the feedback pin, and R_2 is between the feedback pin and ground.

6.3 Zero load

Due to the fact that the internal power is a PDMOS, no bootstrap capacitor is required and so the device works properly even with no load at the output. In this case it works in burst mode, with a random burst repetition rate.

7 Closing the loop

Figure 9. Block diagram of the loop



7.1 Error amplifier and compensation network

The output LC filter of a step-down converter contributes with 180-degree phase shift in the control loop. For this reason a compensation network between the COMP pin and GROUND is added. The simplest compensation network, together with the equivalent circuit of the error amplifier, are shown in *Figure 10*. R_C and C_C introduce a pole and a zero in the open loop gain. CP does not significantly affect system stability but it is useful to reduce the noise of the COMP pin.

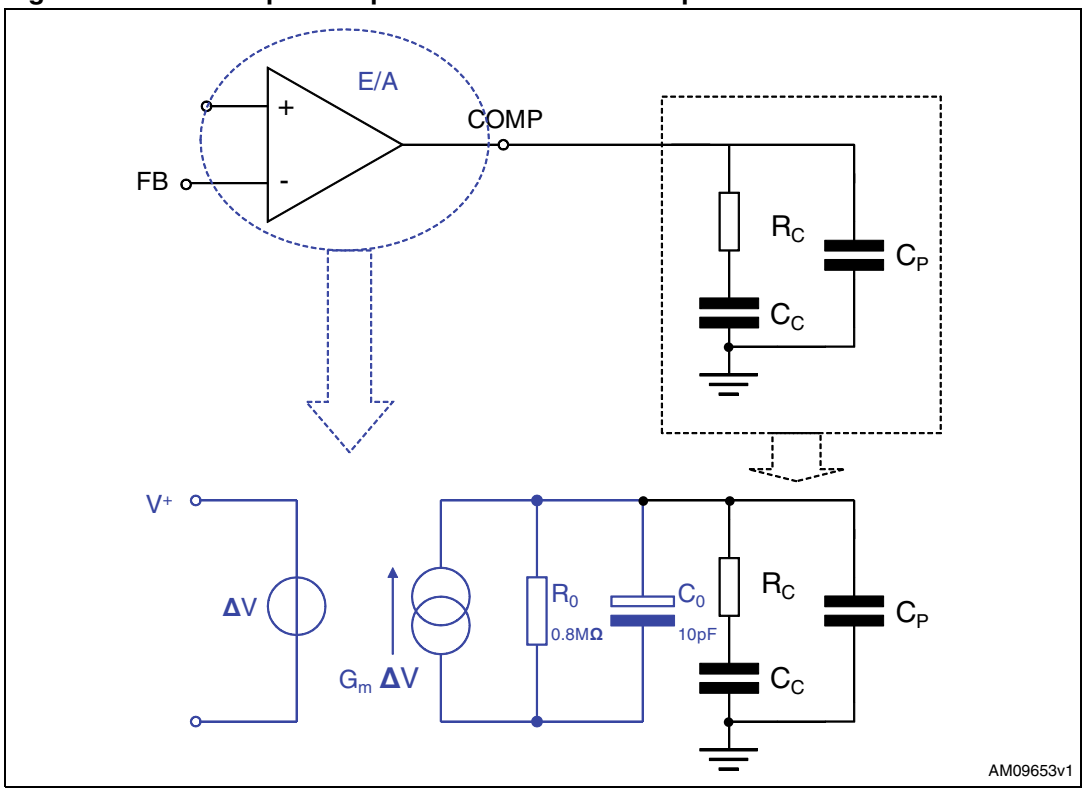
The transfer function of the error amplifier and its compensation network is:

Equation 2

$$A_0(s) = \frac{A_{V0} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_0 \cdot (C_0 + C_p) \cdot R_c \cdot C_c + s \cdot (R_0 \cdot C_c + R_0 \cdot (C_0 + C_p) + R_c \cdot C_c) + 1}$$

where $A_{vo} = G_m \cdot R_o$.

Figure 10. Error amplifier equivalent circuit and compensation network



The poles of this transfer function are (if $C_c >> C_0+C_P$):

Equation 3

$$F_{P1} = \frac{1}{2 \cdot \pi \cdot R_0 \cdot C_c}$$

Equation 4

$$F_{P2} = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_0 + C_p)}$$

whereas the zero is defined as:

Equation 5

$$F_{Z1} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c}$$

F_{P1} is the low frequency which sets the bandwidth, while the zero F_{Z1} is usually put near to the frequency of the double pole of the LC filter (see below). F_{P2} is usually at a very high frequency.

7.2 LC filter

The transfer function of the LC filter is given by:

Equation 6

$$A_{LC}(s) = \frac{R_{LOAD} \cdot (1 + ESR \cdot C_{OUT} \cdot s)}{s^2 \cdot L \cdot C_{OUT} \cdot (ESR + R_{LOAD}) + s \cdot (ESR \cdot C_{OUT} \cdot R_{LOAD} + L) + R_{LOAD}}$$

where R_{LOAD} is defined as the ratio between V_{OUT} and I_{OUT}.

If R_{LOAD}>>ESR, the previous expression of A_{LC} can be simplified and becomes:

Equation 7

$$A_{LC}(s) = \frac{1 + ESR \cdot C_{OUT} \cdot s}{L \cdot C_{OUT} \cdot s^2 + ESR \cdot C_{OUT} \cdot s + 1}$$

The zero of this transfer function is given by:

Equation 8

$$F_O = \frac{1}{2 \cdot \pi \cdot ESR \cdot C_{OUT}}$$

F_0 is the zero introduced by the ESR of the output capacitor and it is very important to increase the phase margin of the loop.

The poles of the transfer function can be calculated through the following expression:

Equation 9

$$F_{PLC1,2} = \frac{-ESR \cdot C_{OUT} \pm \sqrt{(ESR \cdot C_{OUT})^2 - (4 \cdot L \cdot C_{OUT})}}{2 \cdot L \cdot C_{OUT}}$$

In the denominator of A_{LC} the typical second order system equation can be recognized:

Equation 10

$$s^2 + 2 \cdot \delta \cdot \omega_n \cdot s + \omega^2_n$$

If the damping coefficient δ is very close to zero, the roots of the equation become a double root whose value is ω_n.

Similarly for A_{LC}, the poles can usually be defined as a double pole whose value is:

Equation 11

$$F_{PLC} = \frac{1}{2 \cdot \pi \bullet \sqrt{L \cdot C_{OUT}}}$$

7.3 PWM comparator

The PWM gain is given by the following formula:

Equation 12

$$G_{PWM}(s) = \frac{V_{cc}}{(V_{OSCMAX} - V_{OSCMIN})}$$

where V_{OSCMAX} is the maximum value of a sawtooth waveform and V_{OSCMIN} is the minimum value. A voltage feed-forward is implemented to ensure a constant GPWM. This is obtained by generating a sawtooth waveform directly proportional to the input voltage V_{CC}.

Equation 13

$$V_{OSCMAX} - V_{OSCMIN} = K \cdot V_{CC}$$

where K is equal to 0.076. Therefore the PWM gain is also equal to:

Equation 14

$$G_{PWM}(s) = \frac{1}{K} = const$$

This means that even if the input voltage changes, the error amplifier does not change its value to keep the loop in regulation, therefore ensuring a better line regulation and line transient response.

In summary, the open loop gain can be expressed as:

Equation 15

$$G(s) = G_{PWM}(s) \cdot \frac{R_2}{R_1 + R_2} \cdot A_O(s) \cdot A_{LC}(s)$$

Example:

Considering R_C = 10 kΩ, C_C = 10 nF and C_P = 120 pF, the poles and zeroes of A_0 are:

F_{P1} = 20 Hz

F_{P2} = 130 kHz

F_{Z1} = 1.6 kHz

If L = 12 µH, C_{OUT} = 220 µF and ESR = 25 mΩ, the poles and zeroes of A_{LC} become:

F_{PLC} = 2.5 kHz

F_0 = 38 kHz

Finally, R_1 = 5.6 kΩ and R_2 = 3.3 kΩ.

The gain and phase bode diagrams are plotted respectively in *Figure 11* and *12*.

Figure 11. Module plot

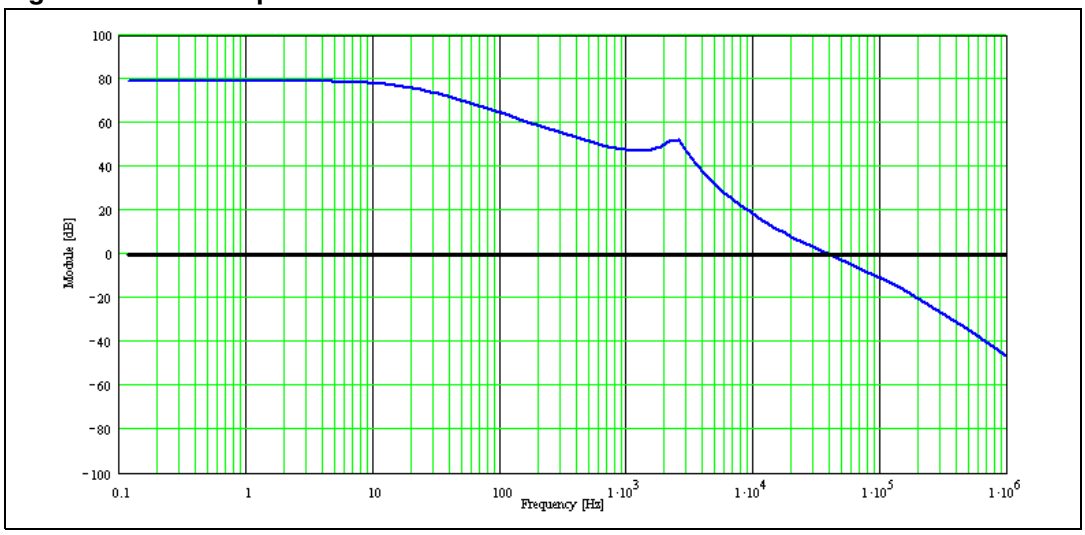
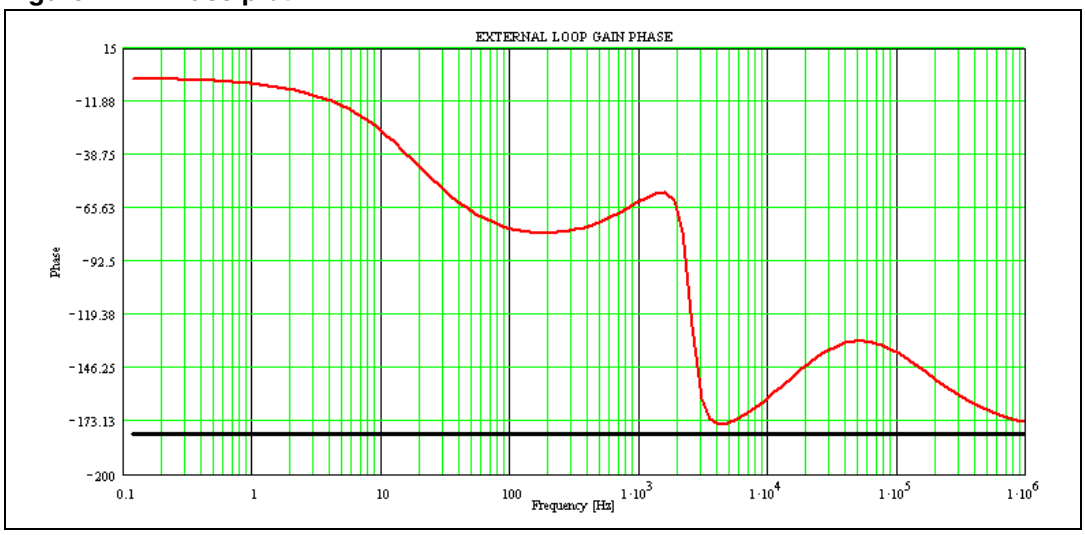


Figure 12. Phase plot



The cut-off frequency and the phase margin are:

Equation 16

$$F_C = 38kHz \quad \text{Phase margin} = 45°$$

8 Application information

8.1 Component selection

- Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

As step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb all this switching current, which can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors must be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency. The critical parameter is usually the RMS current rating, which must be higher than the RMS input current. The maximum RMS input current (flowing through the input capacitor) is:

Equation 17

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

where η is the expected system efficiency, D is the duty cycle and I_O is the output DC current. This function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to I_O divided by 2 (considering η = 1). The maximum and minimum duty cycles are:

Equation 18

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}}$$

and

Equation 19

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

where V_F is the free-wheeling diode forward voltage and V_{SW} the voltage drop across the internal PDMOS. Considering the range D_{MIN} to D_{MAX}, it is possible to determine the max. IRMS going through the input capacitor. Capacitors that can be considered are:

- Electrolytic capacitors:

These are widely used due to their low price and their availability in a wide range of RMS current ratings.

The only drawback is that, considering ripple current rating requirements, they are physically larger than other capacitors.

- Ceramic capacitors:

If available for the required value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to very low ESR).

The drawback is the considerably high cost.

- Tantalum capacitors:

Very good, small tantalum capacitors with very low ESR are becoming more available. However, they can occasionally burn if subjected to very high current during charge.

Therefore, it is better to avoid this type of capacitor for the input filter of the device. They can, however, be subjected to high surge current when connected to the power supply.

Table 6. List of ceramic capacitors for the A5975D

Manufacturer	Series	Capacitor value (µ)	Rated voltage (V)
TAIYO YUDEN	UMK325BJ106MM-T	10	50
MURATA	GRM42-2 X7R 475K 50	4.7	50

- Output capacitor

The output capacitor is very important to meet the output voltage ripple requirements.

Using a small inductor value is useful to reduce the size of the choke but it increases the current ripple. So, to reduce the output voltage ripple, a low ESR capacitor is required. Nevertheless, the ESR of the output capacitor introduces a zero in the open loop gain, which helps to increase the phase margin of the system. If the zero goes to a very high frequency, its effect is negligible. For this reason, ceramic capacitors and very low ESR capacitors in general should be avoided.

Tantalum and electrolytic capacitors are usually a good choice for this purpose. A list of some tantalum capacitor manufacturers is provided in *Table 7*.

Table 7. Output capacitor selection

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
Sanyo POSCAP(1)	TAE	47 to 680	2.5 to 10	25 to 35
	TV	68 to 330	4 to 6.3	25 to 40
AVX	TPS	100 to 470	4 to 35	50 to 200
KEMET	T494/5	100 to 470	4 to 20	30 to 200
Sprague	595D	220 to 390	4 to 20	160 to 650

1. POSCAP capacitors have some characteristics which are very similar to tantalum.

- Inductor

The inductor value is very important as it fixes the ripple current flowing through the output capacitor. The ripple current is usually fixed at 20 - 40% of I_{Omax}, which is 0.6 - 1.2 A with I_{Omax} = 3 A. The approximate inductor value is obtained using the following formula:

Equation 20

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I} \cdot T_{ON}$$

where T_{ON} is the ON time of the internal switch, given by D · T. For example, with V_{OUT} = 3.3 V, V_{IN} = 12 V and ΔI_O = 0.9 A, the inductor value is about 12 µH. The peak current through the inductor is given by:

Equation 21

$$I_{PK} = I_O + \frac{\Delta I}{2}$$

and it can be seen that if the inductor value decreases, the peak current (which must be lower than the current limit of the device) increases. So, when the peak current is fixed, a higher inductor value allows a higher value for the output current. In *Table 8*, some inductor manufacturers are listed.

Table 8. Inductor selection

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	DO3316T	5.6 to 12	3.5 to 4.7
Coilcraft	MSS1260T	5.6 to 15	3.5 to 8
Wurth Elektronik	WE-PD L	4.7 to 27	3.55 to 6

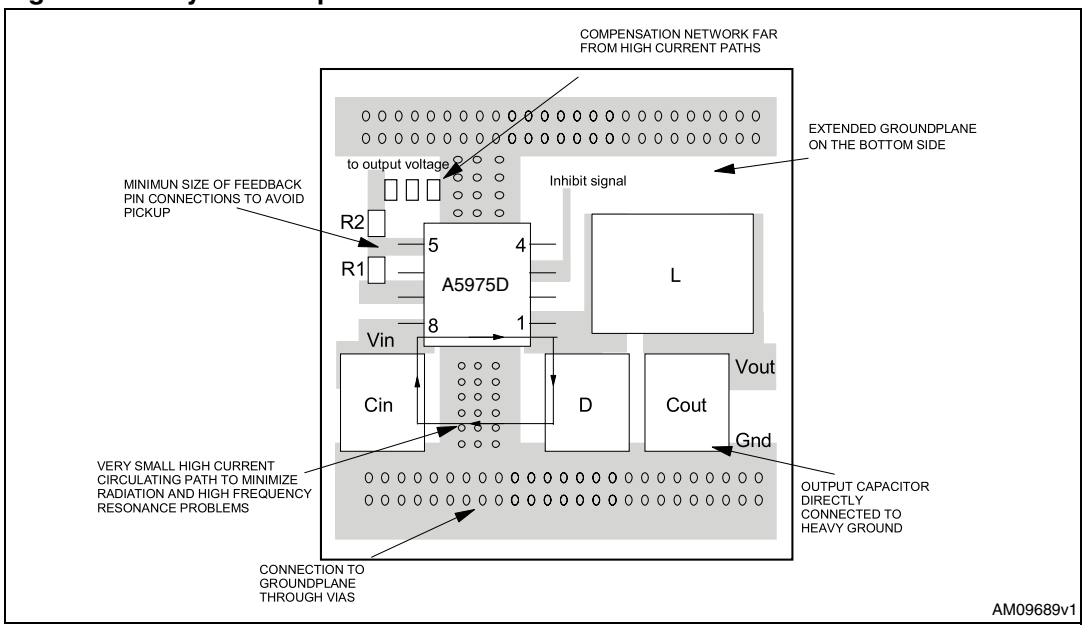
8.2 Layout considerations

The layout of the switching DC-DC converters is very important to minimize noise and interference. Power-generating portions of the layout are the main cause of noise and so high switching current loop areas should be kept as small as possible and lead lengths as short as possible.

High impedance paths (in particular the feedback connections) are susceptible to interference, so they should be as far as possible from the high current paths. A layout example is provided in *Figure 13* below.

The input and output loops are minimized to avoid radiation and high frequency resonance problems. The feedback pin connections to the external divider are very close to the device to avoid pick-up noise. Another important issue is the ground plane of the board. As the package has an exposed pad, it is very important to connect it to an extended ground plane in order to reduce the thermal resistance junction-to-ambient.

Figure 13. Layout example



8.3 Thermal considerations

8.3.1 Thermal resistance R_{THJ-A}

R_{THJ-A} is the equivalent static thermal resistance junction-to-ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junction to the ambient. For this device, the path through the exposed pad is the one conducting the largest amount of heat. The static R_{THJ-A} measured on the application is about 40 °/W.

The junction temperature of the device is:

Equation 22

$$T_J = T_A + R_{thJA} \cdot P_{TOT}$$

The dissipated power of the device is tied to three different sources:

- Conduction losses due to the not insignificant $R_{DS(on)}$, which are equal to:

Equation 23

$$P_{ON} = R_{DS(on)} \cdot (I_{OUT})^2 \cdot D$$

where D is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN}, but in practice it is substantially higher than this value to compensate for the losses in the overall application. For this reason, the switching losses related to the $R_{DS(on)}$ increase compared to an ideal case.

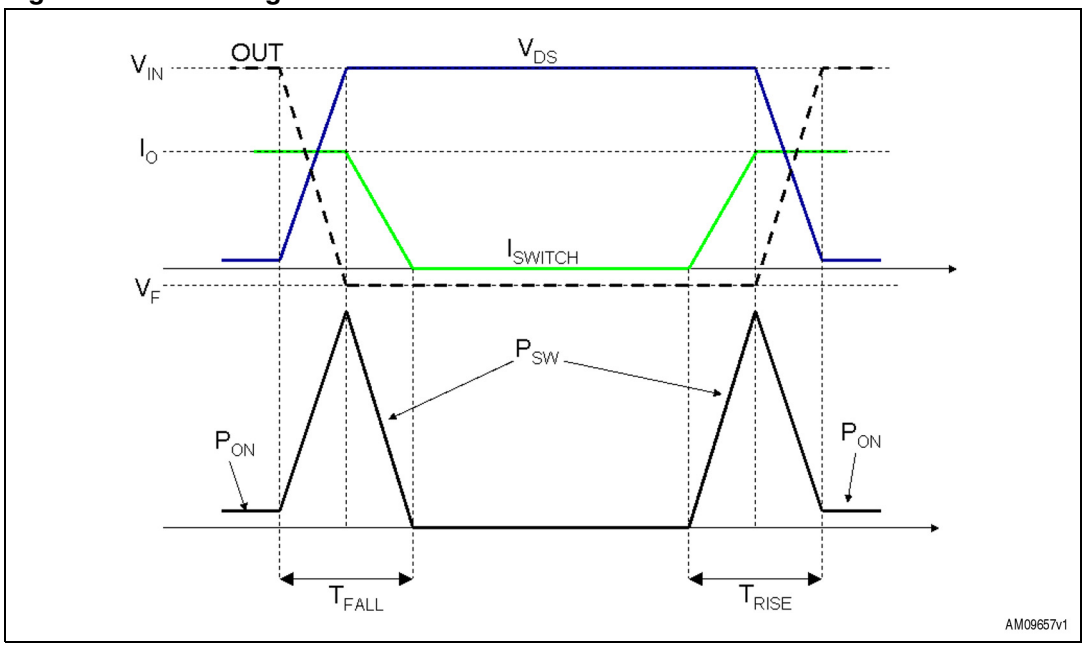
- Switching losses due to turning on and off. These are derived using the following equation:

Equation 24

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{ON} + T_{OFF})}{2} \cdot F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW}$$

where T_{RISE} and T_{FALL} represent the switching times of the power element that cause the switching losses when driving an inductive load (see *Figure 14*). T_{SW} is the equivalent switching time.

Figure 14. Switching losses



- Quiescent current losses.

Equation 25

$$P_Q = V_{IN} \cdot I_Q$$

where I_Q is the quiescent current.

Example:

- V_{IN} = 12 V
- V_{OUT} = 3.3 V
- I_{OUT} = 3 A

$R_{DS(on)}$ has a typical value of 0.25 @ 25 °C and increases up to a maximum value of 0.5. @ 150 °C. We can consider a value of 0.4 Ω.

T_{SW} is approximately 70 ns.

I_Q has a typical value of 5 mA @ V_{IN} = 12 V.

The overall losses are:

Equation 26

$$P_{TOT} = R_{DS(on)} \cdot (I_{OUT})^2 \cdot D + V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW} + V_{IN} \cdot I_Q =$$
$$= 0.4 \cdot 3^2 \cdot 0.3 + 12 \cdot 3 \cdot 70 \cdot 10^{-9} \cdot 250 \cdot 10^3 + 12 \cdot 2.5 \cdot 10^{-3} \cong 1.11W$$

The junction temperature of device is:

Equation 27

$$T_J = T_A + R_{thJA} \cdot P_{TOT}$$

Equation 28

$$T_J = 70 + 0.93 \cdot 42 \cong 116°C$$

8.3.2 Thermal impedance $Z_{THJ-A}(t)$

The thermal impedance of the system, considered as the device in the HSO8 package soldered on the application board, takes on an important rule when the maximum output power is limited by the static thermal performance and not by the electrical performance of the device. Therefore, the embedded power elements could manage a higher current but the system is already taking away the maximum power generated by the internal losses.

In case the output power increases, the thermal shutdown is triggered because the junction temperature triggers the designed thermal shutdown threshold.

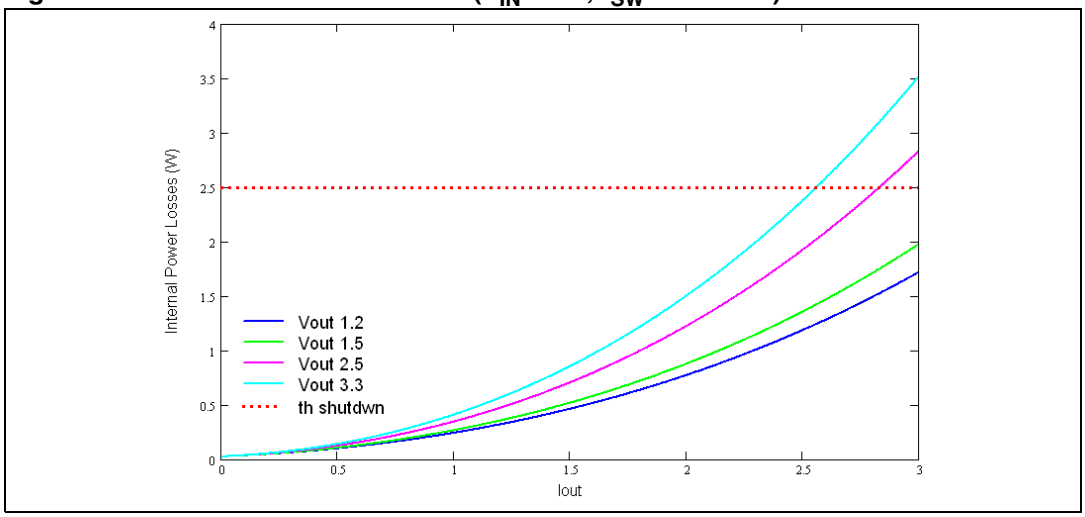
The R_{TH} is a static parameter of the package; it sets the maximum power loss which can be generated from the system given the operation conditions.

If we suppose, as an example, T_A = 40 °C, 140 °C is the maximum operating temperature before triggering the thermal shutdown and R_{TH} = 40 °C/W, therefore, the maximum power loss achievable with the thermal performance of the system is:

$$P_{MAX\ DC} = \frac{\Delta T}{R_{TH}} = \frac{T_{J\ MAX} - T_{AMB}}{R_{TH}} = \frac{100}{40} = 2.5W$$

Figure 15 represents the estimation of power losses for different output voltages at V_{IN}=5 V and T_{AMB}=40°C. The calculations are performed considering the $R_{DS(on)}$ of the power element equal to 0.4 A.

Figure 15. Power losses estimation (V_{IN} = 5 V, f_{SW} = 250 kHz)



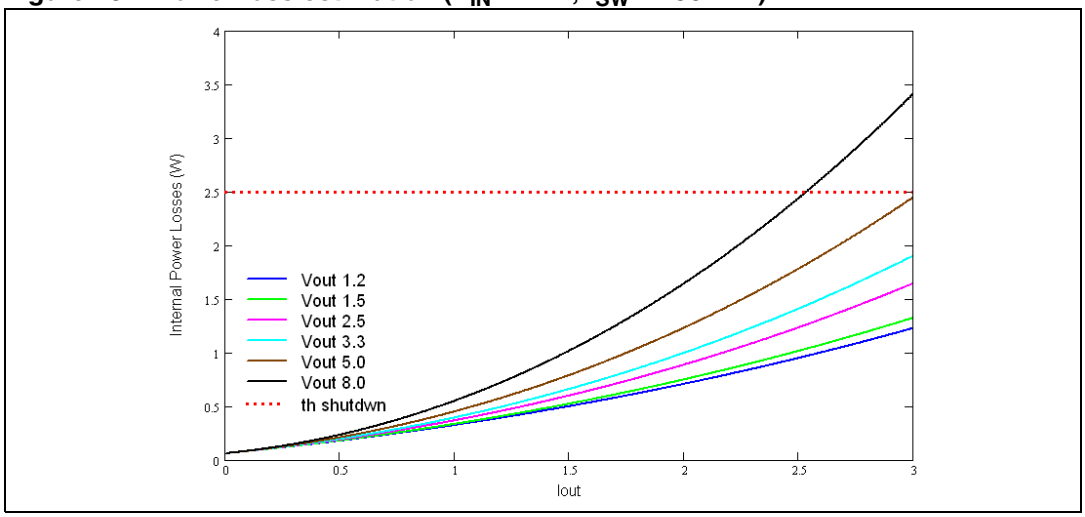
The red trace represents the maximum power which can be taken away, as calculated above, while the other traces are the total internal losses for different output voltages.

The embedded conduction losses are proportional to the duty cycle required for the conversion. Assuming the input voltage constant, the switching losses are proportional to the output current while the quiescent losses can be considered as constant.

As a consequence, in *Figure 15* the maximum power loss is for V_{OUT}=3.3 V, where the system can manage a continuous output current up to 2.5 A. The device could deliver a continuous output current up to 3 A to the load, however, the maximum power loss of 2.5 W is reached with an output current of 2.5 A, so the maximum output power is derated.

Figure 16 plots the power losses for V_{IN}=12 V and main output rails.

Figure 16. Power loss estimation (V_{IN} = 12 V, f_{SW} = 250 kHz)



At V_{IN}=12 V and V_{OUT}=5 V the device can deliver 3 A continuously (see *Figure 17*) because the total power loss is now lower than 2.5 W ((Δ switching loss +Δ quiescent loss) < Δ conduction loss).

As a consequence, the calculation of the internal power losses must be done for each specific operating condition given by the final application.

In applications where the current to the output is pulsed, the thermal impedance should be considered instead of the thermal resistance.

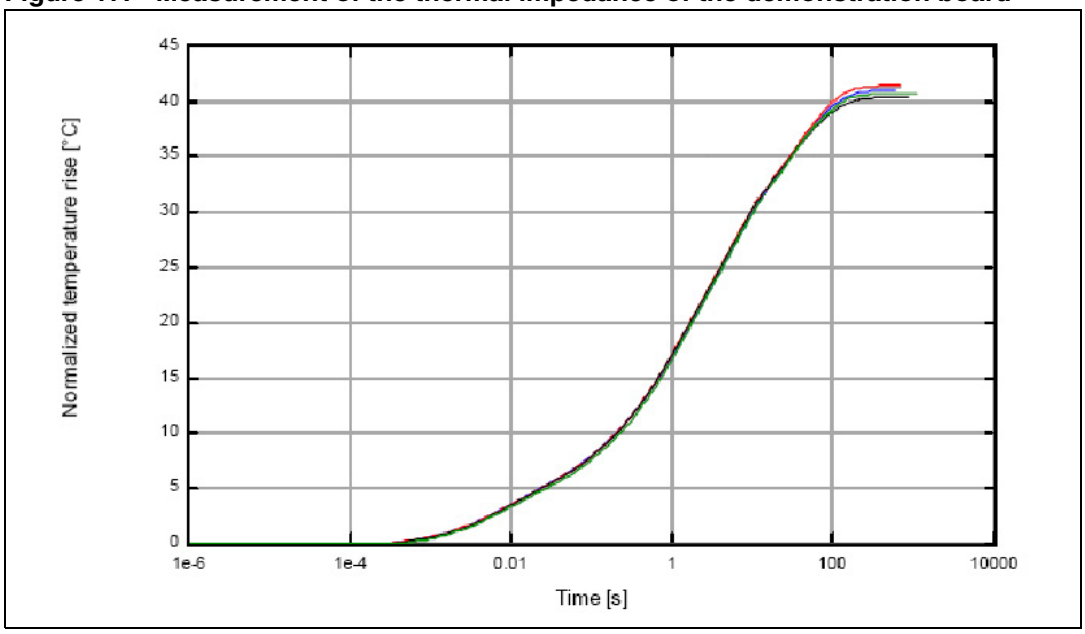
The thermal impedance of the system could be much lower than the thermal resistance, which is a static parameter. And so the maximum power losses can be higher than 2.5 W if a pulsed output power is requested from the load:

$$P_{MAX}(t) = \frac{\Delta T}{Z_{TH}(t)} = \frac{T_{J\,MAX} - T_{AMB}}{Z_{TH}(t)}$$

Therefore, depending on the pulse duration and its frequency, the maximum output current can be delivered to the load.

The characterization of the thermal impedance is strictly dependent on the layout of the board. In *Figure 17* the measurement of the thermal impedance of the demonstration board of the A5975D is provided.

Figure 17. Measurement of the thermal impedance of the demonstration board



As can be seen, for example, for load pulses with a duration of 1 second, the actual thermal impedance is lower than 20 °C/W. This means that, for short pulses, the device can deliver a higher output current value.

8.4 RMS current of the embedded power MOSFET

As the A5975D embeds the high side switch, the internal power dissipation is sometimes the bottleneck for the output current capability (refer to *Section 8.3* for the estimation of the operating temperature).

Nevertheless, as mentioned in the general description *on page 1*, the device can manage a continuous output current of 3 A in most of the application conditions.

However, the rated maximum RMS current of the power elements is 2 A, where:

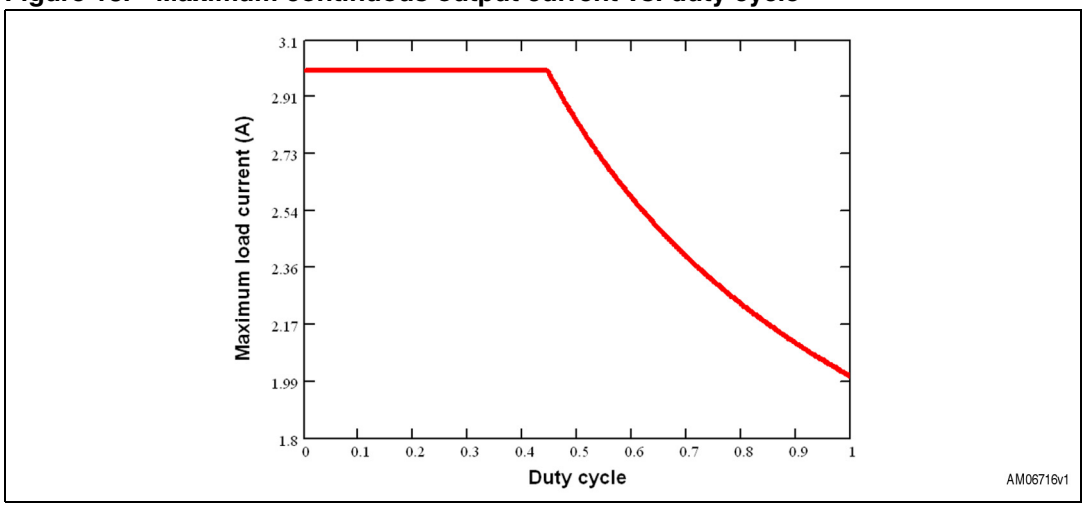
$$I_{RMS\ HS} = I_{LOAD} \cdot \sqrt{D}$$

and the real duty cycle D:

$$D = \frac{V_{OUT} + (R_{DS\ (on)\ LS} + DCR) \cdot I_{LOAD}}{V_{IN} + (R_{DS\ (on)\ LS} - R_{DS\ (on)\ HS}) \cdot I_{LOAD}}$$

Fixing the limit of 2 A for $I_{RMS\ HS}$, the maximum output current can be derived, as illustrated in *Figure 18*.

Figure 18. Maximum continuous output current vs. duty cycle



8.5 Short-circuit protection

In overcurrent protection mode, when the peak current reaches the current limit, the device reduces the T_{ON} down to its minimum value (approximately 250 nsec) and the switching frequency to approximately one third of its nominal value even when synchronized to an external signal (see *Section 5.4: Current protection*). In these conditions, the duty cycle is strongly reduced and, in most applications, this is enough to limit the current to I_{LIM}. In any event, in case of heavy short-circuit at the output (V_O = 0 V) and depending on the application conditions (V_{CC} value and parasitic effect of external components), the current peak could reach values higher than I_{LIM}.

This can be understood considering the inductor current ripple during the ON and OFF phases:

- ON phase

Equation 29

$$\Delta I_{L\,TON} = \frac{V_{IN} - V_{out} - (DCR_L + R_{DS(on)}) \cdot I}{L}(T_{ON})$$

- OFF phase

Equation 30

$$\Delta I_{L\,TOFF} = \frac{-(V_D + V_{out} + DCR_L \cdot I)}{L}(T_{OFF})$$

where V_D is the voltage drop across the diode, DCR_L is the series resistance of the inductor.

In short-circuit conditions, V_{OUT} is negligible, so during T_{OFF} the voltage across the inductor is very small, as equal to the voltage drop across parasitic components (typically the DCR of the inductor and the V_{FW} of the free-wheeling diode), while during T_{ON}, the voltage applied to the inductor is maximized instead as approximately equal to V_{IN}.

So, *Equation 29* and *30* in overcurrent conditions can be simplified to:

Equation 31

$$\Delta I_{L\,TON} = \frac{V_{IN} - (DCR_L + R_{DS(on)}) \cdot I}{L}(T_{ON\,MIN}) \cong \frac{V_{IN}}{L}(250ns)$$

considering T_{ON} which has been already reduced to its minimum.

Equation 32

$$\Delta I_{L\,TOFF} = \frac{-(V_D + V_{out} + DCR_L \cdot I)}{L}(3 \cdot T_{SW}) \cong \frac{-(V_D + V_{out} + DCR_L \cdot I)}{L}(12\mu s)$$

considering that f_{SW} has already been reduced to one third of the nominal.

In case a short-circuit at the output is applied, and V_{IN} = 12 V, the inductor current is controlled in most of the applications (see *Figure 19*). When the application must sustain the short-circuit condition for an extended period, the external components (mainly the inductor and diode) must be selected based on this value.

In case the V_{IN} is very high, it may happen that the ripple current during T_{OFF} (*Equation 32*) does not compensate the current increase during T_{ON}(*Equation 31*). *Figure 21* shows an example of a power-up phase with $V_{IN} = V_{IN\,MAX}$ = 36 V, where $\Delta_{IL\,TON} > \Delta_{IL\,TOFF}$ so the current escalates and the balance between *Equation 31* and occurs at a current slightly higher than the current limit. This must be taken into account in particular to avoid the risk of an abrupt inductor saturation.

Figure 19. Short-circuit current V_{IN} = 12 V

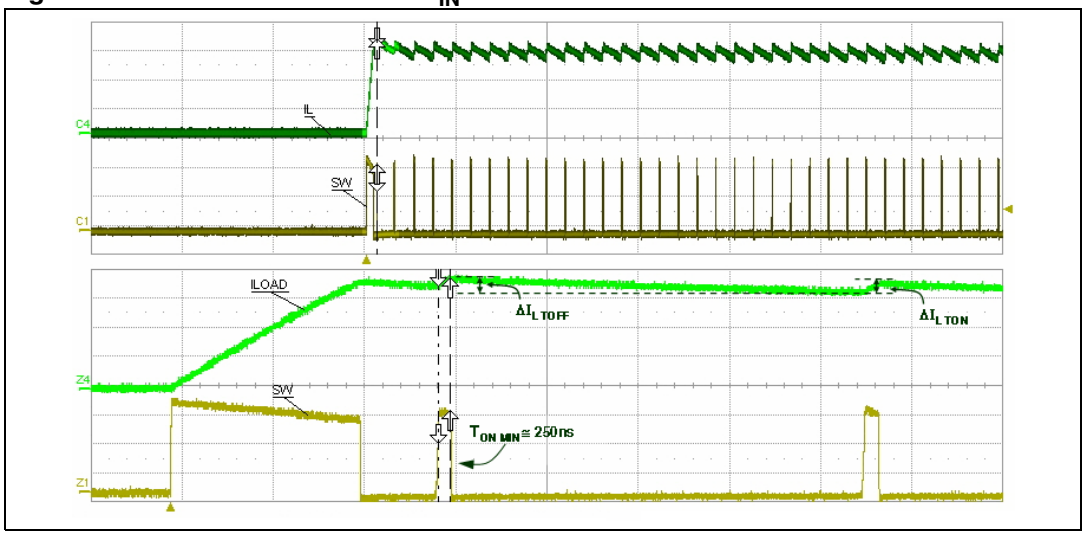


Figure 20. Short-circuit current V_{IN} = 24 V

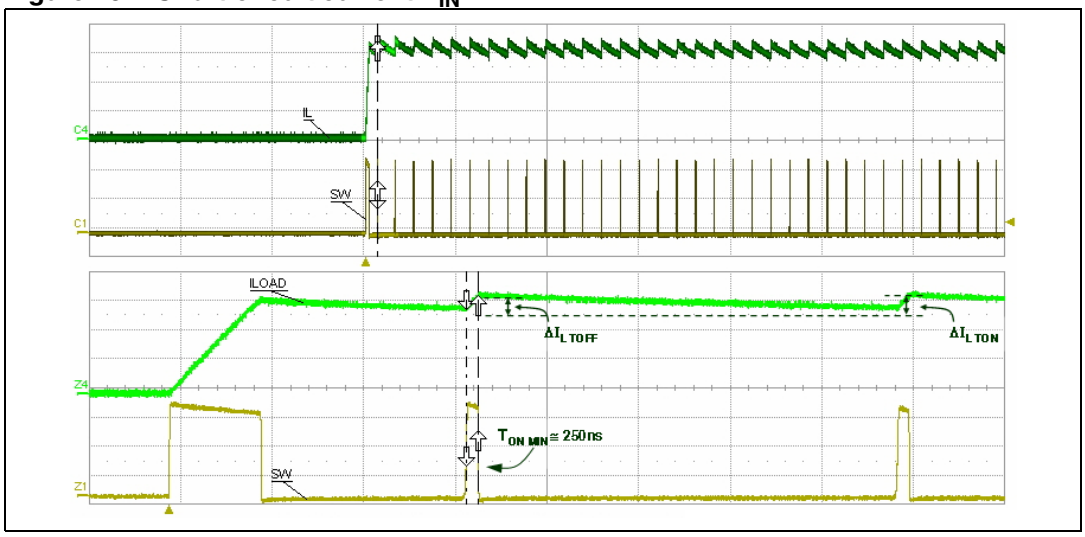
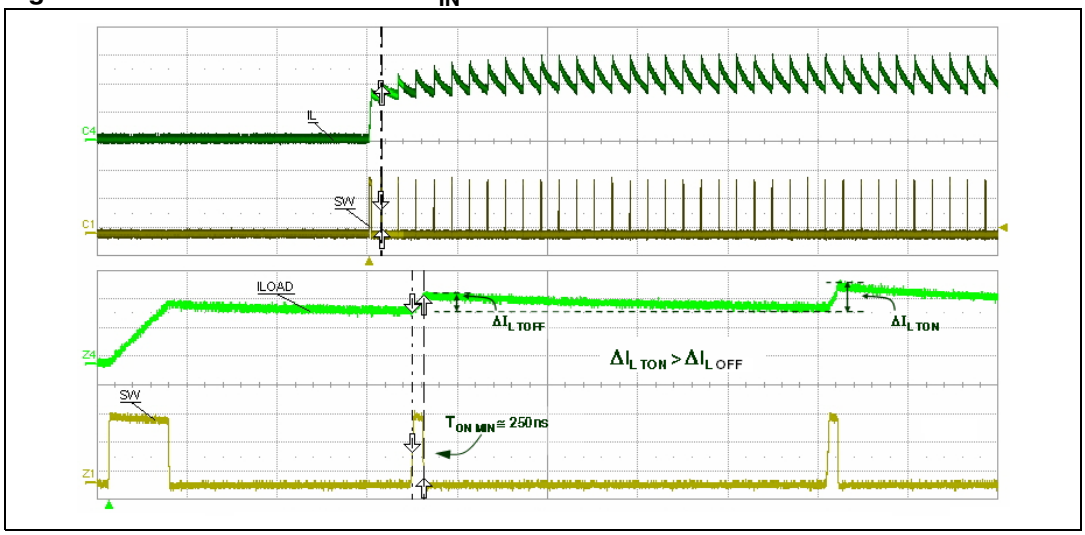


Figure 21. Short-circuit current V_{IN} = 36 V



8.6 Application circuit

Figure 22 shows the demonstration board application circuit, where the input supply voltage, V_{CC}, can range from 4 V to 36 V and the output voltage is adjustable from 1.235 V to 6.3 V due to the voltage rating of the output capacitor.

Figure 22. Demonstration board application circuit

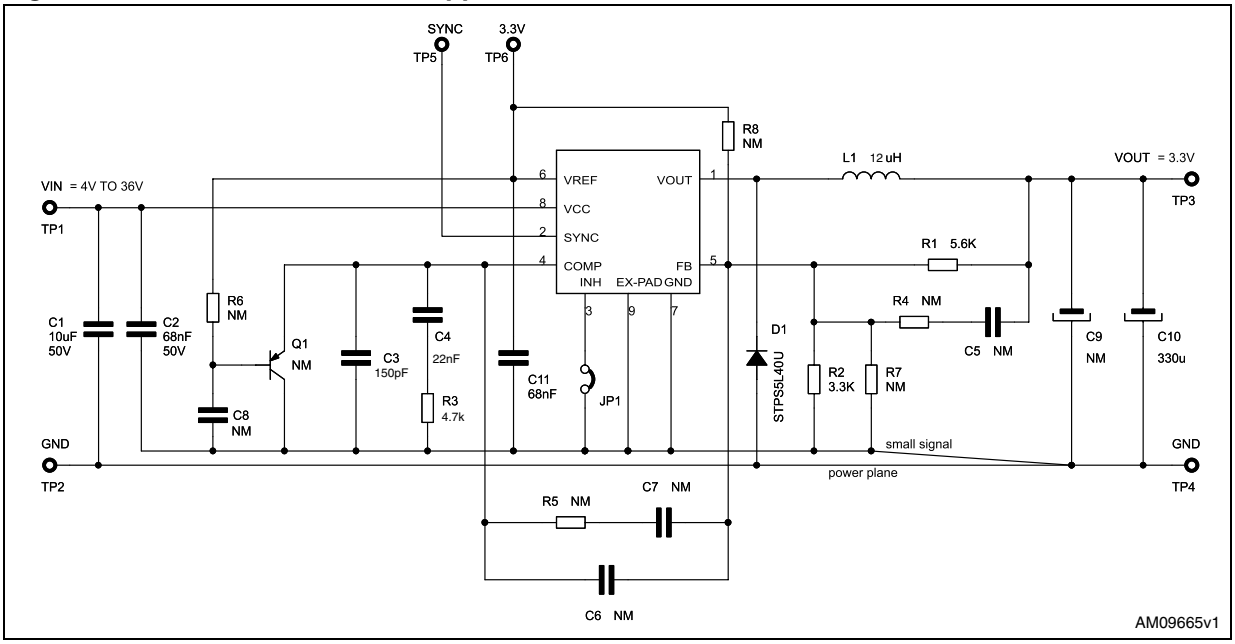
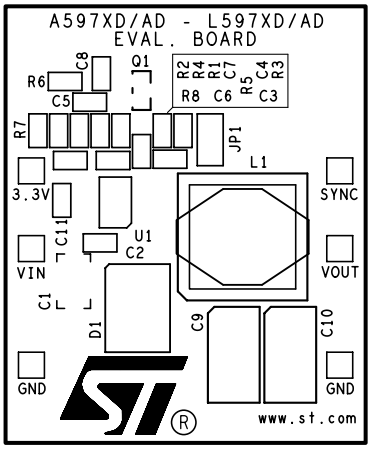


Table 9. Component list

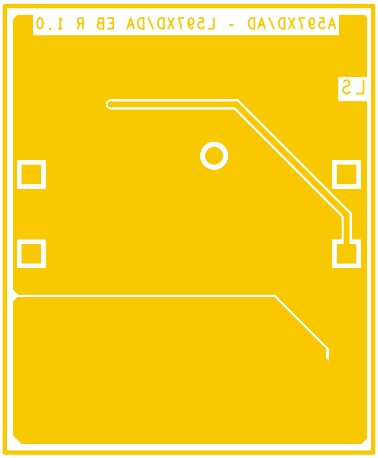
Reference	Part number	Description	Manufacturer
C1	UMK325BJ106MM-T	10 µF, 50 V	Taiyo Yuden
C2		68 nF, 5%, 0603	
C3		120 pF, 5%, 0603	
C4		10 nF, 5%, 0603	
C10	POSCAP 6TVB330ML	330 µH, 25 mΩ	Sanyo
R1		5.6 kΩ, 1%, 0.1 W 0603	
R2		3.3 kΩ, 1%, 0.1 W 0603	
R3		10 kΩ, 1%, 0.1 W 0603	
D1	STPS5L60S	5 A, 60 V	STMicroelectronics
L1	MSS1246T-123	12 µH, $I_{RMS\ 20°C}$ 3A	Coilcraft

Figure 23. PCB layout (component side)



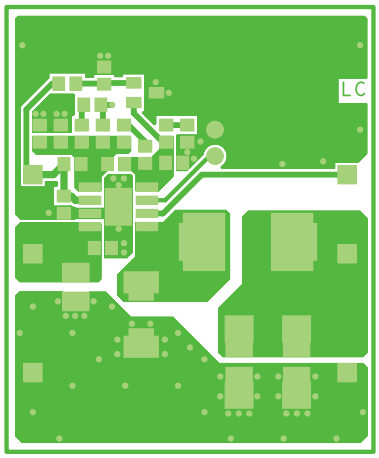
AM09666v1

Figure 24. PCB layout (bottom side)



AM09667v1

Figure 25. PCB layout (front side)



8.7 Positive buck-boost regulator

The device can be used to implement a step-up/down converter with a positive output voltage.

The output voltage is given by:

Equation 33

$$V_{OUT} = V_{IN} \cdot \frac{D}{1 - D}$$

where the ideal duty cycle D for the buck-boost converter is:

Equation 34

$$D = \frac{V_{OUT}}{V_{IN} + V_{OUT}}$$

However, due to power losses in the passive elements, the real duty cycle is always higher than this. The real value (that can be measured in the application) should be used in the following formulas.

The peak current flowing in the embedded switch is:

Equation 35

$$I_{SW} = \frac{I_{LOAD}}{1 - D} + \frac{I_{RIPPLE}}{2} = \frac{I_{LOAD}}{1 - D} + \frac{V_{IN}}{2 \cdot L} \cdot \frac{D}{f_{SW}}$$

while its average current is equal to:

Equation 36

$$I_{SW} = \frac{I_{LOAD}}{1 - D}$$

This is due to the fact that the current flowing through the internal power switch is delivered to the output only during the OFF phase.

The switch peak current must be lower than the minimum current limit of the overcurrent protection (see *Table 4* for details) while the average current must be lower than the rated DC current of the device.

As a consequence, the maximum output current is:

Equation 37

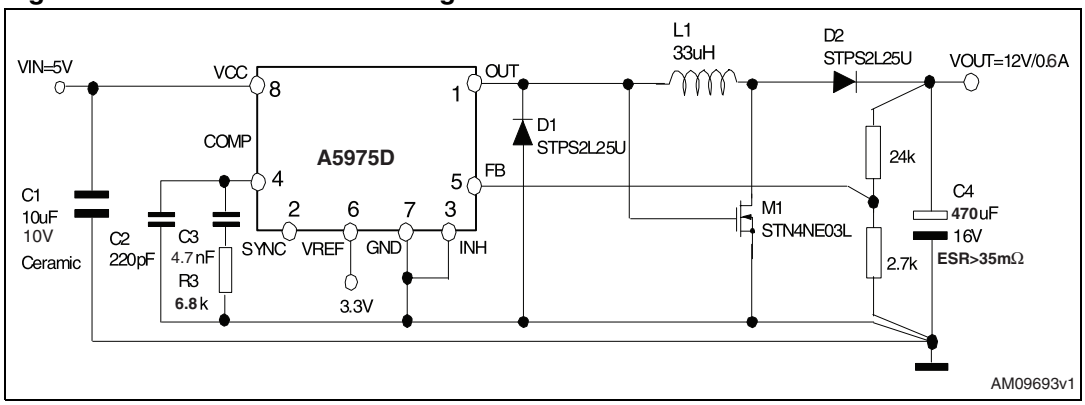
$$I_{OUT\ MAX} \cong I_{SW\ MAX} \cdot (1 - D)$$

where $I_{SW\ MAX}$ represents the rated current of the device.

The current capability is reduced by the term (1-D) and so, for example, with a duty cycle of 0.5, and considering an average current through the switch of 3 A, the maximum output current deliverable to the load is 1.5 A.

Figure 26 below shows the schematic circuit of this topology for a 12 V output voltage and 5 V input.

Figure 26. Positive buck-boost regulator



8.8 Negative buck-boost regulator

In *Figure 27*, the circuit schematic for a standard buck-boost topology is shown. The output voltage is:

Equation 38

$$V_{OUT} = -V_{IN} \cdot \frac{D}{1 - D}$$

where the ideal duty cycle D for the buck-boost converter is:

Equation 39

$$D = \frac{-V_{OUT}}{V_{IN} - V_{OUT}}$$

The considerations given in *Section 8.8* for the real duty cycle are still valid here. Also *Equation 35* to *37* can be used to calculate the maximum output current. So, for example, considering the conversion V_{IN} = 12 V to V_{OUT} = -5 V, I_{LOAD} = 0.5 A:

Equation 40

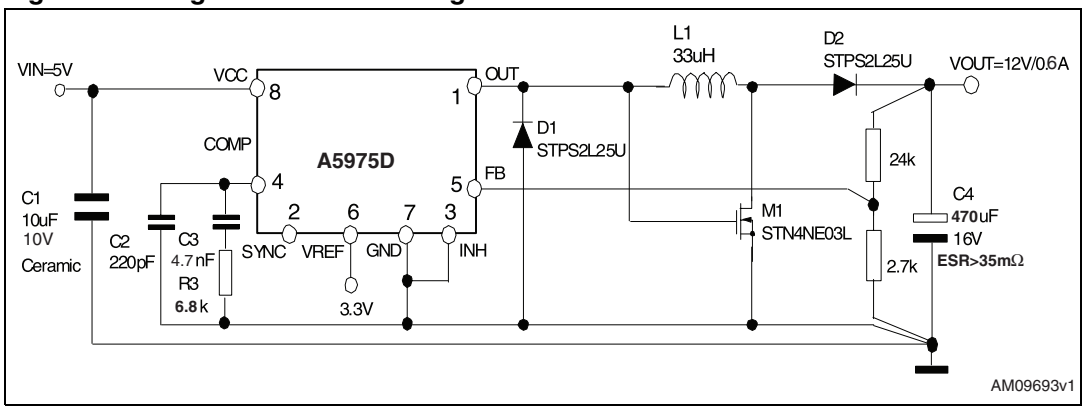
$$D = \frac{5}{5+12} = 0.706$$

Equation 41

$$I_{SW} = \frac{I_{LOAD}}{1-D} = \frac{0.5}{1-0.706} = 1.7A$$

An important point to take into account is that the ground pin of the device is connected to the negative output voltage. Therefore, the device is subjected to a voltage equal to V_{IN}-V_O, which must be lower than 36 V (the maximum operating input voltage).

Figure 27. Negative buck-boost regulator



8.9 Floating boost current generator

The A5975D does not support a nominal boost conversion as this topology requires a low side switch, however, a floating boost can be useful in applications where the load can be floating. A typical example is a current generator for LED driving, as the LED does not require a connection to the ground.

Figure 28. Floating boost topology

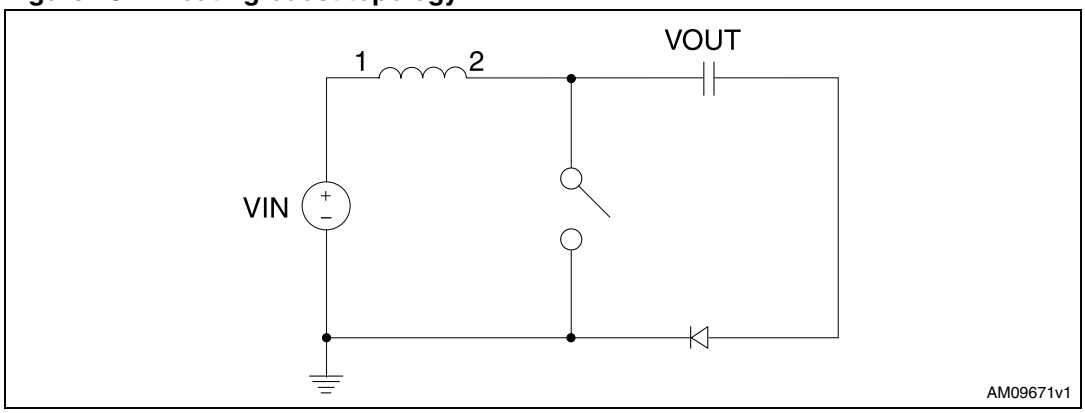
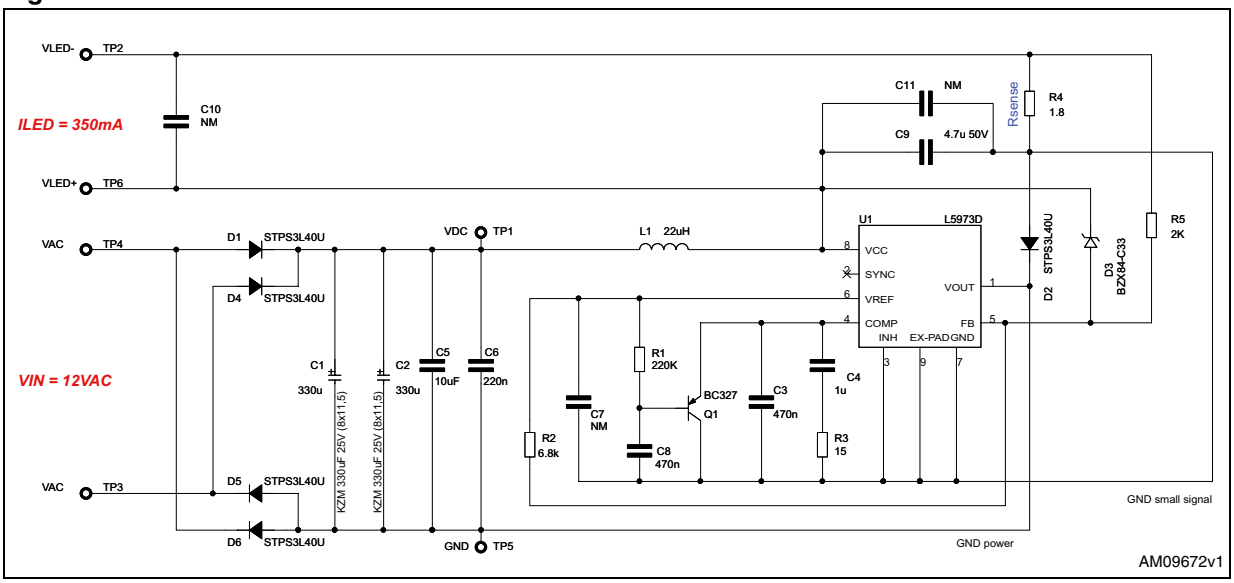


Figure 29. 350 mA LED boost current source



The device is powered from the output voltage so the maximum voltage drop across the LEDs and resistor sense is 36 V.

The output voltage is given by:

Equation 42

$$V_{OUT} = \frac{V_{IN}}{1 - D}$$

where the ideal duty cycle D for the boost converter is:

Equation 43

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

As for positive and inverting buck-boost (see *Section 8.7* and *Section 8.8*.) the measured real duty cycle must be used to calculate the switch current level.

The peak current flowing in the embedded switch is:

Equation 44

$$I_{SW} = \frac{I_{LOAD}}{1 - D} + \frac{I_{RIPPLE}}{2} = \frac{I_{LOAD}}{1 - D} + \frac{V_{IN}}{2 \cdot L} \cdot \frac{D}{f_{SW}}$$

while its average current is equal to:

Equation 45

$$I_{SW} = \frac{I_{LOAD}}{1 - D}$$

This is due to the fact that the current flowing through the internal power switch is delivered to the output only during the OFF phase.

The switch peak current must be lower than the minimum current limit of the overcurrent protection (see *Table 4* for details) while the average current must be lower than the rated DC current of the device.

As a consequence, the maximum output current is:

Equation 46

$$I_{OUT\ MAX} \cong I_{SW\ MAX} \cdot (1 - D)$$

where $I_{SW\ MAX}$ represents the rated current of the device.

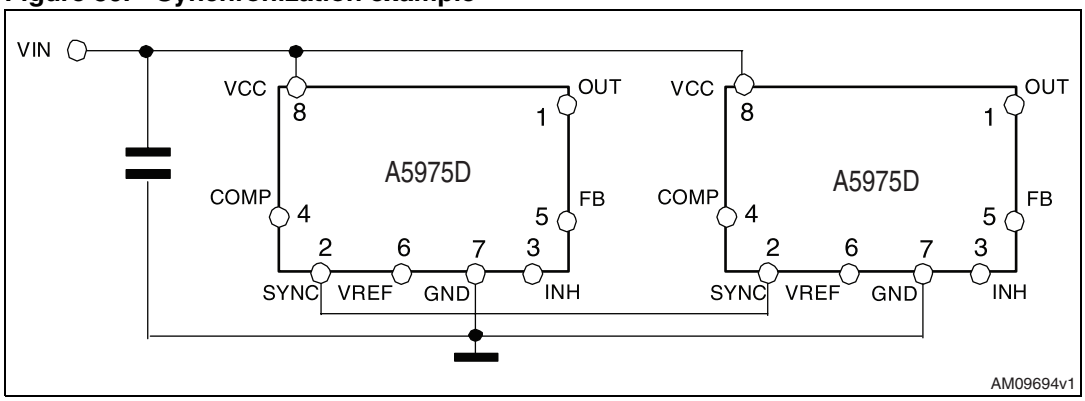
Figure 29 shows a tested circuit to implement a boost current source for high current LED driving (350 mA). To implement a boost conversion the LED string must be composed of a minimum device number having a total voltage drop larger than maximum input voltage.

The input voltage can be either DC or AC thanks to the input bridge rectifier. In the case of a DC voltage source D1, D2, D3, D4, C1, and C2 can be removed from the circuit and 1 µF capacitor value can be used for C5.

8.10 Synchronization example

See *Section 5.3* for details.

Figure 30. Synchronization example



8.11 Compensation network with MLCC at the output

The A5975D standard compensation network (please refer to *Figure 1* and *Section 7*) introduces a single zero and a low frequency pole in the system bandwidth, so a high ESR output capacitor must be selected to compensate the 180-degree phase shift given by the LC double pole.

The selection of the output capacitor must guarantee that the zero introduced by this component is inside the designed system bandwidth and close to the frequency of the double pole introduced by the LC filter. A general rule for the selection of this compound for the system stability is provided in *Equation 47*.

Equation 47

$$f_{Z\,ESR} = \frac{1}{2 \cdot \pi \cdot ESR \cdot C_{OUT}} < bandwidth$$

$$f_{LC} < f_{Z\,ESR} < 10 \cdot f_{LC}$$

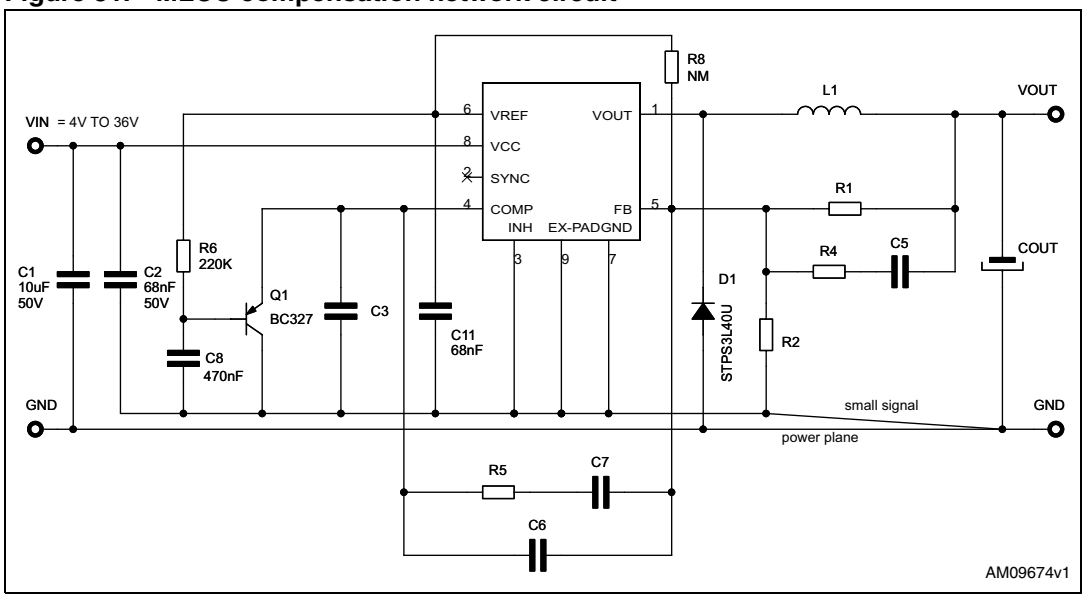
MLCCs (multiple layer ceramic capacitor) with values in the range of 10 µF-22 µF and rated voltages in the range of 10 V-25 V are available today at relatively low cost from many manufacturers.

These capacitors have very low ESR values (a few mΩ) and are therefore occasionally used for the output filter in order to reduce the voltage ripple and the overall size of the application.

However, the zero given by the output capacitor falls outside the designed bandwidth and so the system becomes unstable with the standard compensation network.

Figure 31 shows the type III compensation network stabilizing the system with ceramic capacitors at the output (the optimum components value depends on the application). This configuration introduces two zeros and a low frequency pole in the designed bandwidth and so guarantees a proper phase margin.

Figure 31. MLCC compensation network circuit

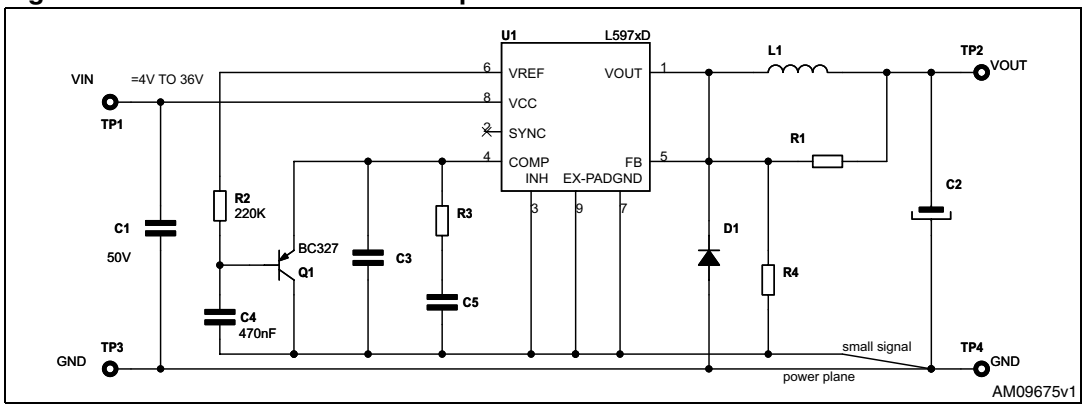


8.12 External soft-start network

At startup, the device can quickly increase the current up to the current limit in order to charge the output capacitor. If soft ramp-up of the output voltage is required, an external soft-start network can be implemented, as shown in *Figure 32*. The capacitor C is charged up to an external reference through R and the BJT clamps the COMP pin.

This clamps the duty cycle, limiting the slew rate of the output voltage.

Figure 32. Soft-start network example



9 Typical characteristics

Figure 33. Line regulator

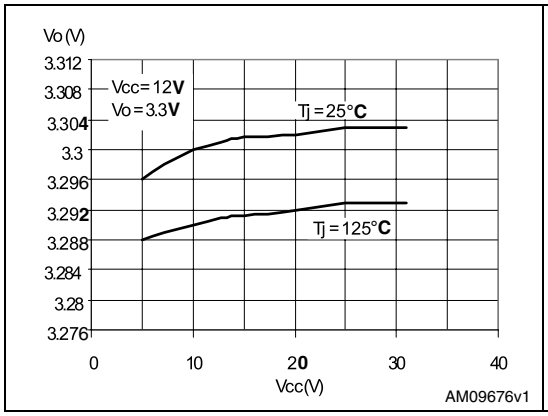


Figure 34. Shutdown current vs. junction temperature

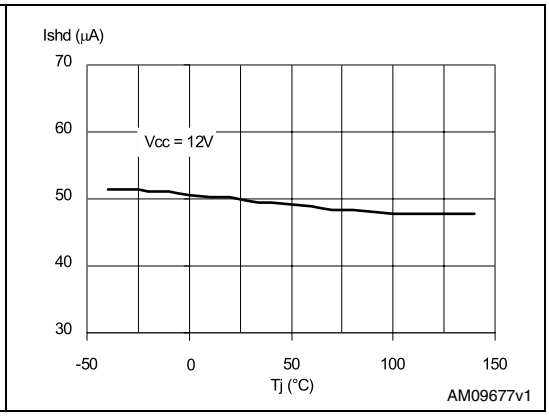


Figure 35. Output voltage vs. junction temperature

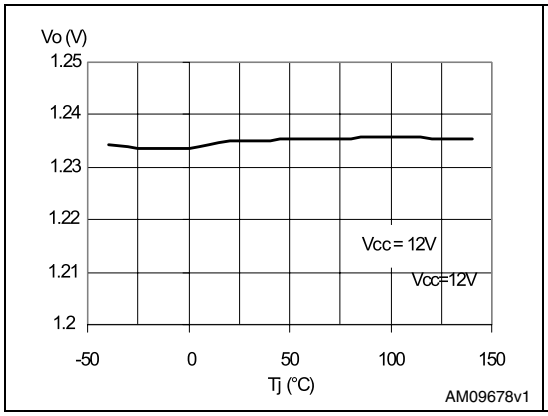


Figure 36. Switching frequency vs. junction temperature

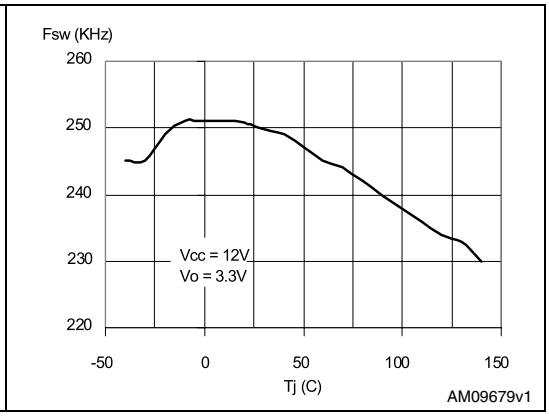


Figure 37. Quiescent current vs. junction temperature

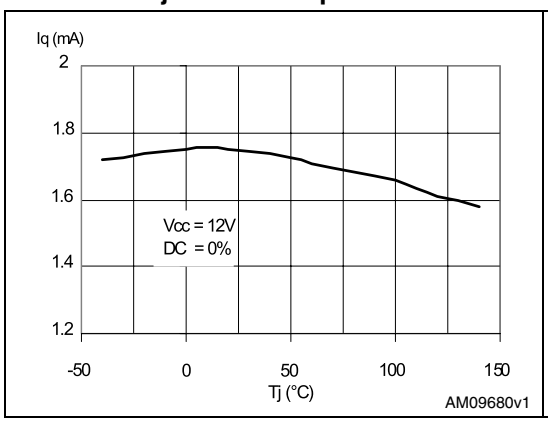


Figure 38. Junction temperature vs. output current (V_{IN} 5 V)

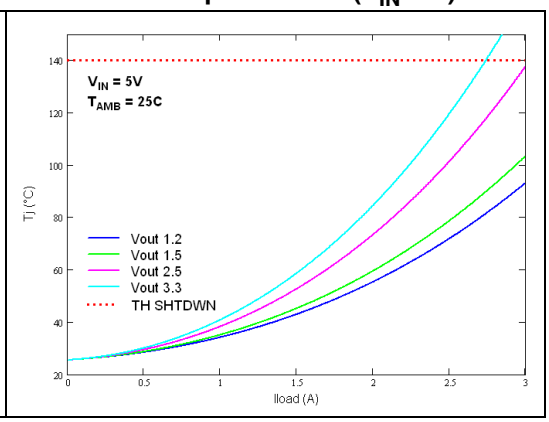


Figure 39. Junction temperature vs. output current (V_{IN} 12 V)

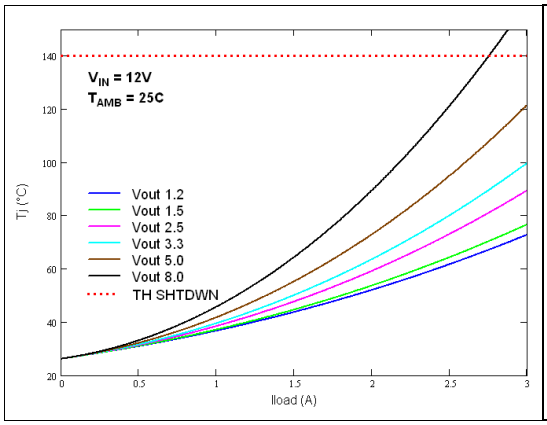


Figure 40. Efficiency vs. output current (V_{IN} 12 V)

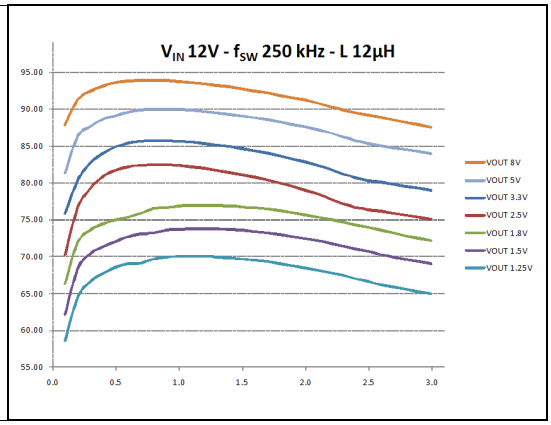
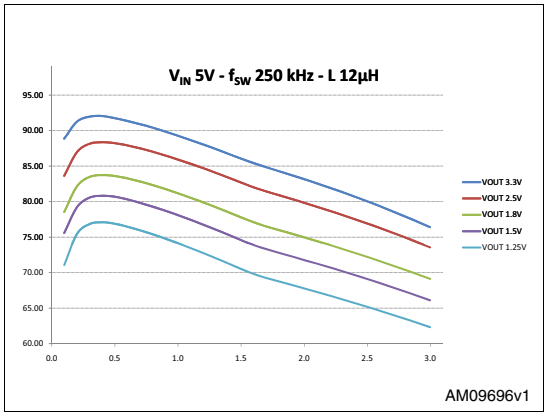


Figure 41. Efficiency vs. output current (V_{IN} 5 V)



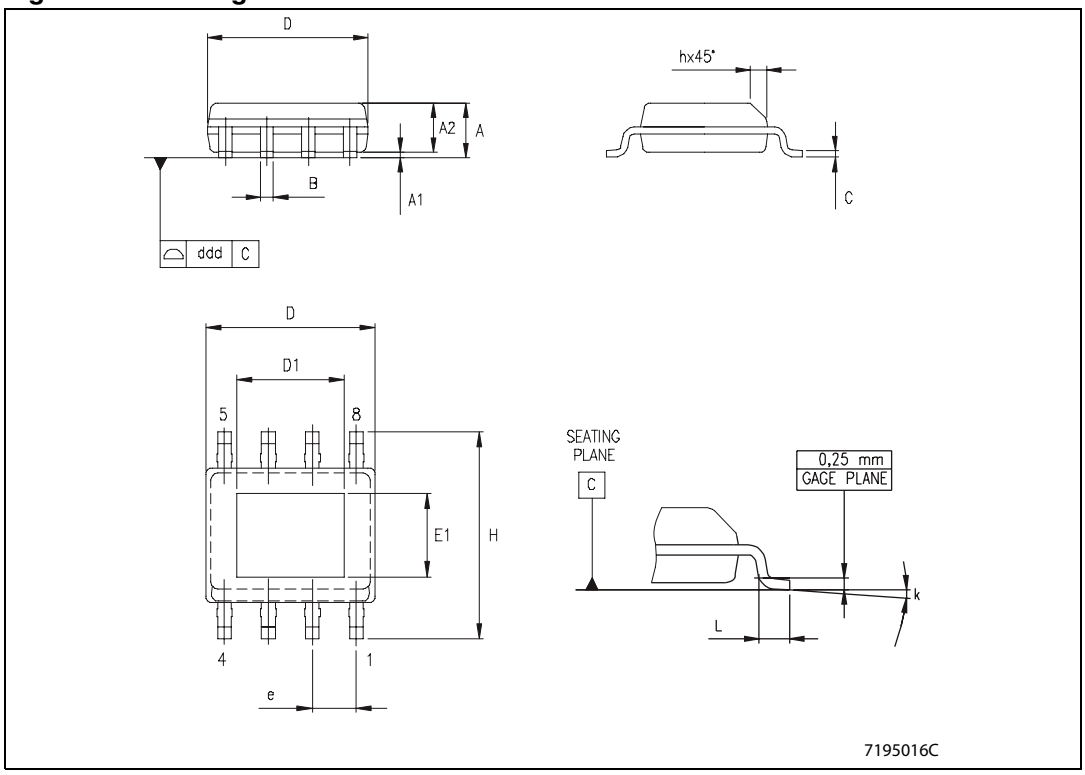
10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 10. HSOP8 mechanical data

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.70			0.0669
A1	0.00		0.10		0.00	0.0039
A2	1.25			0.0492		
b	0.31		0.51	0.0122		0.0201
c	0.17		0.25	0.0067		0.0098
D	4.80	4.90	5.00	0.1890	0.1929	0.1969
D1	3	3.1	3.2	0.118	0.122	0.126
E	5.80	6.00	6.20	0.2283		0.2441
E1	3.80	3.90	4.00	0.1496		0.1575
E2	2.31	2.41	2.51	0.091	0.095	0.099
e		1.27				
h	0.25		0.50	0.0098		0.0197
L	0.40		1.27	0.0157		0.0500
k	0° (min), 8° (max)					
ccc			0.10			0.0039

Figure 42. Package dimensions



11 Ordering information

Table 11. Ordering information

Order codes	Package	Packaging
A5975D	HSOP8	Tube
A5975DTR		Tape and reel

12 Revision history

Table 12. Document revision history

Date	Revision	Changes
19-Apr-2011	1	Initial release

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