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November 2010

NC7SV00 TinyLogic[®] ULP-A 2-Input NAND Gate

Features

- 0.9V to 3.6V V_{CC} Supply Operation
- 3.6V Over-Voltage Tolerant I/Os at Vcc from 0.9V to 3.6V
- Extremely High Speed tpd
 - 1.0ns: Typical for 2.7V to 3.6V V_{CC}
 - 1.2ns: Typical for 2.3V to 2.7V V_{CC}
 - 2.0ns: Typical for 1.65V to 1.95V V_{CC}
 - 3.2ns: Typical for 1.4V to 1.6V V_{CC}
 - 6.0ns: Typical for 1.1V to 1.3V V_{CC}
 - 13.0ns: Typical for 0.9V V_{CC}
- Power-Off High-Impedance Inputs and Outputs
- High Static Drive (I_{OH}/I_{OL})
 - ±24mA at 3.00V V_{CC}
 - ±18mA at 2.30V V_{CC}
 - ±6mA at 1.65V V_{CC}
 - $\pm 4mA$ at 1.4V V_{CC}
 - $\pm 2mA$ at 1.1V V_{CC}
 - $\pm 0.1 mA$ at 0.9V V_{CC}
- Uses Proprietary Quiet Series[™] Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages
- Ultra-Low Dynamic Power

Description

The NC7SV00 is a single two-input NAND gate from Fairchild's Ultra-Low Power (ULP-A) Series of TinyLogic®. ULP-A is ideal for applications that require extreme high speed, high drive, and low power. This product is designed for a wide low-voltage operating range (0.9V to 3.6V $V_{\rm CC}$) and applications that require more drive and speed than the TinyLogic® ULP series, but still offer best-in-class, low-power operation.

The NC7SV00 is uniquely designed for optimized power and speed and is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SV00P5X	V00	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel
NC7SV00L6X	F5	6-Lead MicroPak™, 1.00mm Wide	5000 Units on Tape & Reel
NC7SV00FHX	F5	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	5000 Units on Tape & Reel

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Battery Life

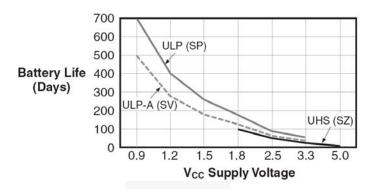
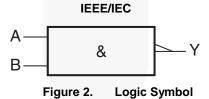


Figure 1. Battery Life vs. V_{CC} Supply Voltage

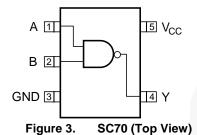
Notes:

- TinyLogic[®] ULP and ULP-A with up to 50% less power consumption can extend battery life significantly. Battery Life = (V_{battery}•I_{battery}•.9)/(P_{device})/24hrs/day where, P_{device} = (I_{CC}• V_{CC}) + (C_{PD}+ C_L) • V_{CC2}• f.
- 2. Assumes ideal 3.6V Lithium lon battery with current rating of 900mAH and derated 90% and device frequency at 10MHz, with C_L =15pF load.

Connection Diagram



Pin Configurations



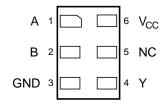


Figure 4. MicroPak™ (Top Through View)

Pin Definitions

Pin # SC70	Pin # MicroPak™	Name	Description
1	1	A	Input
2	2	В	Input
3	3	GND	Ground
4	4	Υ	Output
	5	NC	No Connect
5	6	Vcc	Supply Voltage

Function Table

Inp	uts	Output			
Α	В	Y			
L	L	Н			
L	Н	Н			
Н	L	Н			
Н	Н	L			

H=HIGH Logic Level L=LOW Logic Level

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Para	Min.	Max.	Unit	
V _{CC}	Supply Voltage	-0.5	4.6	V	
V _{IN}	DC Input Voltage		-0.5	4.6	V
\/	DC Output Valtage	HIGH or LOW State ⁽³⁾	-0.5	V _{CC} + 0.5	W
V _{OUT}	DC Output Voltage	V _{CC} =0V	-0.5	4.6	V
I _{IK}	DC Input Diode Current	$V_{IN} < 0V$		-50	mA
	D0.0 + + D1. + O	V _{OUT} < 0V		-50	
l _{OK}	I _{OK} DC Output Diode Current	$V_{OUT} > V_{CC}$		+50	mA
I _{OH} /I _{OL}	DC Output Source/Sink Curren		±50	mA	
I _{CC} or I _{GND}	DC V _{CC} or Ground Current per	Supply Pin		±50	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
TJ	Junction Temperature Under B	ias	\(+150	°C
TL	Junction Lead Temperature, So	oldering 10 Seconds		+260	°C
		SC70-5		150	
P_{D}	Power Dissipation at +85°C	MicroPak™-6		130	mW
		MicroPak2™-6		120	
FCD	Human Body Model, JEDEC:JE		4000	\/	
ESD	Charge Device Model, JEDEC:JESD22-C101			2000	V

Note:

3. IO absolute maximum rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit	
V _{CC}	Supply Voltage		0.9	3.6	V	
V _{IN}	Input Voltage		0	3.6	V	
V	Output Valtage	V _{CC} =0V	0	3.6	V	
V _{OUT}	Output Voltage	HIGH or LOW State	0	V _{CC}	7 V	
		V _{CC} =3.0V to 3.6V		±24.0		
		V _{CC} =2.3V to 3.6V		±18.0		
1 /1	Output Current in 1 /1	V _{CC} =1.65V to 1.95V		±6.0	m A	
I _{OH} /I _{OL}	Output Current in I _{OH} /I _{OL}	V _{CC} =1.4V to 1.6V		±4.0	mA	
		V _{CC} =1.1V to 1.3V		±2.0		
		V _{CC} =0.9V		±0.1		
T _A	Operating Temperature, Free Air		-40	+85	°C	
Δt/ΔV	Minimum Input Edge Rate	V _{IN} =0.8V to 2.0, V _{CC} =3.0V		10	ns/V	
		SC70-5		425		
θ_{JA}	Thermal Resistance	MicroPak™-6		500	°C/W	
		MicroPak2™-6		560		

Note:

4. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

		.,		T _A =2	5°C	T _A =-40	to 85°C	11.24
Symbol	Parameter	V _{cc}	Conditions	Min.	Max.	Min.	Max.	Units
		0.90		.65 x V _{CC}		.65 x V _{CC}		
		$1.10 \le V_{CC} \le 1.30$]	.65 x V _{CC}		.65 x V _{CC}		
	HIGH Level Input	$1.40 \le V_{CC} \le 1.60$.65 x V _{CC}		.65 x V _{CC}		Ī ,,
V _{IH}	Voltage	$1.65 \le V_{CC} \le 1.95$.65 x V _{CC}		.65 x V _{CC}		V
		$2.30 \leq V_{CC} \leq 2.70$		1.6		1.6		
		$2.70 \leq V_{CC} \leq 3.60$		2.0		2.0		
		0.90			.35 x V _{CC}		.35 x V _{CC}	
		$1.10 \le V_{CC} \le 1.30$.35 x V _{CC}		.35 x V _{CC}	
	LOW Level Input	$1.40 \le V_{CC} \le 1.60$.35 x V _{CC}		.35 x V _{CC}	.,
V _{IL}	Voltage	$1.65 \leq V_{CC} \leq 1.95$.35 x V _{CC}		.35 x V _{CC}	V
		$2.30 \leq V_{CC} \leq 2.70$			0.7		0.7	
		$2.70 \leq V_{CC} \leq 3.60$			0.8		0.8	
1		0.90		V _{CC} -0.1		V _{CC} -0.1		
		$1.10 \le V_{CC} \le 1.30$		V _{CC} -0.1		V _{CC} -0.1		
		$1.40 \le V_{CC} \le 1.60$	1. 100	V _{CC} -0.2		V _{CC} -0.2		
		$1.65 \le V_{CC} \le 1.95$	- I _{OH} =-100μA	V _{CC} -0.2		V _{CC} -0.2		
		$2.30 \leq V_{CC} \leq 2.70$		V _{CC} -0.2		V _{CC} -0.2		
		$2.70 \leq V_{CC} \leq 3.60$		V _{CC} -0.2		V _{CC} -0.2		
		$1.10 \le V_{CC} \le 1.30$	I _{OH} =-2mA	.75 x V _{CC}		.75 x V _{CC}		
V_{OH}	HIGH Level Output Voltage	$1.40 \le V_{CC} \le 1.60$	I _{OH} =-4mA	.75 x V _{CC}		.75 x V _{CC}		V
	Vollago	$1.65 \leq V_{CC} \leq 1.95$	l – 6mΛ	1.25		1.25		
		$2.30 \leq V_{CC} \leq 2.70$	I _{OH} =-6mA	2.00		2.00		
		$2.30 \leq V_{CC} \leq 2.70$	1 12m A	1.8		1.8		
		2.70≤ V _{CC} ≤ 3.60	I _{OH} =-12mA	2.2		2.2		
		$2.30 \leq V_{CC} \leq 2.70$	1 40m A	1.7		1.7		
		$2.70 \leq V_{CC} \leq 3.60$	I _{OH} =-18mA	2.4		2.4		
		$2.70 \leq V_{CC} \leq 3.60$	I _{OH} =-24mA	2.2		2.2		

Continued on following page...

DC Electrical Characteristics (Continued)

0	Barrantan	.,	O a sa distinua	T _A =2	25°C	T _A =-40	to 85°C	11
Symbol	Parameter	V _{CC}	Conditions	Min.	Max.	Min.	Max.	Units
		0.90			0.1		0.1	
		$1.10 \le V_{CC} \le 1.30$			0.1		0.1	
		$1.40 \le V_{CC} \le 1.60$	Ι _{ΟL} =100μΑ		0.2		0.2	
		$1.65 \leq V_{CC} \leq 1.95$	10L=100μA		0.2		0.2	
		$2.30 \leq V_{CC} \leq 2.70$			0.2		0.2	
		$2.70 \leq V_{CC} \leq 3.60$			0.2		0.2	
Vol	LOW Level	$1.10 \le V_{CC} \le 1.30$	I _{OL} =2mA		0.25 x V _{CC}		0.25 x V _{CC}	V
VOL	Output Voltage	$1.40 \le V_{CC} \le 1.60$	I _{OL} =4mA		0.25 x V _{CC}		0.25 x V _{CC}	V
		$1.65 \le V_{CC} \le 1.95$	I _{OL} =6mA		0.3		0.3	
		$2.30 \leq V_{CC} \leq 2.70$	I _{OI} =12mA		0.4		0.4	
		$2.70 \leq V_{CC} \leq 3.60$	I _{OL} =12IIIA		0.4		0.4	
		2.30≤ V _{CC} ≤ 2.70	I _{OL} =18mA		0.6		0.6	
		$2.70 \leq V_{CC} \leq 3.60$	IOL=IOIIIA		0.4		0.4	
		$2.70 \leq V_{CC} \leq 3.60$	I _{OL} =24mA		0.55		0.55	
I _{IN}	Input Leakage Current	0.90 to 3.60	$0 \leq V_{\text{IN}} \leq 3.60$		±0.1		±0.5	μA
l _{OFF}	Power Off Leakage Current	0	$0 \leq \left(V_{IN}, v_O\right) \leq 3.60$		0.5		0.5	μΑ
la.	Quiescent	0.90 to 3.60	V _{IN} =V _{CC} , or GND		0.9		0.9	
Icc	Supply Current	0.90 10 3.60	$V_{CC} \leq V_{IN} \leq 3.6 V$				±0.9	μA

AC Electrical Characteristics

Cumala al	Davamatar	W	Canditions		T _A =25°	С	T _A =-40	to 85°C	l lusite	Figure
Symbol	Parameter	V _{cc}	Conditions	Min.	Тур.	Max.	Min.	Max.	Units	Figure
		0.90	$C_L=15pF, R_L=1M\Omega$		13					
		$1.10 \le V_{CC} \le 1.30$	C 15°E D 2kO	3.0	6.0	9.9	1.0	14.6	y.	
	Propagation	$1.40 \le V_{CC} \le 1.60$	$C_L=15pF, R_L=2k\Omega$	1.0	3.2	6.0	1.0	7.2	200	Figure 5
t _{PHL} , t _{PLH}	Delay	Delay 1.65 ≤ V _{CC} ≤ 1.95		1.0	2.0 4.5 1.0 5.3	ns	Figure 6			
		$2.30 \leq V_{CC} \leq 2.70$	C_L =30pF, R_L =500 Ω	0.8	1.2	2.6	0.7	3.7	/	
		$2.70 \leq V_{CC} \leq 3.60$		0.7	1.0	2.3	0.6 3.0			
C _{IN}	Input Capacitance	0			2				pF	5
C _{PD}	Power Dissipation Capacitance	0.90 to 3.60	V _{IN} =0V or V _{CC} , f=10MHz		8				pF	

AC Loadings and Waveforms

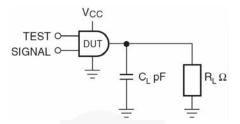


Figure 5. AC Test Circuit

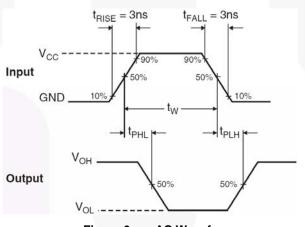


Figure 6. AC Waveforms

Symbol		V _{cc}								
Symbol	3.3V ± 0.3V 2.5V ± 0.2V 1.8V ± 0.15V 1.5V ± 0.1V 1.2V ± 0.1V									
V _{mi}	1.5V	V _{CC} /2								
V_{mo}	1.5V	V _{cc} /2								

Physical Dimensions

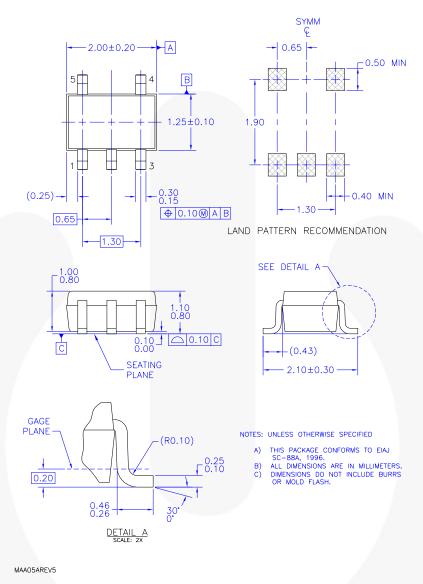


Figure 7. 5-Lead, SC70, EIAJ SC-88a, 1.25mm Wide

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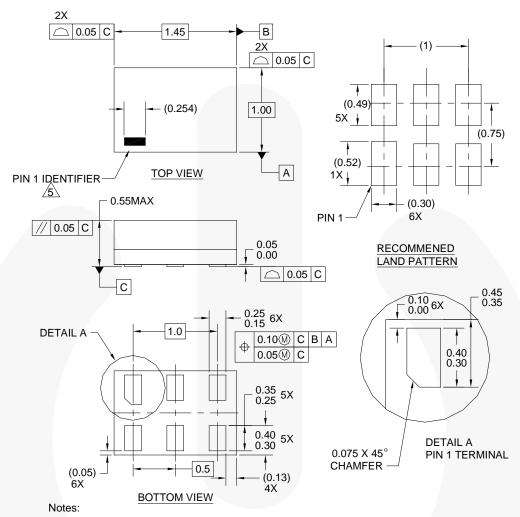
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Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/products/analog/pdf/sc70-5 tr.pdf.

Package Designator	Package Designator Tape Section		Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
P5X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



- 1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994
- 4. FILENAME AND REVISION: MAC06AREV4
- 5 PIN ONE IDENTIFIER IS 2X LENGTH OF ANY

OTHER LINE IN THE MARK CODE LAYOUT.

Figure 8. 6-Lead, MicroPak™, 1.0mm Wide

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Tape and Reel Specification

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Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
L6X	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions

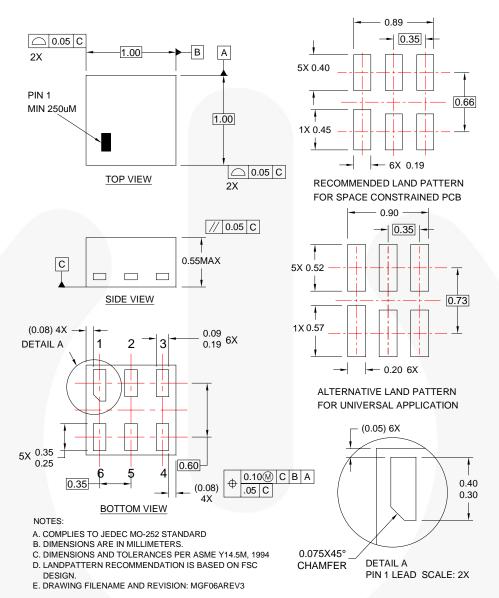


Figure 9. 6-Lead, MicroPak2, 1x1mm Body, .35mm Pitch

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Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/packaging/MicroPAK2 6L tr.pdf.

Package Designator Tape Section		Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
FHX	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed





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SPM®
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SuperFET®
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SuperSOT™.6
SuperSOT™.8
SupreMOS®
SyncFET™
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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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