

N-channel 650 V, 0.215 Ω typ., 12.5 A MDmesh™ V Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data

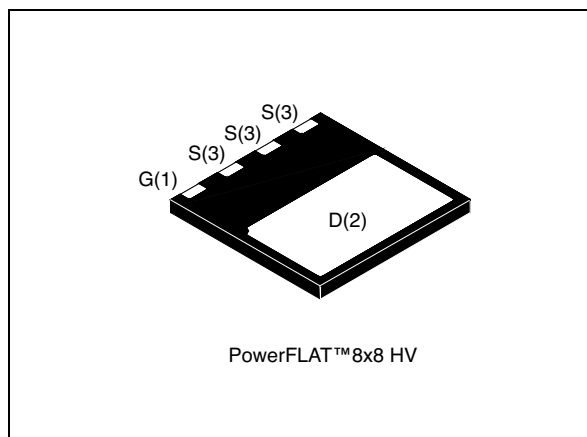
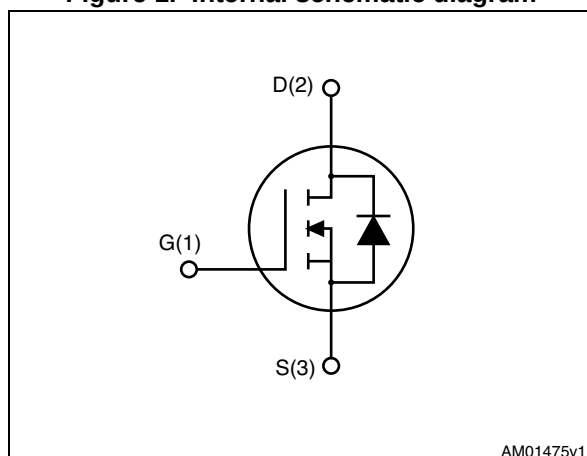


Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)max.}$	I_D
STL19N65M5	710 V	0.240 Ω	12.5 A ⁽¹⁾

1. The value is rated according to $R_{thj-case}$ and limited by package.

- Worldwide best $R_{DS(on)}$ * area
- Higher V_{DSS} rating and high dv/dt capability
- Excellent switching performance

Applications

- Switching applications

Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL19N65M5	19N65M5	PowerFLAT™ 8x8 HV	Tape and reel

Contents

1 **Electrical ratings** **3**

2 **Electrical characteristics** **4**

 2.1 **Electrical characteristics (curves)** **6**

3 **Test circuits** **9**

4 **Package mechanical data** **10**

5 **Packaging mechanical data** **14**

6 **Revision history** **16**



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	12.5	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	8.3	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	50	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 25\text{ °C}$	2.3	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 100\text{ °C}$	1.5	A
$P_{TOT}^{(3)}$	Total dissipation at $T_{amb} = 25\text{ °C}$	2.8	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ °C}$	90	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	210	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. The value is rated according to $R_{thj-case}$ and limited by package.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of inch², 2oz Cu
4. $I_{SD} \leq 12.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{Peak} \leq V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.39	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb max	45	°C/W

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 7.5\text{ A}$		0.215	0.240	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	1240	-	pF
C_{oss}	Output capacitance		-	32	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0,$ $V_{DS} = 0\text{ to }80\% V_{(BR)DSS}$	-	30	-	pF
$C_{o(tr)}^{(2)}$	Equivalent capacitance time related		-	99	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	3	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 7.5\text{ A},$ $V_{GS} = 10\text{ V}$ (see Figure 16)	-	31	-	nC
Q_{gs}	Gate-source charge		-	8	-	nC
Q_{gd}	Gate-drain charge		-	14	-	nC

1. $C_{oss\text{ eq.}}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. $C_{oss\text{ eq.}}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 9.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17 and 20)	-	36	-	ns
$t_{r(v)}$	Voltage rise time		-	7	-	ns
$t_{f(i)}$	Current fall time		-	9	-	ns
$t_{c(off)}$	Crossing time		-	11	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		12.5	A
$I_{SDM}^{(1),(2)}$	Source-drain current (pulsed)		-		50	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 15\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 15\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 17)	-	290		ns
Q_{rr}	Reverse recovery charge		-	3.4		μC
I_{RRM}	Reverse recovery current		-	23.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 15\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17)	-	352		ns
Q_{rr}	Reverse recovery charge		-	4		μC
I_{RRM}	Reverse recovery current		-	24		A

1. The value is rated according to $R_{thj-case}$ and limited by package.
2. Pulse width limited by safe operating area
3. Pulsed: pulse duration = $300\ \mu\text{s}$, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

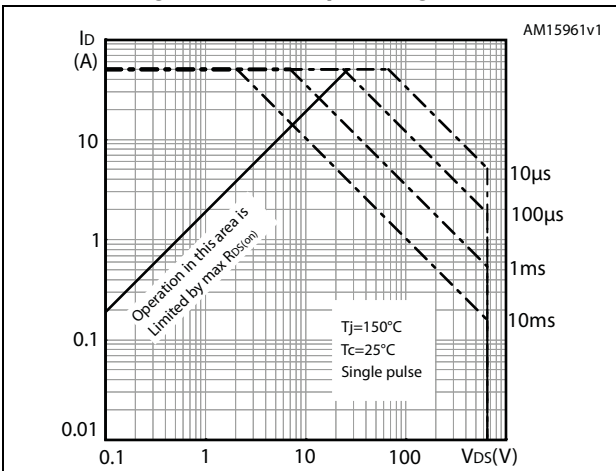


Figure 3. Thermal impedance

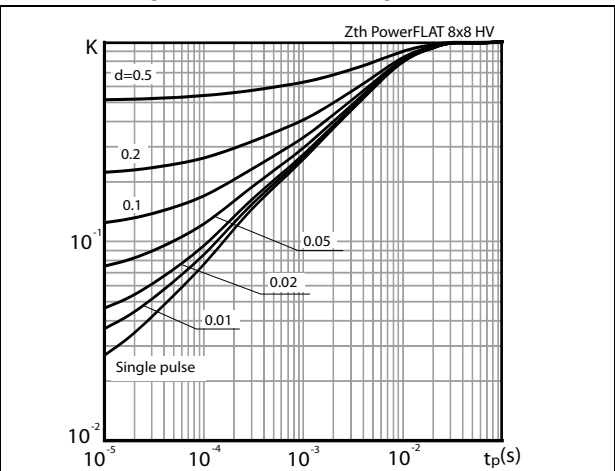


Figure 4. Output characteristics

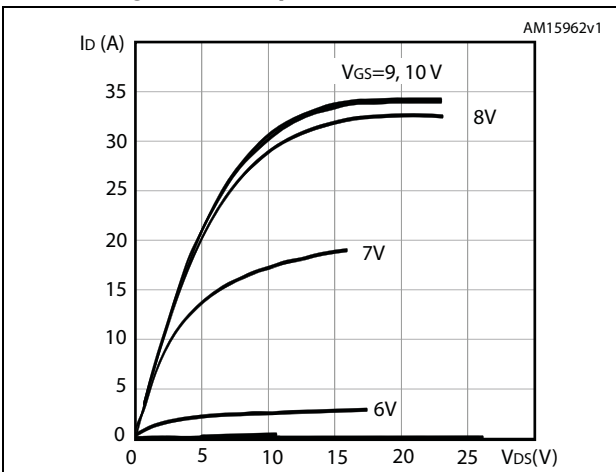


Figure 5. Transfer characteristics

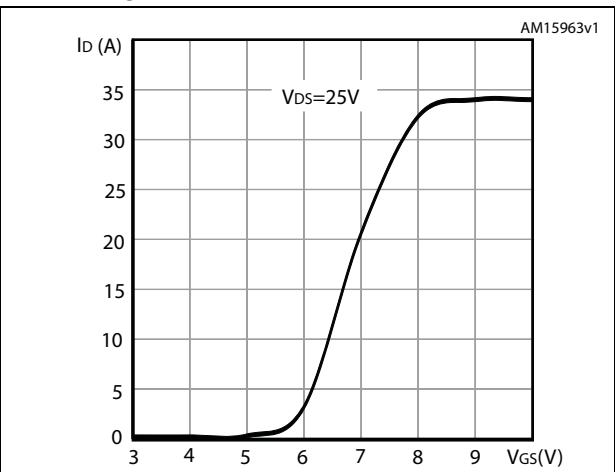


Figure 6. Gate charge vs gate-source voltage

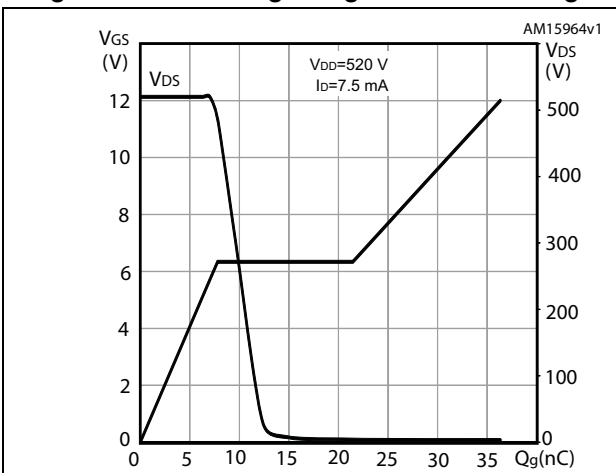


Figure 7. Static drain-source on-resistance

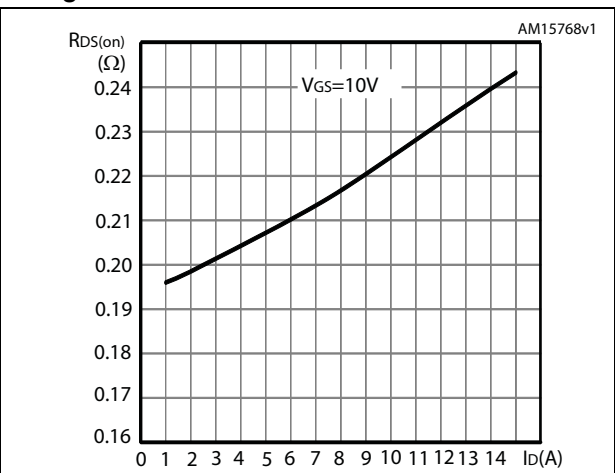


Figure 8. Capacitance variations

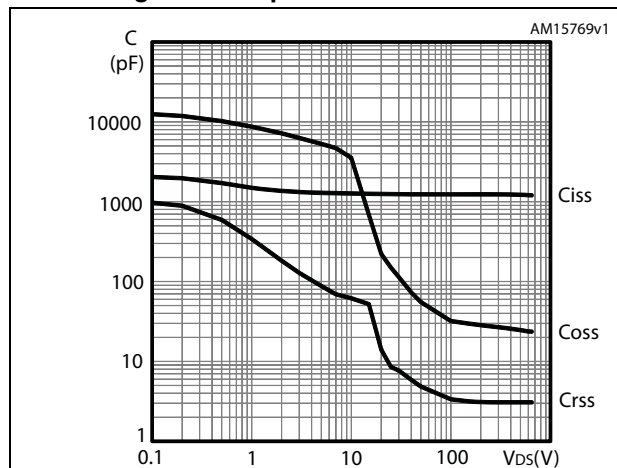


Figure 9. Output capacitance stored energy

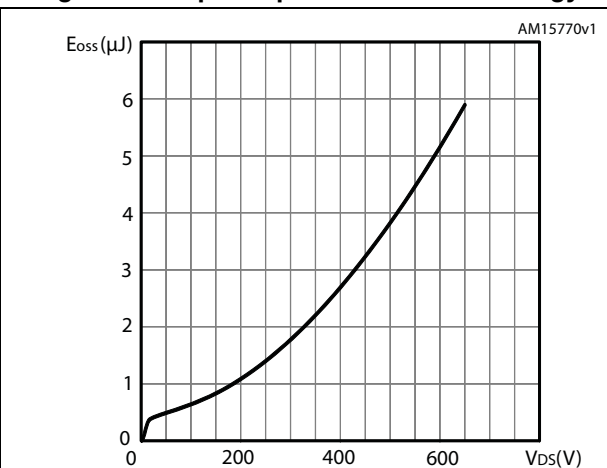


Figure 10. Normalized gate threshold voltage vs. temperature

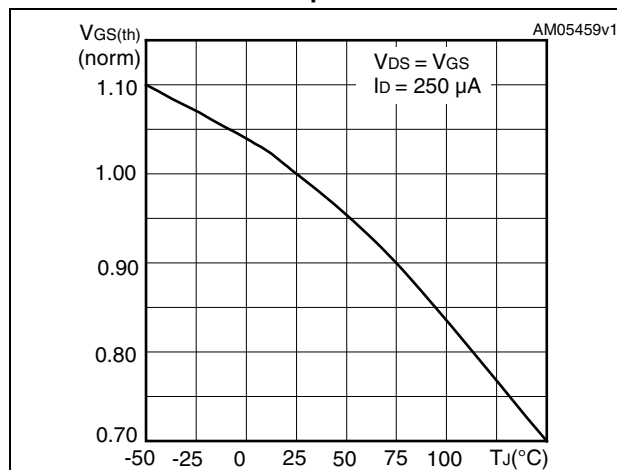


Figure 11. Normalized on-resistance vs. temperature

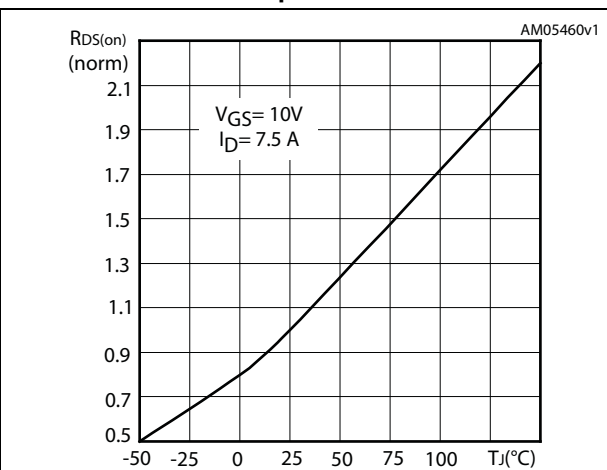


Figure 12. Drain-source diode forward characteristics

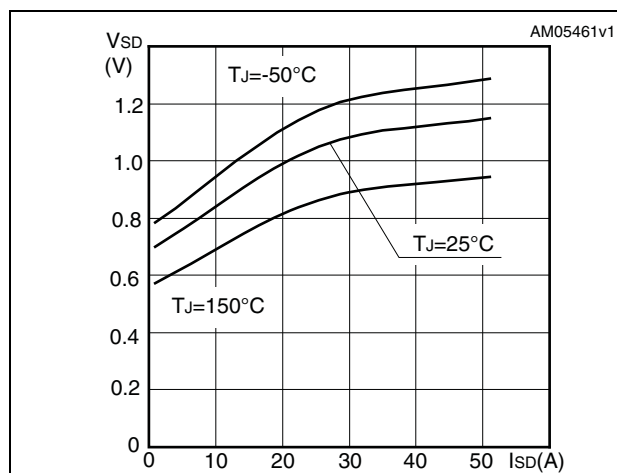


Figure 13. Normalized VDS vs. temperature

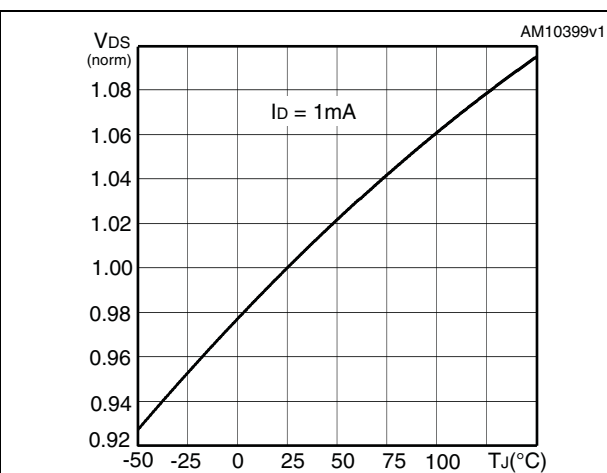
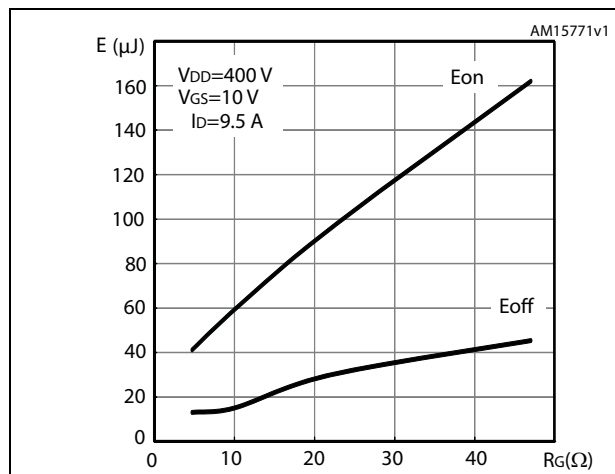


Figure 14. Switching losses vs gate resistance ⁽¹⁾



1. E_{on} including reverse recovery of a SiC diode

3 Test circuits

Figure 15. Switching times test circuit for resistive load

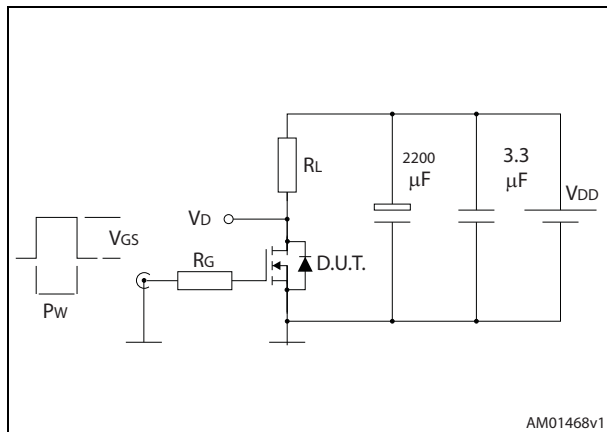


Figure 16. Gate charge test circuit

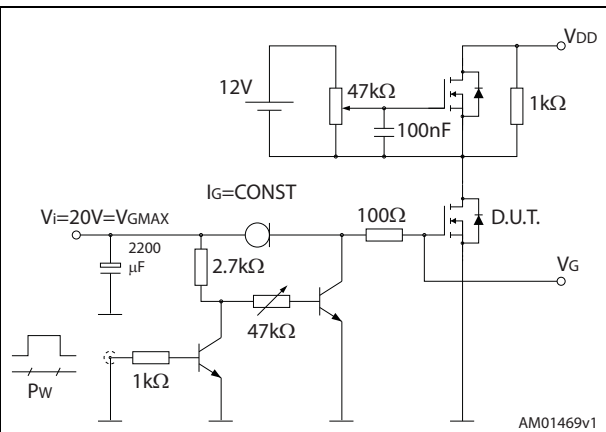


Figure 17. Test circuit for inductive load switching and diode recovery times

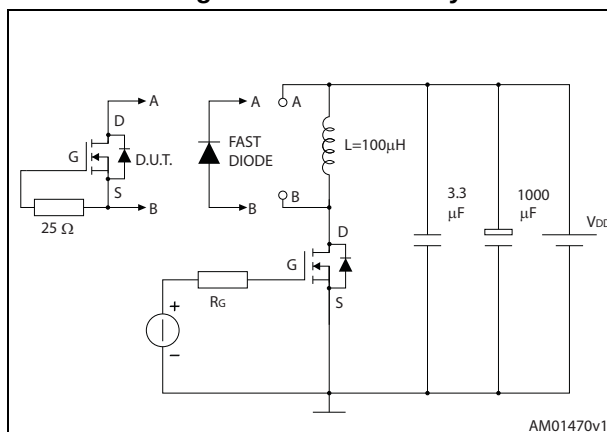


Figure 18. Unclamped inductive load test circuit

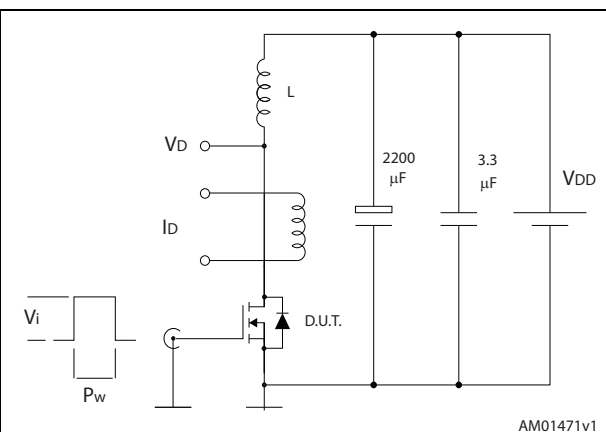


Figure 19. Unclamped inductive waveform

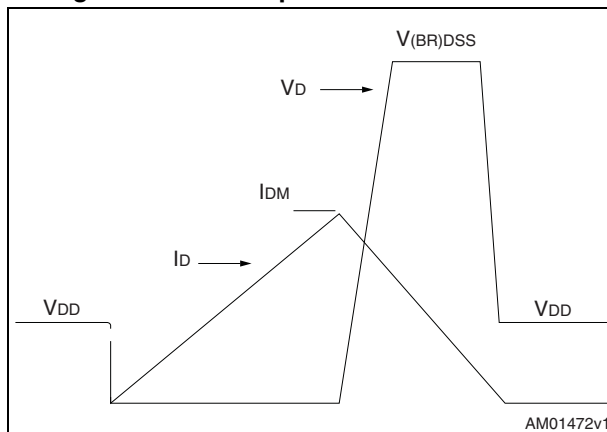
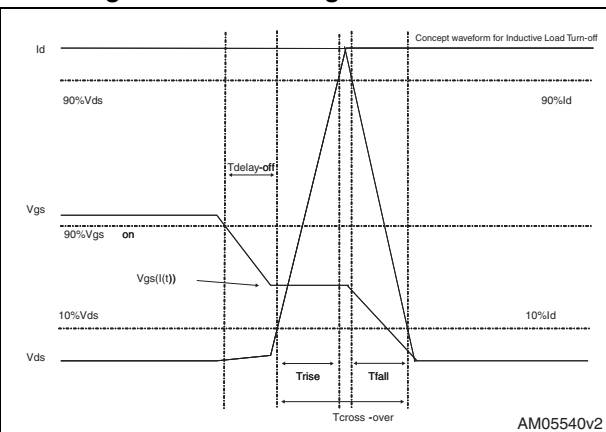


Figure 20. Switching time waveform



4 Package mechanical data

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Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 21. PowerFLAT™ 8x8 HV drawing mechanical data

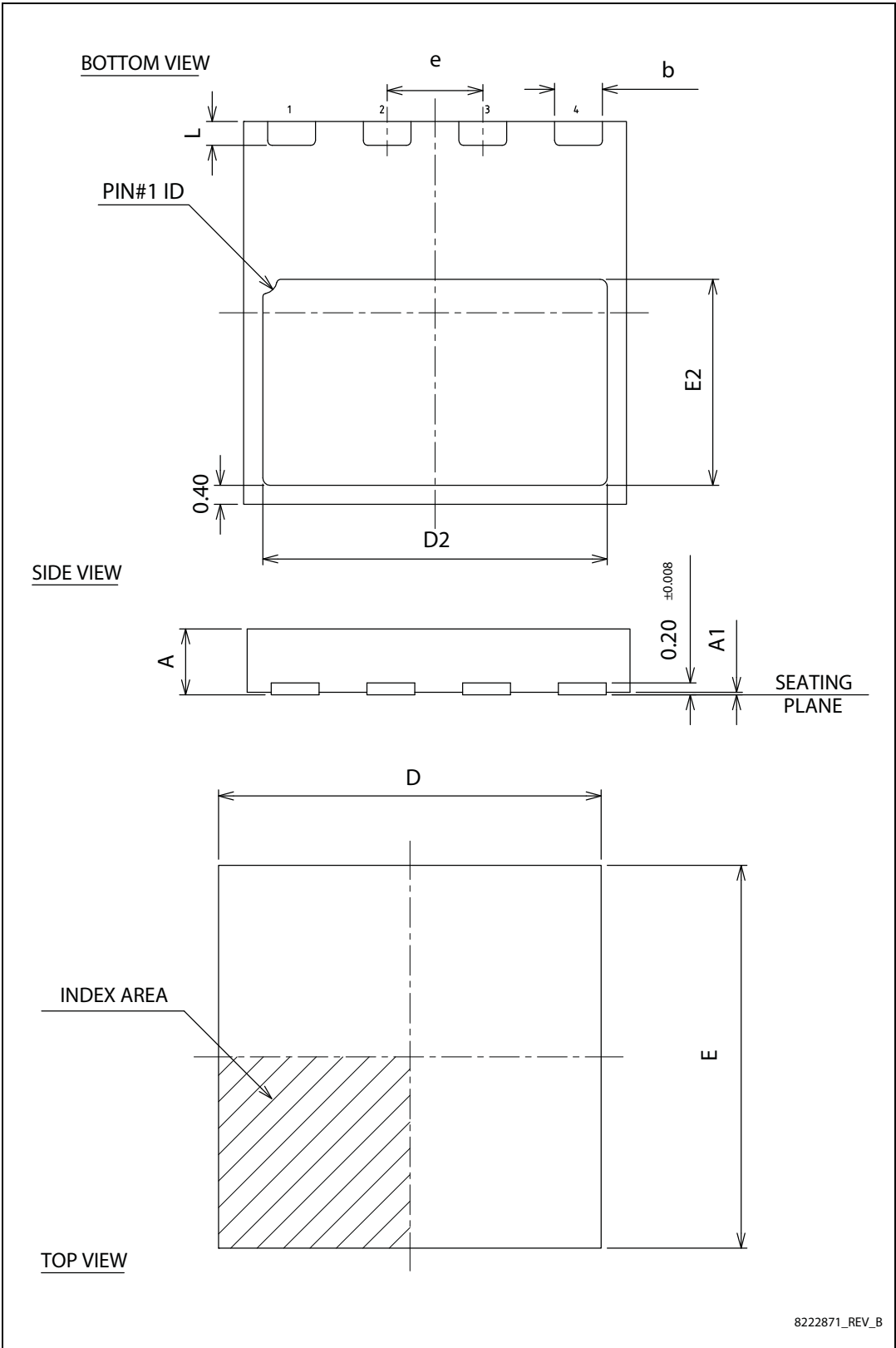
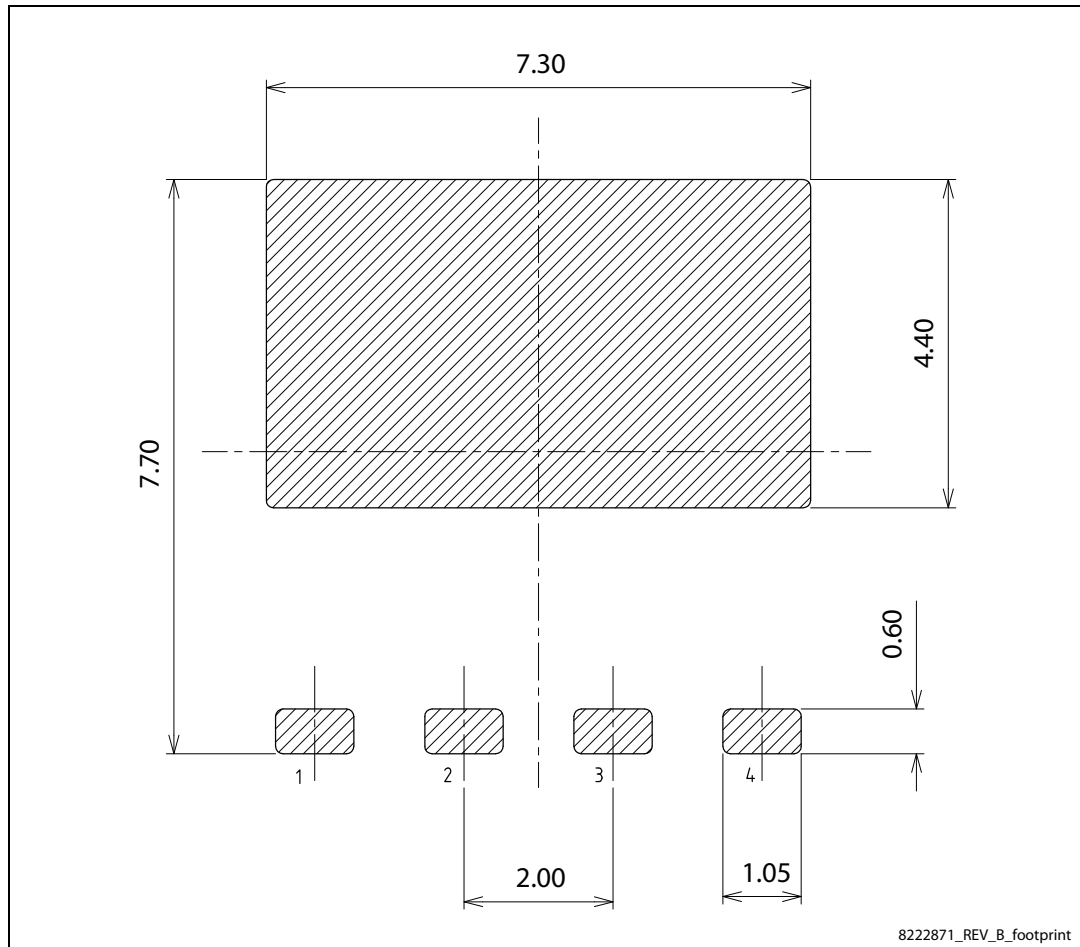


Figure 22. PowerFLAT™ 8x8 HV recommended footprint (dimension in millimeters)



5 Packaging mechanical data

Figure 23. PowerFLAT™ 8x8 HV tape (dimension in millimeters)

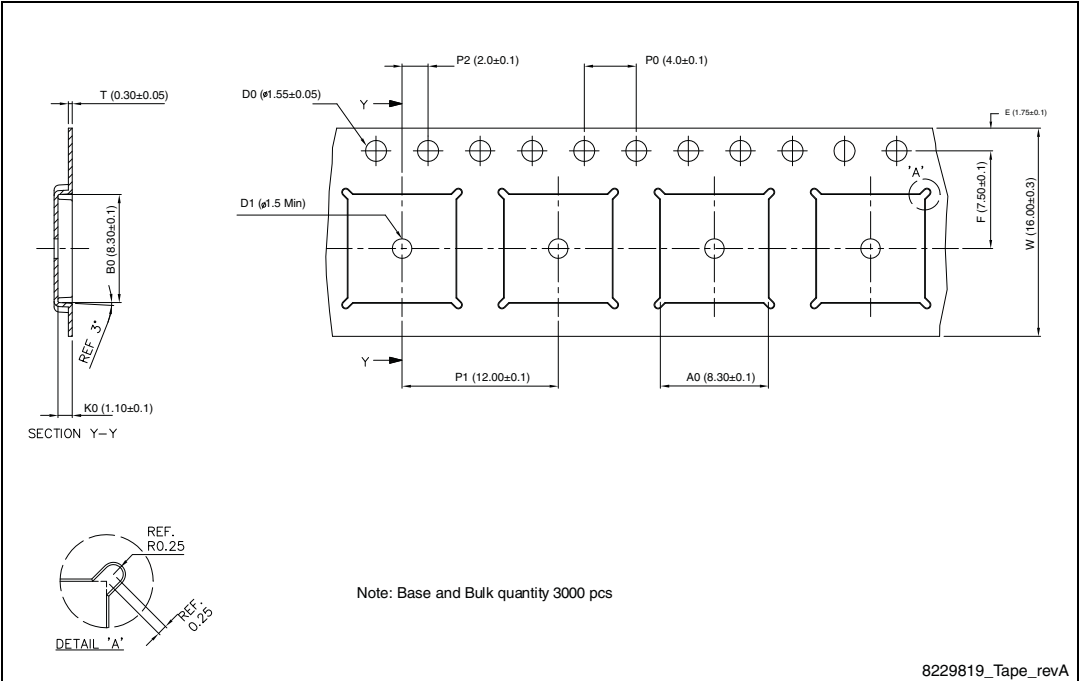


Figure 24. PowerFLAT™ 8x8 HV package orientation in carrier tape

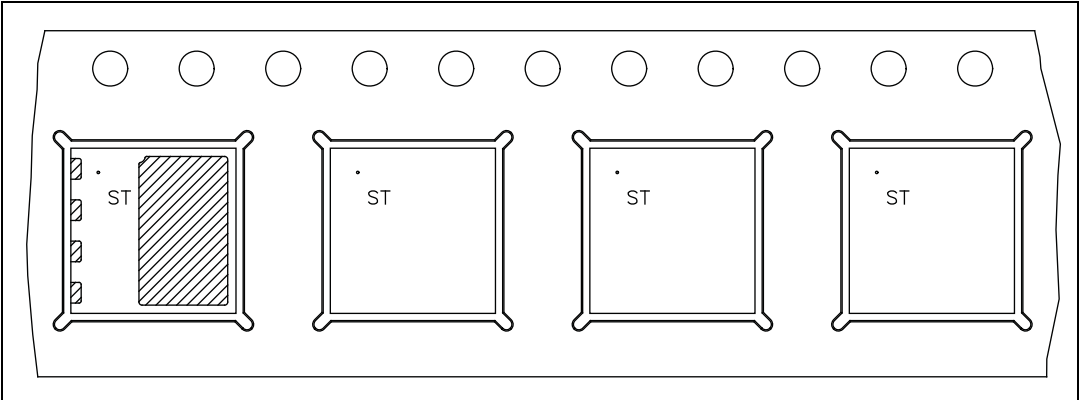
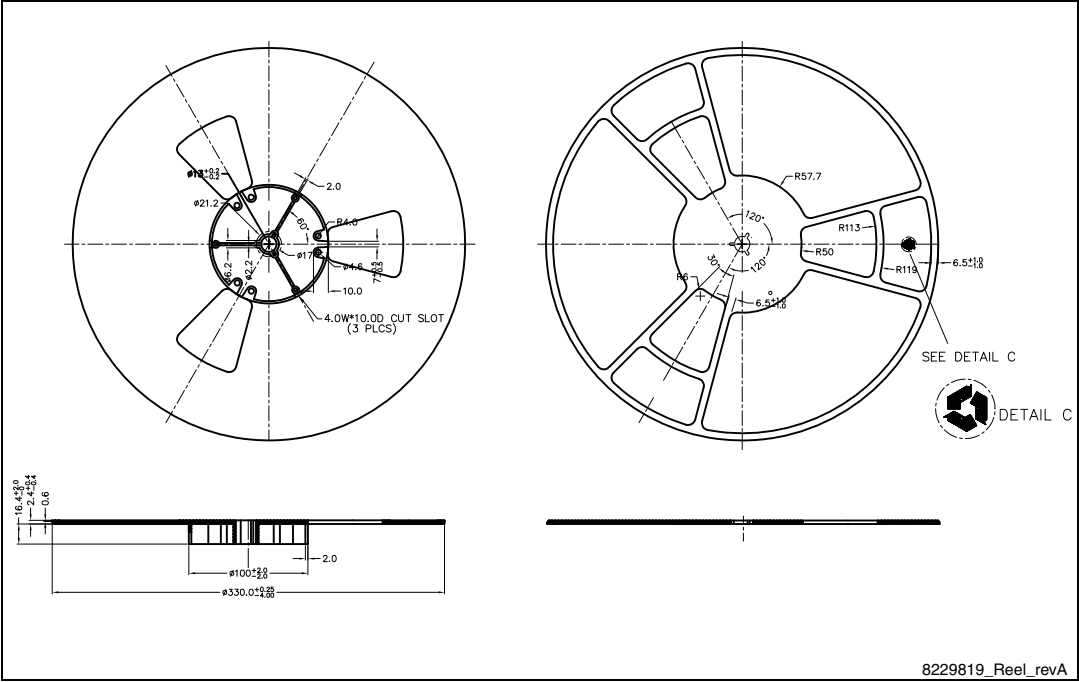


Figure 25. PowerFLAT™ 8x8 HV reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
17-Jul-2013	1	First release

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