

ISOFACE™

ISO1H815G

Galvanic Isolated 8 Channel High-Side Switch

Datasheet

Revision 2.2, 2013-01-31

Power Management & Multimarket

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| Revision History | | | | | | | |
|---|--|--|--|--|--|--|--|
| Page or Item Subjects (major changes since previous revision) | | | | | | | |
| Revision 2.2, 2 | 013-01-31 | | | | | | |
| Page 12 | Page 12 table 4.1 Extended operating temperature added | | | | | | |
| Revision 2.1 | | | | | | | |
| Page 16 | Page 16 table 4.8 updated | | | | | | |
| Revision 2.0 | | | | | | | |
| all | Final Datasheet | | | | | | |

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ISOFACE™

ISO1H815G

Coreless Transformer Isolated Digital Output 8 Channel 0.625 A High-Side Switch

Product Highlights

- Coreless transformer isolated data interface
- Galvanic isolation
- 8 High-side output switches 1,2A
- μC compatible 8-bit parallel peripheral



Features

- Interface 3.3/5V CMOS operation compatible
- Parallel interface
- Direct control mode
- High common mode transient immunity
- Short circuit protection
- · Maximum current internally limited
- Overload protection
- Overvoltage protection (including load dump)
- Undervoltage shutdown with autorestart and hysteresis
- Switching inductive loads
- · Common output disable pin
- · Thermal shutdown with restart
- Thermal independence of separate channels
- Common diagnostic output for overtemperature
- ESD protection
- Loss of GNDbb and loss of V_{bb} protection
- Reverse Output Voltage protection
- · Isolated return path for DIAG signal
- RoHS compliant

Typical Application

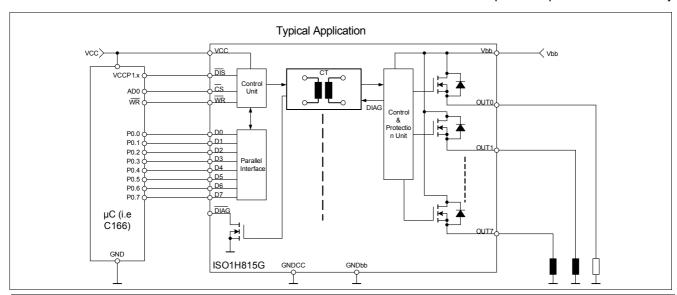
- Isolated switch for industrial applications (PLC)
- All types of resistive, inductive and capacitive loads
- µC compatible power switch for 24V DC applications
- Driver for solenoid, relays and resistive loads

Description

The ISO1H815G is a galvanically isolated 8 bit data interface in PG-DSO-36 package that provides 8 fully protected high-side power switches that are able to handle currents up to 1.2A.

An 8 bit parallel μC compatible interface allows to connect the IC directly to a μC system. The input interface supports also a direct control mode and is designed to operate with 3.3/5V CMOS compatible levels.

The data transfer from input to output side is realized by



| Туре | On-state Resistance | Package |
|-----------|---------------------|----------|
| ISO1H815G | 200mΩ | PG-DSO36 |

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Pin Configuration and Functionality

1 Pin Configuration and Functionality

1.1 Pin Configuration

| 1.1 | FIII | Comiguration |
|-----|--------|--|
| Pin | Symbol | Function |
| 1 | N.C. | Not connected |
| 2 | VCC | Positive 3.3/5V logic supply |
| 3 | DIS | Output disable |
| 4 | CS | Chip select |
| 5 | WR | Parallel write |
| 6 | D0 | Data input bit0 |
| 7 | D1 | Data input bit1 |
| 8 | D2 | Data input bit2 |
| 9 | D3 | Data input bit3 |
| 10 | D4 | Data input bit4 |
| 11 | D5 | Data input bit5 |
| 12 | D6 | Data input bit6 |
| 13 | D7 | Data input bit7 |
| 14 | DIAG | Common diagnostic output for overtemperature |
| 15 | GNDCC | Input logic ground |
| 16 | N.C. | Not connected |
| 17 | N.C. | Not connected |
| 18 | N.C. | Not connected |
| 19 | GNDbb | Output driver ground |
| 20 | N.C | Not connected |
| 21 | OUT7 | High-side output of channel 7 |
| 22 | OUT7 | High-side output of channel 7 |
| 23 | OUT6 | High-side output of channel 6 |
| 24 | OUT6 | High-side output of channel 6 |
| 25 | OUT5 | High-side output of channel 5 |
| 26 | OUT5 | High-side output of channel 5 |
| 27 | OUT4 | High-side output of channel 4 |
| 28 | OUT4 | High-side output of channel 4 |
| 29 | OUT3 | High-side output of channel 3 |
| 30 | OUT3 | High-side output of channel 3 |
| 31 | OUT2 | High-side output of channel 2 |
| 32 | OUT2 | High-side output of channel 2 |
| 33 | OUT1 | High-side output of channel 1 |
| 34 | OUT1 | High-side output of channel 1 |
| 35 | OUT0 | High-side output of channel 0 |
| 36 | OUT0 | High-side output of channel 0 |
| TAB | Vbb | Positive driver power supply voltage |

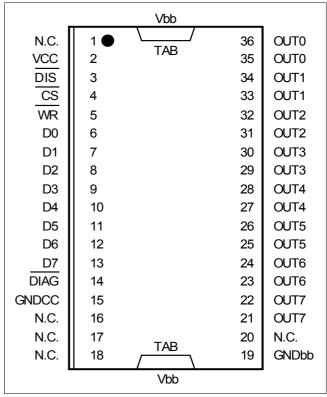


Figure 1 Power SO-36 (430mil)

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Pin Configuration and Functionality

1.2 Pin Functionality

VCC (Positive 3.3/5V logic supply)

The VCC supplies the input interface that is galvanically isolated from the output driver stage. The input interface can be supplied with 3.3/5V.

DIS (Output disable)

The high-side outputs OUT0...OUT7 can be immediately switched off by means of the low active pin $\overline{\text{DIS}}$ that is an asynchronous signal. The input registers are also reset by the $\overline{\text{DIS}}$ signal. The Output remains switched off after low-high transition of $\overline{\text{DIS}}$ signal, till new information is written into the input register. Current Sink to GNDCC.

CS (Chip select)

The system microcontroller selects the ISO1H815G by means of the low active pin \overline{CS} to activate the parallel interface. By connecting the \overline{CS} pin and \overline{WR} pin to ground the parallel direct control is activated. Current Source to VCC.

WR (Parallel write)

In parallel mode data at the input pins (D0 ... D7) are latched by means of the rising edge of the low active signal \overline{WR} (write). Current Source to VCC.

D0 ... D7 (Data input bit0 ... bit7)

The present data can be latched on the rising edge of the write signal WR. D0 ... D7 control the corresponding output channels OUT0 ...OUT7. By connecting CS and WR to ground, the signals at D0 ... D7 directly control the outputs. Current Sink to GNDCC.

DIAG (Common diagnostic output for overtemperature)

The low active $\overline{\text{DIAG}}$ signal contains the OR-wired information of the separated overtemperature detection units for each channel. The output pin $\overline{\text{DIAG}}$ provides an open drain functionality. A current source is also connected to the pin $\overline{\text{DIAG}}$. In normal operation the signal $\overline{\text{DIAG}}$ is high. When overtemperature or Vbb below ON-Limit is detected the signal $\overline{\text{DIAG}}$ changes to low.

GNDCC (Ground for VCC domain)

This pin acts as the ground reference for the input interface that is supplied by VCC.

GNDbb (Output driver ground domain)

This pin acts as the ground reference for the output

driver that is supplied by Vbb.

OUT0 ... OUT7 (High side output channel 0 ... 7)

The output high side channels are internally connected to Vbb and controlled by the corresponding data input pins D0 ... D7 in parallel mode.

TAB (Vbb, Positive supply for output driver)

The heatslug is connected to the positive supply port of the output interface.



Blockdiagram

Blockdiagram 2

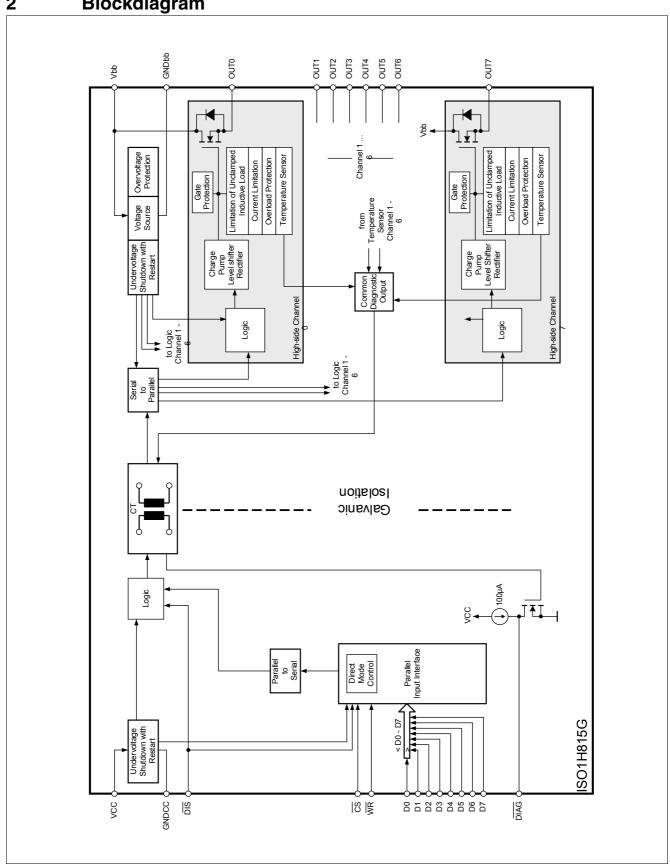


Figure 2 **Blockdiagram**



3 Functional Description

3.1 Introduction

The ISOFACE ISO1H815G includes 8 high-side power switches that are controlled by means of the integrated parallel interface. The interface is 8bit µC compatible. Furthermore a direct control mode can be selected that allows the direct control of the outputs OUT0...OUT7 by means of the inputs D0...D7 without any additional logic signal. The IC can replace 8 optocouplers and the 8 high-side switches in conventional I/O-Applications as a galvanic isolation is implemented by means of the integrated coreless transformer technology. The µC compatible interfaces allow a direct connection to the ports of a microcontroller without the need for other components. Each of the 8 high-side power switches is protected against short to Vbb, overload, overtemperature and against overvoltage by an active zener clamp.

The diagnostic logic on the power chip recognizes the overtemperature information of each power transistor. The information is send via the internal coreless transformer to the pin $\overline{\text{DIAG}}$ at the input interface.

3.2 Power Supply

The IC contains 2 galvanic isolated voltage domains that are independent from each other. The input interface is supplied at VCC and the output stage is supplied at Vbb. The different voltage domains can be switched on at different time. The output stage is only enabled once the input stage enters a stable state.

3.3 Output Stage

Each channel contains a high-side vertical power FET that is protected by embedded protection functions.

The continuous current for each channel is 1.2A (all channels ON).

3.3.1 Output Stage Control

Each output is independently controlled by an output latch and a common reset line via the pin $\overline{\text{DIS}}$ that disables all eight outputs and reset the latches. The parallel input data is transferred to the input latches with a high-to-low transition of the signal $\overline{\text{WR}}$ (write) while the $\overline{\text{CS}}$ is logic low. A low-to-high transition of $\overline{\text{CS}}$ transfers then the data of the input latches to the output buffer.

3.3.2 Power Transistor Overvoltage Protection

Each of the eight output stages has it own zener clamp that causes a voltage limitation at the power transistor when solenoid loads are switched off. V_{ON} is then clamped to 47V (min.).

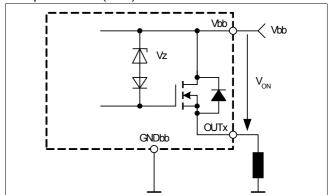


Figure 3 Inductive and overvoltage output clamp (each channel)

Energy is stored in the load inductance during an inductive load switch-off.

$$E_L = 1/2 \times L \times I_L^2$$

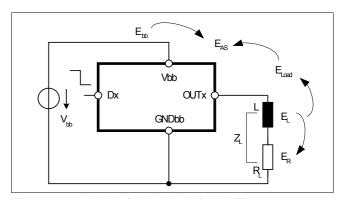


Figure 4 Inductive load switch-off energy dissipation (each channel)

While demagnetizing the load inductance, the energy dissipation in the DMOS is

$$E_{AS} = E_{bb} + E_L - E_R = V_{ON(CL)} \times i_L(t)dt$$

with an approximate solution for $R_L > 0\Omega$:

$$\mathbf{E}_{\mathrm{AS}} = \frac{\mathbf{I}_{\mathrm{L}} \times \mathbf{L}}{2 \times \mathbf{R}_{\mathrm{L}}} \times (\mathbf{V}_{\mathrm{bb}} + \left| \mathbf{V}_{\mathrm{ON(CL)}} \right|) \times \ln \left(1 + \frac{\mathbf{I}_{\mathrm{L}} \times \mathbf{R}_{\mathrm{L}}}{\left| \mathbf{V}_{\mathrm{ON(CL)}} \right|} \right)$$



3.3.3 Power Transistor Overcurrent Protection

The outputs are provided with a current limitation that enters a repetitive switched mode after an initial peak current has been exceeded. The initial peak short circuit current limit is set to $I_{L(SCp)}.$ During the repetitive mode short circuit current the limit is set to $I_{L(SCr)}.$ If this operation leads to an overtemperature condition, a second protection level ($T_{\rm j} > 135^{\circ} C)$ will change the output into a low duty cycle PWM (selective thermal shutdown with restart) to prevent critical chip temperatures.

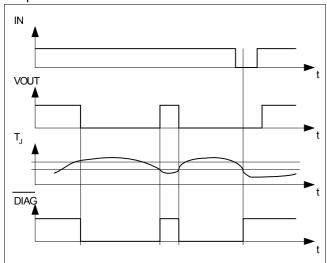


Figure 5 Overtemperature detection

The following figures show the timing for a turn on into short circuit and a short circuit in on-state. Heating up of the chip may require several milliseconds, depending on external conditions.

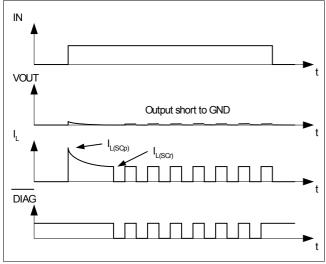


Figure 6 Turn on into short circuit, shut down by overtemperature, restart by cooling

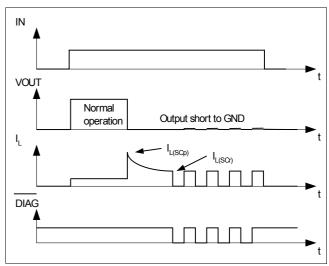


Figure 7 Short circuit in on-state, shut down down by overtemperature, restart by cooling

3.4 Common Diagnostic Output

The overtemperature detection information are OR-wired in the common diagnostic output block. The information is send via the integrated coreless transformer to the input interface. The output stage at pin DIAG has an open drain functionality combined with a current source.

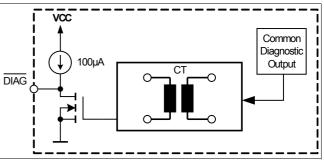


Figure 8 Common diagnostic output



3.5 Parallel Interface

The ISO1H815G contains a parallel interface that can be directly controlled by the microcontroller output ports. The parallel interface can also be switched over to a direct control that allows direct changes of the outputs OUT0 ... OUT7 by means of the corresponding inputs D0 ... D7 without additional logic signals. To activate the parallel direct control mode pin $\overline{\text{CS}}$ and pin $\overline{\text{WR}}$ have to be connected both to ground.

3.5.1 Parallel Interface Signal Description

 $\overline{\text{CS}}$ - Chip select. The system microcontroller selects the ISO1H815G by means of the $\overline{\text{CS}}$ pin. Whenever the pin is in a logic low state, data can be transferred from the μC .

CS High to low transition:

Parallel input data can be written in from then on

CS Low to high transition:

 The data in the input latches is transferred to the output buffer

 $\overline{\text{WR}}$ - Write. The system controller enables the write procedure in the ISO1H815G by means of the signal $\overline{\text{WR}}$. A logic low state signal at pin $\overline{\text{WR}}$ writes the input data into the input latches when the $\overline{\text{CS}}$ pin is in a logic low state.

WR Logic low level:

 Parallel input data at the pins D0 - D7 is written into the input latches

WR Logic high level:

 The parallel input data is latched in the input latches. Any changes at the pins D0 - D7 after the low-to-high transition of WR do not affect the input latches.

D0 ... **D7** - Parallel input. Parallel data bits are fed into the pins D0 ... D7. The data is written into the input latches when \overline{WR} is logic low.

3.5.2 uC Control Mode

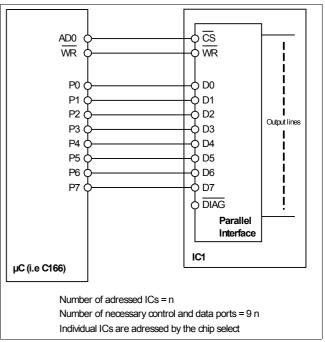


Figure 9 Parallel bus configuration

3.5.3 Direct Control Mode

Beside the use of the parallel μC compatible interface a parallel direct control mode can be choosen. In this mode the output OUT0...OUT7 can be directly controlled via the inputs D0...D7 without the need for additional logic signals. To activate this mode pin \overline{CS} and \overline{WR} need to be connected to ground.

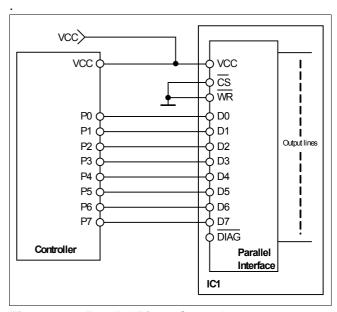


Figure 10 Parallel Direct Control



3.6 Parallel Interface Timing

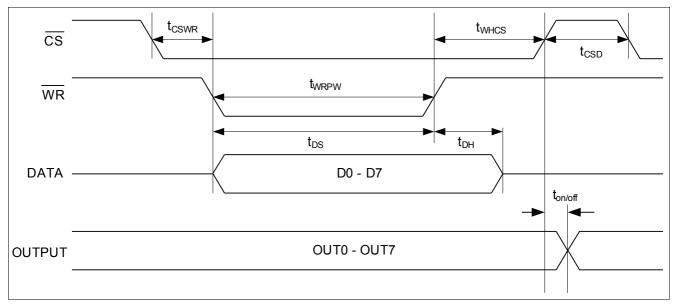


Figure 11 Parallel input - output timing diagram

3.7 Transmission Failure Detection

There is a failure detection unit integrated to ensure also a stable functionality during the integrated coreless transformer transmission. This unit decides wether the transmitted data is valid or not. If four times serial data coming in from the internal registers is not accepted, the output stages are switched off until the next valid data is received.



4 Electrical Characteristics

Note: All voltages at pins 2 to 14 are measured with respect to ground GNDCC (pin 15). All voltages at pin 20 to pin 36 and TAB are measured with respect to ground GNDbb (pin 19). The voltage levels are valid if other ratings are not violated. The two voltage domains V_{CC} and V_{bb} are internally galvanic isolated.

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 2 (VCC) and TAB (Vbb) is discharged before assembling the application circuit. Supply voltages higher than V_{bb(AZ)} require an external current limit for the GNDbb pin, e.g. with a 15Ω resistor in GNDbb connection. Operating at absolute maximum ratings can lead to a reduced lifetime.

| Parameter | Symbol | Limit | Unit | |
|--|-----------------------|------------------|------------------|----|
| at $T_j = -40 \dots 135$ °C, unless otherwise specified | | min. | max. | |
| Supply voltage input interface (VCC) | V _{CC} | -0.5 | 6.5 | ٧ |
| Supply voltage output interface (Vbb) | V_{bb} | -1 ¹⁾ | 45 | |
| Continuos voltage at data inputs (D0 D7) | V _{Dx} | -0.5 | 6.5 | |
| Continuos voltage at pin CS | V _{CS} | -0.5 | 6.5 | |
| Continuos voltage at pin WR | V_{WR} | -0.5 | 6.5 | |
| Continuos voltage at pin DIS | V_{DIS} | -0.5 | 6.5 | |
| Continuos voltage at pin DIAG | V_{DIAG} | -0.5 | 6.5 | |
| Load current (short-circuit current) | IL | | self limited | Α |
| Reverse current through GNDbb ¹⁾ | I _{GNDbb} | -1.6 | | |
| Operating Temperature | Tj | -25 | internal limited | °C |
| Extended Operation Temperature ²⁾ | T _j | -40 | internal limited | |
| Power Dissipation ³⁾ | P _{tot} | | 3.3 | W |
| Inductive load switch-off energy dissipation ⁴⁾ single pulse, $T_j = 125$ °C, $I_L = 1.2A$ one channel active all channel simultaneously active (each channel) | E _{AS} | _ | 5 0.5 | J |
| Load dump protection ³⁾ $V_{loadDump}^{5)}=V_A + V_S$ V_{IN} = low or high t_d = 400ms, R_I = 2 Ω , R_L = 27 Ω , V_A = 13.5V t_d = 350ms, R_I = 2 Ω , R_L = 57 Ω , V_A = 27V | V _{Loaddump} | | 90 117 | V |
| Electrostatic discharge voltage (Human Body Model) according to JESD22-A114-B | V _{ESD} | | 2 | kV |
| Electrostatic discharge voltage (Charge Device Model) according to ESD STM5.3.1 - 1999 | V _{ESD} | | 1 | kV |
| Continuos reverse drain current ¹⁾³⁾ , each channel | Is | _ | 4 | Α |
| | 1 | | 1 | |

- defined by P_{tot}
- 2) not subject to production test, slight deviation of electrical parameters possible.
- 3) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thick) copper area for drain connection. PCB is vertical without blown air.
- 4) not subject to production test, specified by design
- 5) $V_{Loaddump}$ is setup without the DUT connected to the generator per ISO7637-1 and DIN40839



4.2 Thermal Characteristics

| Parameter | Symbol Limit Values | | Symbol | Limit Values | | alues Ur | | Test Condition |
|--|---------------------|------|--------|--------------|-----|----------|--|-----------------------|
| at T_j = -25 125°C, V_{bb} =1530V, V_{CC} =3.05.5V, unless otherwise specified | | min. | typ. | max. | | | | |
| Thermal resistance junction - case | R_{thJC} | | | 1.5 | K/W | | | |
| Thermal resistance @ min. footprint | R _{th(JA)} | | | 50 | | | | |
| Thermal resistance @ 6cm² cooling area ¹⁾ | R _{th(JA)} | | | 38 | | | | |

¹⁾ Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70μm thick) copper area for drain connection. PCB is vertical without blown air.

4.3 Load Switching Capabilities and Characteristics

| Parameter | ameter Symbol Limit Values | | es | Unit | Test Condition | |
|--|----------------------------|------|------------------------|-------------------------|-----------------------|--|
| at $T_j = -25 \dots 125$ °C, $V_{bb}=15 \dots 30$ V, $V_{CC}=3.0 \dots 5.5$ V, unless otherwise specified | | min. | typ. | max. | | |
| On-state resistance, $I_L = 0.5A$, each channel $T_j = 25^{\circ}C$ $T_j = 125^{\circ}C$ two parallel channels, $T_j = 25^{\circ}C:^{1)}$ four parallel channels, $T_j = 25^{\circ}C:^{1)}$ | R _{ON} | _ | 150 270 75 38 | 200 320 100 50 | mΩ | |
| Nominal load current Device on PCB 38K/W, T_a = 85°C, T_j < 125°C one channel: ¹⁾ two parallel channels: ¹⁾ four parallel channels: ¹⁾ | I _{L(NOM)} | | 1.4 2.2 4.4 | | A | |
| Turn-on time to 90% $V_{OUT}^{2)}$ $R_L = 47\Omega$, $V_{Dx} = 0$ to 5V | t _{on} | | 64 | 120 | μs | |
| Turn-off time to 10% $V_{OUT}^{2)}$ $R_L = 47\Omega$, $V_{Dx} = 5$ to 0V | t _{off} | | 89 | 170 | | |
| Slew rate on 10 to 30% V_{OUT} $R_L = 47\Omega$, $V_{bb} = 15V$ | dV/dt _{on} | | 1 | 2 | V/µs | |
| Slew rate off 70 to 40% V_{OUT} $R_L = 47\Omega$, $V_{bb} = 15V$ | -dV/dt _{off} | | 1 | 2 | | |

¹⁾ not subject to production test, specified by design

4.4 Operating Parameters

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---------------------|--------------|------|------|-------|-------------------------|
| at $T_j = -25 \dots 125$ °C, $V_{bb}=15\dots 30V$, $V_{CC}=3.0\dots 5.5V$, unless otherwise specified | | min. | typ. | max. | | |
| Common mode transient immunity ¹⁾ | $\Delta V_{ISO}/dt$ | -25 | - | 25 | kV/μs | $\Delta V_{ISO} = 200V$ |
| Magnetic field immunity ¹⁾ | H _{IM} | 100 | | | A/m | IEC61000-4-8 |

²⁾ The turn-on and turn-off time includes the switching time of the high-side switch and the transmission time via the coreless transformer in normal operating mode. During a failure on the coreless transformer transmission turn-on or turn-off time can increase by up to 50µs.



| Voltage domain V _{bb} | Operating voltage | V_{bb} | 11 | _ | 35 | V | |
|--------------------------------|--|------------------------|-----|-----|------|----|------------------------------|
| (Output interface) | Undervoltage shutdown | V _{bb(under)} | 7 | | 10.5 | | |
| | Undervoltage restart | $V_{bb(u_rst)}$ | _ | | 11 | | |
| | Undervoltage hysteresis | $\Delta V_{bb(under)}$ | _ | 0.5 | | | |
| | Undervoltage current | I _{bb(uvlo)} | _ | 1 | 2.5 | mA | $V_{bb} < 7V$ |
| | Operating current | I _{GNDL} | | 10 | 14 | mA | All Channels ON - no load |
| | Leakage output current (included in $I_{bb(off)}$) $V_{Dx} = low, each channel$ | I _{L(off)} | | 5 | 30 | μΑ | |
| Voltage domain V _{CC} | Operating voltage | V _{CC} | 3.0 | | 5.5 | V | |
| (Input interface) | Undervoltage shutdown | V _{CC(under)} | 2.5 | | 2.9 | | |
| | Undervoltage restart | $V_{CC(u_rst)}$ | | | 3 | | |
| | Undervoltage hysteresis | $\Delta V_{CC(under)}$ | | 0.1 | | | |
| | Undervoltage current | I _{CC(uvlo)} | | 1 | 2 | mA | V _{cc} < 2.5V |
| | Operating current | I _{CC(on)} | | 4.5 | 6 | mA | |

¹⁾ not subject to production test



4.5 Output Protection Functions

| Parameter ¹⁾ | Symbol | Limit Values | | | Unit | Test Condition |
|---|---------------------|--------------|--------------------------------|------|------|-----------------------|
| at T _j = -25 125°C, V_{bb} =1530V, V_{CC} =3.05.5V, unless otherwise specified | | min. | typ. | max. | | |
| Initial peak short circuit current limit, each channel $T_i = -25^{\circ}C$, $V_{bb} = 30V$, $t_m = 700\mu s$ | I _{L(SCp)} | | | 4.5 | Α | |
| $T_i = 25^{\circ}C$ | | | 3.0 | | | |
| $T_i = 125$ °C | | 1.4 | | | | |
| two parallel channels: ³⁾ four parallel channels: ³⁾ | | | current of on ne current of | | | |
| Repetitive short circuit current limit ³⁾ $T_{i} = T_{it} \text{ (see timing diagrams)}$ | I _{L(SCr)} | | | | | |
| each channel: | | | 2.2 | | | |
| two parallel channels: ³⁾ | | | 2.2 | | | |
| four parallel channels: ³⁾ | | | 2.2 | | | |
| Output clamp (inductive load switch off) at $V_{OUT} = V_{bb} - V_{ON(CL)}$ | V _{ON(CL)} | 47 | 53 | 60 | V | |
| Overvoltage protection | $V_{bb(AZ)}$ | 47 | | | | |
| Thermal overload trip temperature ²⁾³⁾ | T _{jt} | 135 | | | °C | |
| Thermal hysteresis ³⁾ | ΔT_{jt} | | 10 | | K | |

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet.
 Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continous repetitive operation.

- 2) Higher operating temperature at normal function for each channel available
- 3) not subject to production test, specified by design

4.6 Diagnostic Characteristics at pin DIAG

| Parameter | Symbol | Limit Values | | | Limit Values Unit T | |
|--|-------------------------|--------------|------|------|---------------------|--------------------------------|
| at T_j = -25 125°C, V_{bb} =1530V, V_{CC} =3.05.5V, unless otherwise specified | | min. | typ. | max. | | |
| Common diagnostic sink current (overtemperature of any channel) $T_j = 135^{\circ}C$ | I _{diagsink} | | | 5 | mA | V _{diagon} < 0.25xVCC |
| Common diagnostic source current | I _{diagsource} | | 100 | | μΑ | |



4.7 Input Interface

| Parameter Symb | | Limit Values | | | Unit | Test Condition |
|--|--------------------|--------------------------|------|--------------------------|------|-----------------------|
| at T_j = -25 125°C, V_{bb} =1530V, V_{CC} =3.05.5V, unless otherwise specified | | min. | typ. | max. | | |
| Input low state voltage (D0 D7, DIS, CS, WR) | V _{IL} | -0.3 | | 0.3 x V _{CC} | V | |
| Input high state voltage (D0 D7, DIS, CS, WR) | V _{IH} | 0.7 x V _{CC} | | V _{CC} + 0.3 | | |
| Input voltage hysteresis (D0 D7, DIS, CS, WR) | V _{IHys} | | 100 | | mV | |
| Input pull down current (D0 D7, DIS) | I _{Idown} | | 100 | | μΑ | |
| Input pull up current (CS, WR) | -I _{lup} | | 100 | | | |
| Output disable time (transition \overline{DIS} to logic low) ¹⁾²⁾ Normal operation Turn-off time to 10% V_{OUT} $R_L = 47\Omega$ | t _{DIS} | | 85 | 170 | μs | |
| Output disable time (transition \overline{DIS} to logic low) ¹⁾²⁾³⁾ Disturbed operation Turn-off time to 10% V_{OUT} $R_L = 47\Omega$ | t _{DIS} | | | 230 | | |

- 1) The time includes the turn-on/off time of the high-side switch and the transmission time via the coreless transformer.
- 2) If Pin DIS is set to low the outputs are set to low; after DIS set to high a new write cycle is necessary to set the output again.
- 3) The parameter is not subject to production test verified by design/characterization

4.8 Parallel Interface Input Timing

| Parameter | Symbol | Limit Values | | | Symbol Limit Values Uni | Unit | Test Condition |
|--|-------------------|--------------|------|------|-------------------------|------|-----------------------|
| at T_j = -25 125°C, V_{bb} =1530V, V_{CC} =3.05.5V, unless otherwise specified | | min. | typ. | max. | | | |
| WR pulse width | t _{WRPW} | 20 | | | ns | | |
| Data setup time before WR | t _{DS} | 20 | | | | | |
| Data hold time after WR | t _{DH} | 10 | | | | | |
| Chip select valid to WR | t _{CSWR} | 0 | | | | | |
| WR logic high to CS logic high | t _{whcs} | 10 | | | | | |
| Delay to next CS cycle | t _{CSD} | 20 | | | μs | | |
| Output data refresh rate in direct control mode | t _{OR} | 20 | | _ | | | |



4.9 Reverse Voltage

| Parameter | Symbol | Limit Values | | Unit | Test Condition | |
|--|------------------|--------------|------|------|-----------------------|--|
| at T_j = -25 125°C, V_{bb} =1530V, V_{CC} =3.05.5V, unless otherwise specified | | min. | typ. | max. | | |
| Reverse voltage ¹⁾²⁾ | -V _{bb} | | | | ٧ | |
| $R_{GND} = 0 \Omega$ | | | | 1 | | |
| $R_{GND} = 150 \Omega$ | | | | 45 | | |
| Diode forward on voltage | -V _{ON} | | | | | |
| IF = 1.25A, V _{Dx} = low, each channel | 5.1 | | | 1.2 | | |

¹⁾ defined by P_{tot}

4.10 Isolation and Safety-Related Specification

| Parameter Measured from input terminals to output terminals, unless otherwise specified | Value | Unit | Conditions |
|---|-------|-----------------|--|
| Rated dielectric isolation voltage V _{ISO} | 500 | V _{AC} | 1 - minute duration ¹⁾ |
| Short term temporary overvoltage | 1250 | V | 5s acc. DIN EN60664-1 1) |
| Minimum external air gap (clearance) | 2.6 | mm | shortest distance through air. |
| Minimum external tracking (creepage) | 2.6 | mm | shortest distance path along body. |
| Minimum Internal Gap | 0.01 | mm | Insulation distance through insulation |

¹⁾ The parameter is not subject to production test, verified by characterization; Production Test with 1100V, 100ms duration

4.11 Reliability

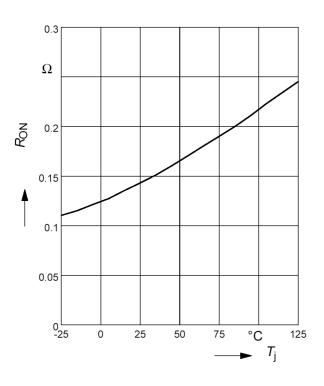
For Qualification Report please contact your local Infineon Technologies office!

²⁾ not subject to production test, specified by design



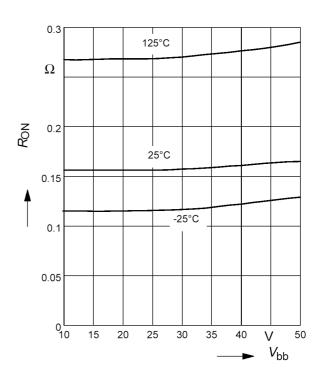
Typ. on-state resistance

$$R_{ON} = f(T_j)$$
; $V_{bb} = 15V$; $V_{in} = high$



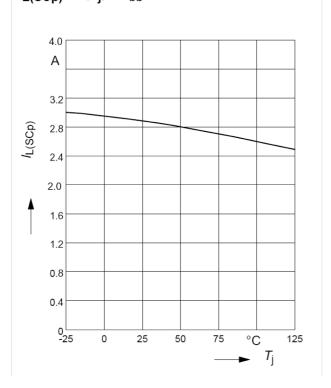
Typ. on-state resistance

$$R_{ON} = f(V_{bb}); I_{L} = 0.5A; V_{in} = high$$



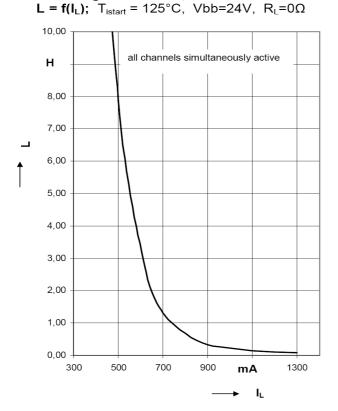
Typ. initial peak short circuit current limit

$$I_{L(SCp)} = f(T_j)$$
; $V_{bb} = 24V$



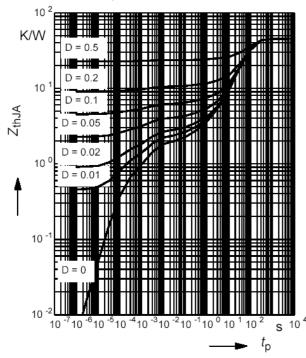


Maximum allowable load inductance for a single switch off, calculated

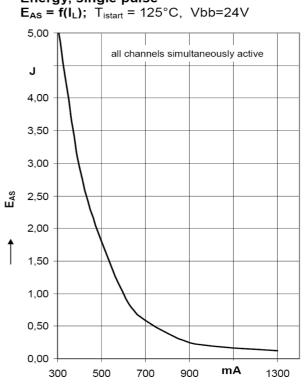


Typ. transient thermal impedance $Z_{\text{thJA}} = f(t_{\text{p}})$ @ min. footprint

Parameter: $D=t_p/T$

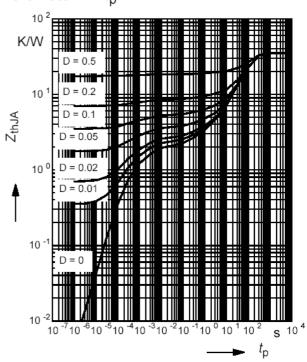


Maximum allowable inductive switch-off Energy, single pulse



Typ. transient thermal impedance $Z_{\rm thJA}$ =f($t_{\rm p}$) @ 6cm² heatsink area

Parameter: $D=t_p/T$





Package Outlines

5 Package Outlines

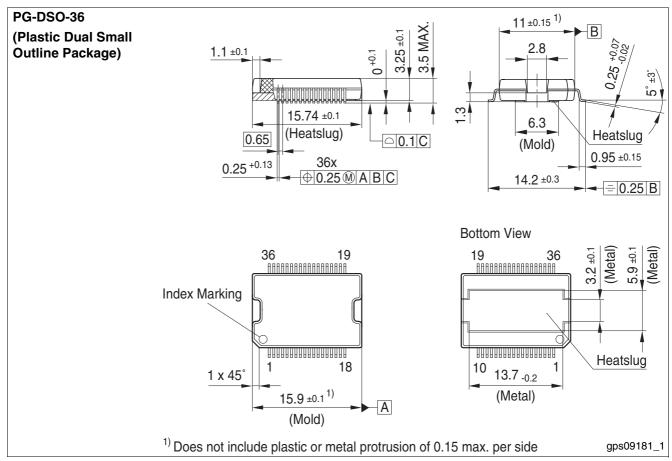


Figure 12 PG-DSO36

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ПОСТАВКА ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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http://moschip.ru/get-element

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