

# **BUK9207-30B**

# N-channel TrenchMOS logic level FET Rev. 03 — 16 June 2010

**Product data sheet** 

## **Product profile**

#### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

#### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant

- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 185 °C rating

### 1.3 Applications

- 12 V loads
- Automotive systems

- General purpose power switching
- Motors, lamps and solenoids

#### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \ge 25 ^{\circ}\text{C}; T_j \le 185 ^{\circ}\text{C}$		-	-	30	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; see <u>Figure 1</u> ; see <u>Figure 3</u>	<u>[1]</u>	-	-	75	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>		-	-	167	W
Static chara	acteristics						
R <sub>DSon</sub>	drain-source on-state	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}$		-	4.4	5	mΩ
	resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 9}}{\text{see Figure 10}};$		-	5.9	7	mΩ



### N-channel TrenchMOS logic level FET

Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Avalanche	ruggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 75 A; $V_{sup} \le 30$ V; $R_{GS}$ = 50 $\Omega$ ; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	329	mJ
Dynamic ch	naracteristics					
$Q_{GD}$	gate-drain charge	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A};$ $V_{DS} = 24 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see Figure 11	-	12	-	nC

<sup>[1]</sup> Continuous current is limited by package.

# 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain <sup>[1]</sup>	mb	D
3	S	source		$G \longrightarrow A$
mb	D	mounting base; connected to drain	1 3	mbb076 S
			SOT428 (DPAK)	

<sup>[1]</sup> It is not possible to make connection to pin 2.

# 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9207-30B	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

# 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 185 °C		-	-	30	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$		-	-	30	V
$V_{GS}$	gate-source voltage			-15	-	15	V
I <sub>D</sub>	drain current	$T_{mb} = 25  ^{\circ}\text{C};  V_{GS} = 5  \text{V};  \text{see}  \frac{\text{Figure 1}}{\text{Figure 1}};$	<u>[1]</u>	-	-	75	V V
		see Figure 3	[2]	-	-	112	Α
		$T_{mb} = 100  ^{\circ}\text{C};  V_{GS} = 5  \text{V};  \text{see}  \frac{\text{Figure 1}}{}$	<u>[1]</u>	-	-	75	Α
I <sub>DM</sub>	peak drain current	$T_{mb}$ = 25 °C; $t_p$ ≤ 10 μs; pulsed; see Figure 3		-	-	449	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>		-	-	167	W
T <sub>stg</sub>	storage temperature			-55	-	185	°C
Tj	junction temperature			-55	-	185	°C
Source-drain	diode						
Is	source current	T <sub>mb</sub> = 25 °C	[3]	-	-	75	Α
			[2]	-	-	112	Α
I <sub>SM</sub>	peak source current	$t_p \le 10 \ \mu s$ ; pulsed; $T_{mb} = 25 \ ^{\circ}C$		-	-	449	Α
Avalanche ru	iggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 75 A; $V_{sup}$ ≤ 30 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped		-	-	329	mJ

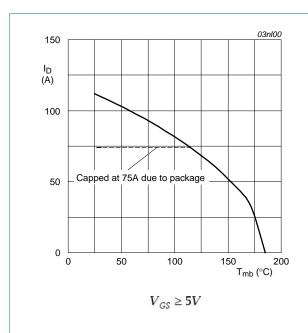
<sup>[1]</sup> Continuous current is limited by package.

<sup>[2]</sup> Current is limited by power dissipation chip rating.

<sup>[3]</sup> Continuous current is limited by package.

03no96

#### N-channel TrenchMOS logic level FET



 $P_{der}$  (%)

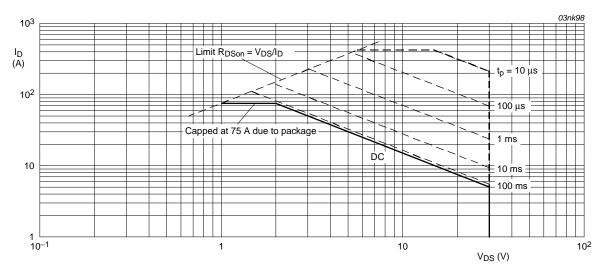
80

40  $P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$ 

120

Fig 1. Normalized continuous drain current as a function of mounting base temperature

Fig 2. Normalized total power dissipation as a function of mounting base temperature



 $T_{mb} = 25$ °C;  $I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.95	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient		-	71.4	-	K/W

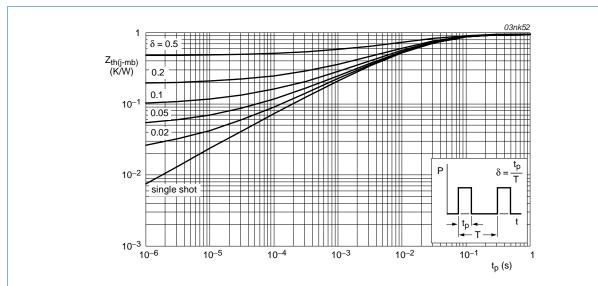


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

# 6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
$V_{(BR)DSS}$	drain-source	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	30	-	-	V
	breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = -55 \text{ °C}$ ; see <u>Figure 8</u>	-	-	2.3	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = 25$ °C; see <u>Figure 8</u>	1.1	1.5	2	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 185 \text{ °C}$ ; see <u>Figure 8</u>	0.4	-	-	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	1	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 185 \text{ °C}$	-	-	500	μΑ
I <sub>GSS</sub>	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 15 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nΑ
		$V_{DS} = 0 \text{ V}; V_{GS} = -15 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
$R_{DSon}$	drain-source on-state	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}$	-	4.4	5	$m\Omega$
	resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}$	-	-	7.7	$m\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 185 °C;$ see <u>Figure 9</u> ; see <u>Figure 10</u>	-	-	13.3	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 9</u> ; see <u>Figure 10</u>	-	5.9	7	mΩ
Dynamic	characteristics					
Q <sub>G(tot)</sub>	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 5 \text{ V};$	-	31	-	nC
$Q_{GS}$	gate-source charge	T <sub>j</sub> = 25 °C; see <u>Figure 11</u>	-	8	-	nC
$Q_{GD}$	gate-drain charge		-	12	-	nC
C <sub>iss</sub>	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	2573	3430	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; see <u>Figure 12</u>	-	635	762	pF
C <sub>rss</sub>	reverse transfer capacitance		-	268	367	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 25 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 5 \text{ V};$	-	19	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 10 \Omega; T_j = 25 \degree C$	-	82	-	ns
$t_{d(off)}$	turn-off delay time		-	100	-	ns
t <sub>f</sub>	fall time		-	107	-	ns
L <sub>D</sub>	internal drain inductance	measured from drain to center of die ; $T_j = 25  ^{\circ}\text{C}$	-	2.5	-	nΗ
L <sub>S</sub>	internal source inductance	measured from source lead to source bond pad; $T_j = 25$ °C	-	7.5	-	nΗ
Source-d	rain diode					
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ °C}$ ; see <u>Figure 13</u>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 20 \text{ A}$ ; $dI_S/dt = -100 \text{ A/}\mu\text{s}$ ;	-	55	-	ns
Q <sub>r</sub>	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 25 \text{ V}; T_j = 25 \text{ °C}$	-	42	-	nC

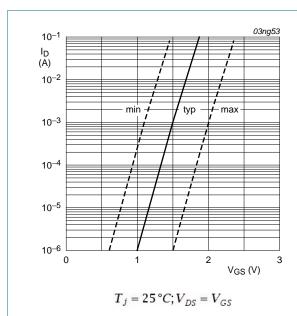


Fig 5. Sub-threshold drain current as a function of gate-source voltage

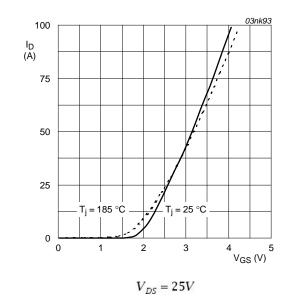


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

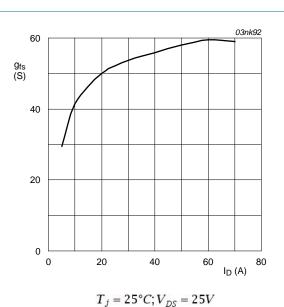


Fig 6. Forward transconductance as a function of drain current; typical values

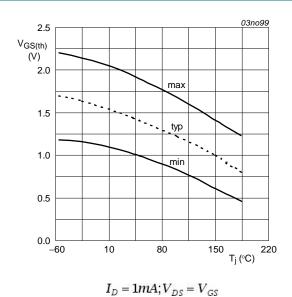


Fig 8. Gate-source threshold voltage as a function of junction temperature

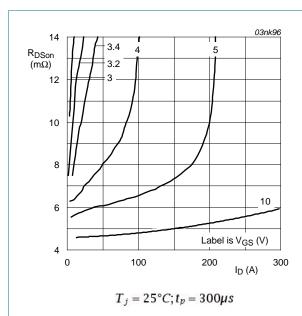


Fig 9. Drain-source on-state resistance as a function of drain current; typical values

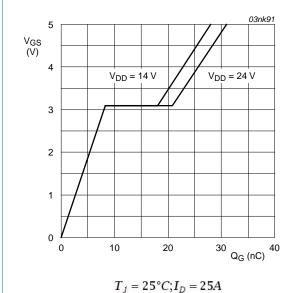


Fig 11. Gate-source voltage as a function of turn-on gate charge; typical values

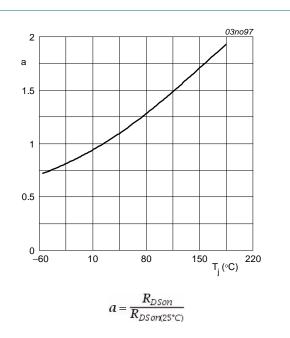
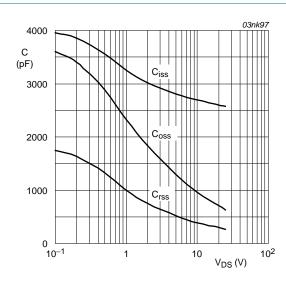
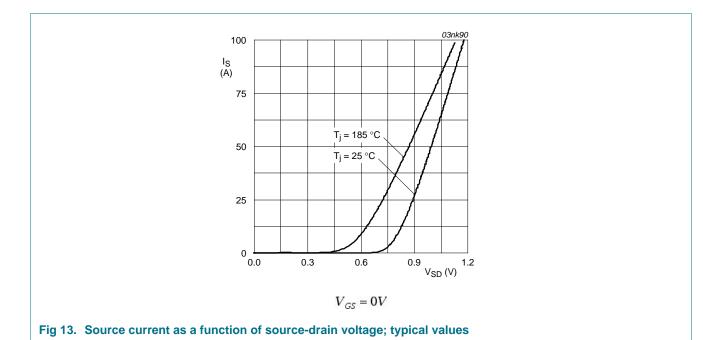


Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



 $V_{GS} = 0V; f = 1MHz$ 

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



# 7. Package outline

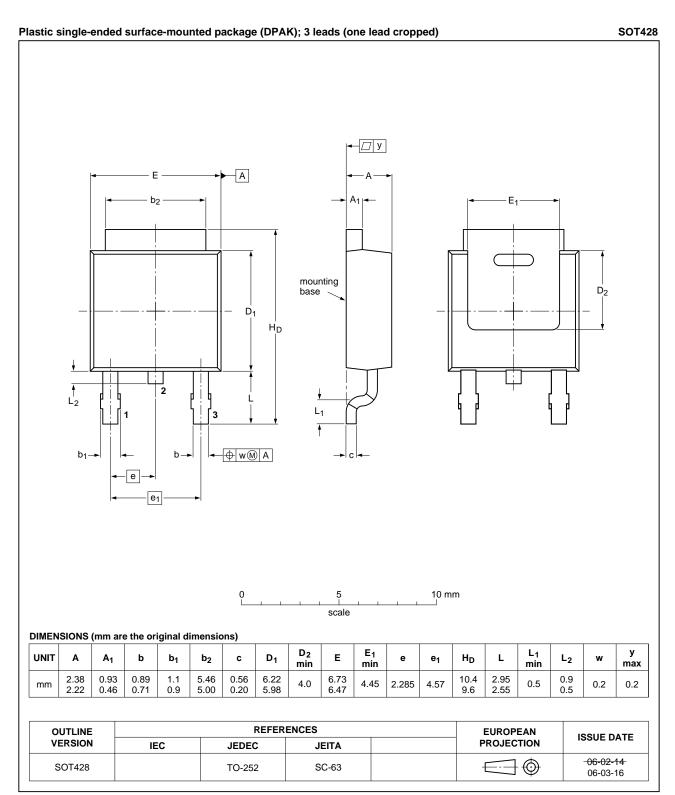


Fig 14. Package outline SOT428 (DPAK)

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# 8. Revision history

#### Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BUK9207-30B v.3	20100616	Product data sheet	-	BUK9207-30B v.2	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guideline of NXP Semiconductors.</li> </ul>				
	<ul> <li>Legal texts</li> </ul>	have been adapted to the	new company name where	appropriate.	
BUK9207-30B v.2 (9397 750 12233)	20031212	Product data	-	-	

## 9. Legal information

#### 9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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# BUK9207-30B

# **Nexperia**

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# 11. Contents

1	Product profile
1.1	General description
1.2	Features and benefits1
1.3	Applications1
1.4	Quick reference data1
2	Pinning information2
3	Ordering information2
4	Limiting values3
5	Thermal characteristics5
6	Characteristics6
7	Package outline10
8	Revision history11
9	Legal information12
9.1	Data sheet status
9.2	Definitions12
9.3	Disclaimers
9.4	Trademarks13
10	Contact information13

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