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Si3457DV

Single P-Channel Logic Level PowerTrench® MOSFET

General Description

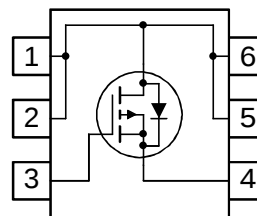
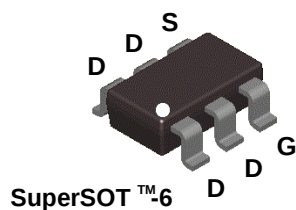
This P-Channel Logic Level MOSFET is produced using Fairchild's advanced PowerTrench process. It has been optimized for battery power management applications.

Applications

- Battery management
- Load switch
- Battery protection

Features

- -4 A, -30 V. $R_{DS(ON)} = 50 \text{ m}\Omega @ V_{GS} = -10 \text{ V}$
 $R_{DS(ON)} = 75 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	-30	V
V _{GSS}	Gate-Source Voltage	±25	V
I _D	Drain Current – Continuous (Note 1a)	-4	A
	– Pulsed	-20	
P _D	Maximum Power Dissipation (Note 1a)	1.6	W
	(Note 1b)	0.8	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	30	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.457	Si3457DV	7"	8mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C		-22		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C		4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10\text{ V}, I_D = -4\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -3.4\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -4\text{ A}; T_J = 125^\circ$		44 67 60	50 75 70	m Ω
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	-20			A
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -4\text{ A}$		8.4		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		470		pF
C_{oss}	Output Capacitance			126		pF
C_{rss}	Reverse Transfer Capacitance			61		pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -15\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$		7	14	ns
t_r	Turn–On Rise Time			12	22	ns
$t_{d(off)}$	Turn–Off Delay Time			16	29	ns
t_f	Turn–Off Fall Time			6	12	ns
Q_g	Total Gate Charge	$V_{DS} = -15\text{ V}, I_D = -4\text{ A},$ $V_{GS} = -5\text{ V}$		6	8.1	nC
Q_{gs}	Gate–Source Charge			2.1		nC
Q_{gd}	Gate–Drain Charge			2		nC

Drain–Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain–Source Diode Forward Current				–1.3	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = –1.3 A (Note 2)		–0.77	–1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- a) 78°C/W when mounted on a 1 in^2 pad of 2 oz copper



- b) 156°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

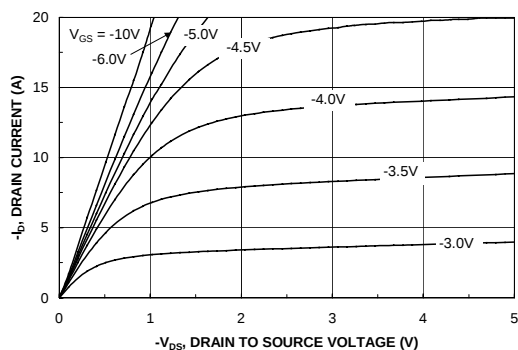


Figure 1. On-Region Characteristics.

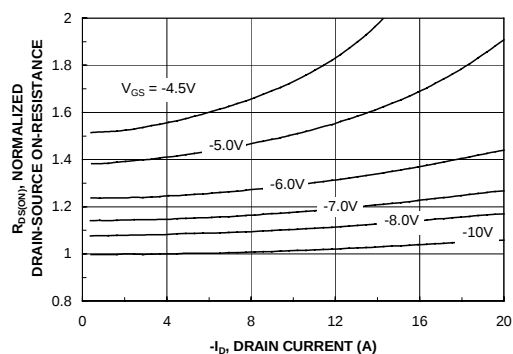


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

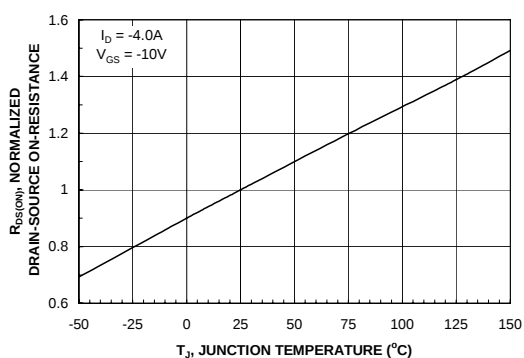


Figure 3. On-Resistance Variation with Temperature.

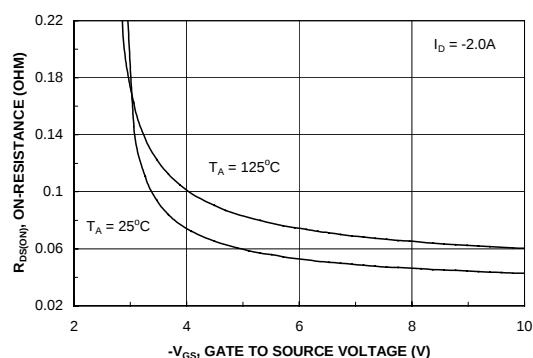


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

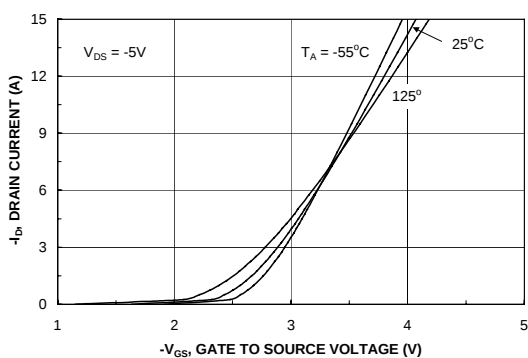


Figure 5. Transfer Characteristics.

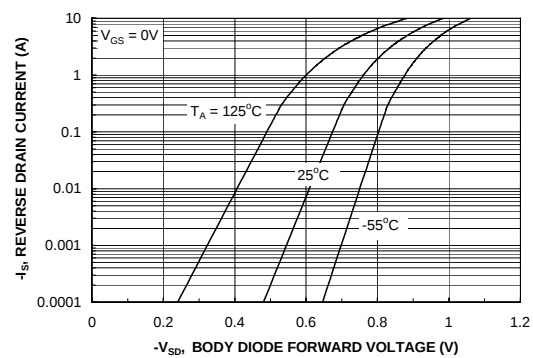


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

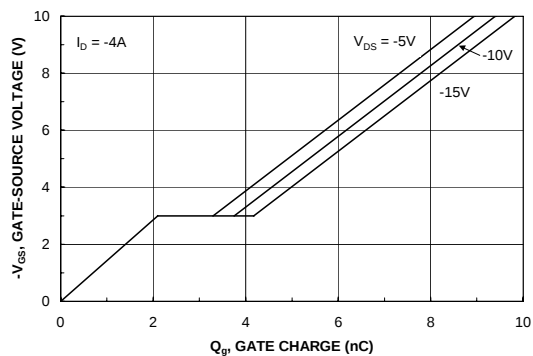


Figure 7. Gate Charge Characteristics.

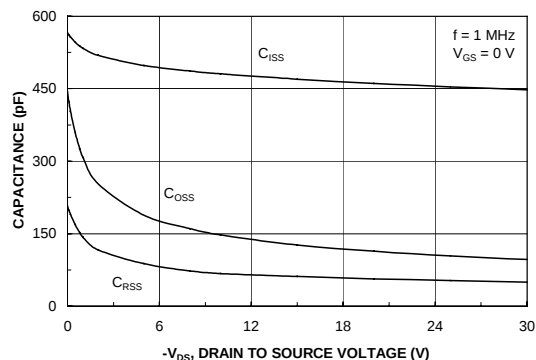


Figure 8. Capacitance Characteristics.

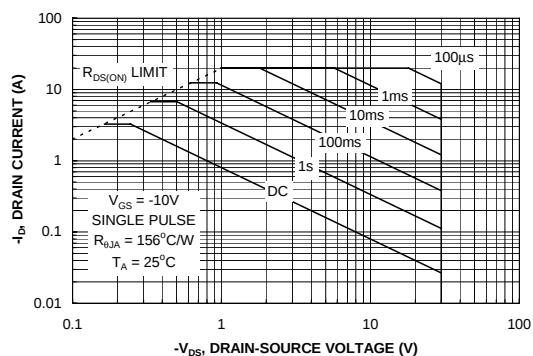


Figure 9. Maximum Safe Operating Area.

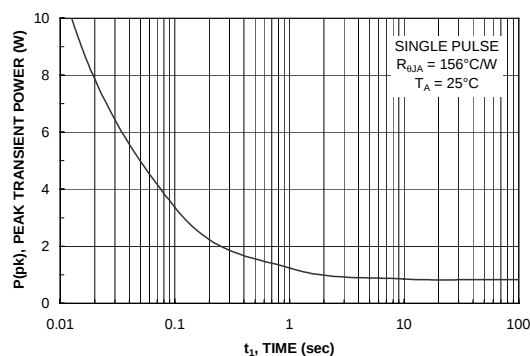


Figure 10. Single Pulse Maximum Power Dissipation.

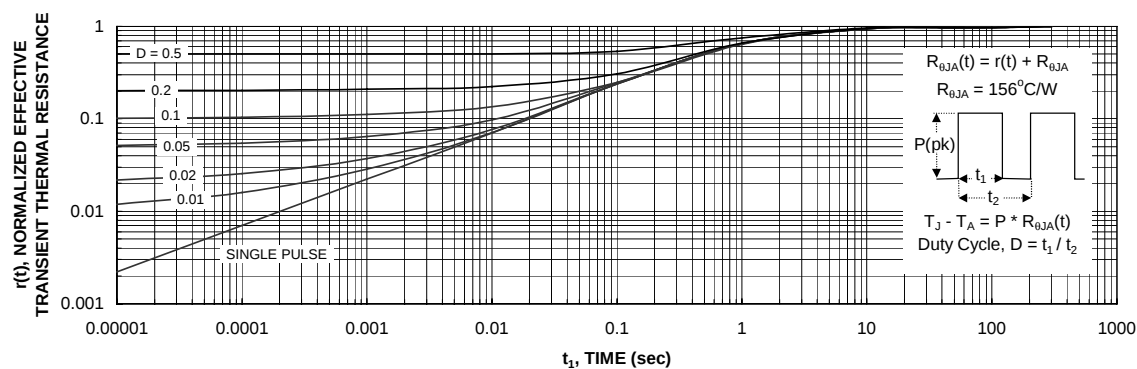


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

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moschip.ru

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