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January 2015

FDMS86202ET120

N-Channel Shielded Gate PowerTrench® MOSFET 120 V, 102 A, 7.2 m Ω

Features

- Extended T_J rating to 175°C
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)} = 7.2 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 13.5 \text{ A}$
- Max $r_{DS(on)} = 10.3 \text{ m}\Omega$ at $V_{GS} = 6 \text{ V}$, $I_D = 11.5 \text{ A}$
- Advanced Package and Silicon combination for low r_{DS(on)} and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

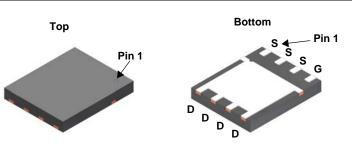


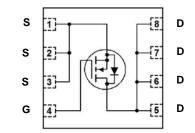
General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Application

■ DC-DC Conversion





Power 56

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parame		Ratings	Units	
V_{DS}	Drain to Source Voltage			120	V
V_{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25 °C	(Note 5)	102	
	-Continuous	T _C = 100 °C	(Note 5)	72	Α
I _D	-Continuous	T _A = 25 °C	(Note 1a)	13.5	— A
	-Pulsed		(Note 4)	538	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	600	mJ
D	Power Dissipation	T _C = 25 °C		187	w
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	3.3	VV
T _J , T _{STG}	Operating and Storage Junction Tempera	ture Range		-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.8	°C/W
R_{\thetaJA}	Thermal Resistance, Junction to Ambient (Note 1a)	45	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86202ET	FDMS86202ET120	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Parameter

Off Characteristics								
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	120			V		
$\Delta BV_{DSS} \over \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		103		mV/°C		
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 96 V, V _{GS} = 0 V			1	μΑ		
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA		

Test Conditions

Min

Тур

Max

Units

On Characteristics

Symbol

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		-10		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 13.5 A		6.0	7.2	
		$V_{GS} = 6 \text{ V}, I_D = 11.5 \text{ A}$		8.1	10.3	mΩ
		$V_{GS} = 10 \text{ V}, I_D = 13.5 \text{ A}, T_J = 125 ^{\circ}\text{C}$		10.9	13.2	
9 _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 13.5 A		44		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 60.V V 0.V		3275	4585	pF
Coss	Output Capacitance	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		460	644	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12		17	30	pF
R_g	Gate Resistance		0.1	0.9	2.7	Ω

Switching Characteristics

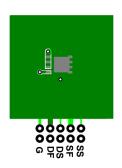
t _{d(on)}	Turn-On Delay Time			21	33	ns
t _r	Rise Time	V _{DD} = 60 V, I _D = 13.5 A,		8.75	17.5	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$		27.2	44	ns
t _f	Fall Time			6.1	12.2	ns
Q_g	Total Gate Charge	V _{GS} = 0 V to 10 V		45	64	nC
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V to 6 V}$ $V_{DD} = 6$	60 V,	29	41	nC
Q_{gs}	Gate to Source Charge	I _D = 13.	5 A	14.3		nC
Q_{ad}	Gate to Drain "Miller" Charge			9.5		nC

Drain-Source Diode Characteristics

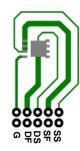
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.1 \text{ A}$ (Note 2)	0.69	1.2	V
		$V_{GS} = 0 \text{ V}, I_S = 13.5 \text{ A}$ (Note 2)	0.76	1.3	
t _{rr}	Reverse Recovery Time	I _F = 13.5 A, di/dt = 100 A/μs	79	127	ns
Q _{rr}	Reverse Recovery Charge	T _F = 13.5 A, α//αt = 100 A/μs	140	224	nC

Notes:

^{1.} R_{0JA} is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0CA} is determined by the user's board design.



a) 45 °C/W when mounted on a 1 in² pad of 2 oz copper



b) 115 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- 3. E_{AS} of 600 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 20 A, V_{DD} = 120 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 65 A.
- 4. Pulse Id please refer to Fig.11 SOA curve for detail.
- 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_J = 25 °C unless otherwise noted

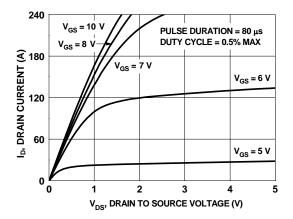


Figure 1. On Region Characteristics

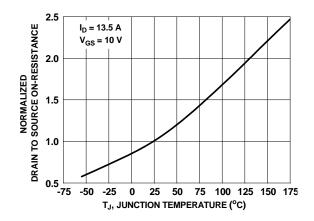


Figure 3. Normalized On Resistance vs Junction Temperature

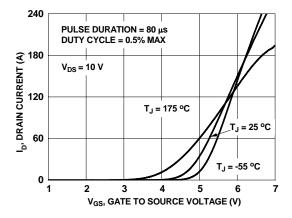


Figure 5. Transfer Characteristics

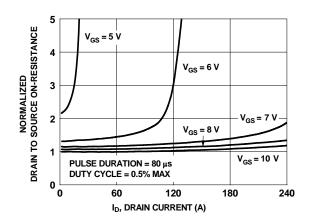


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

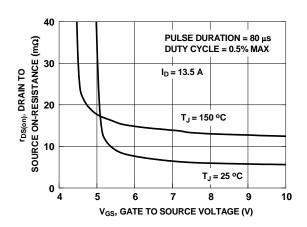


Figure 4. On-Resistance vs Gate to Source Voltage

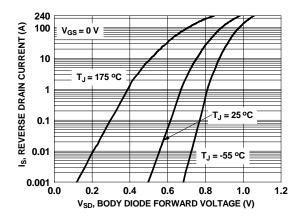


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

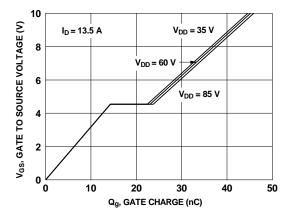


Figure 7. Gate Charge Characteristics

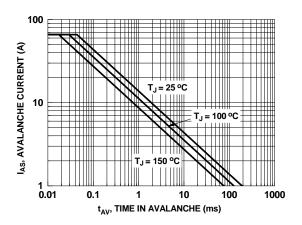


Figure 9. Unclamped Inductive Switching Capability

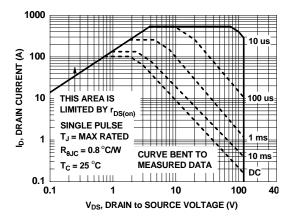


Figure 11. Forward Bias Safe Operating Area

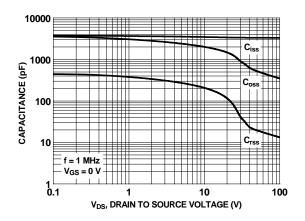


Figure 8. Capacitance vs Drain to Source Voltage

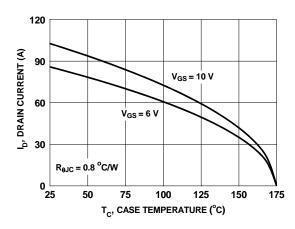


Figure 10. Maximum Continuous Drain Current vs Case Temperature

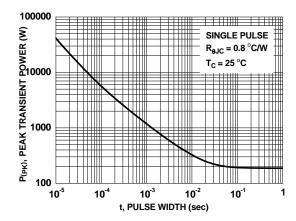


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25$ °C unless otherwise noted

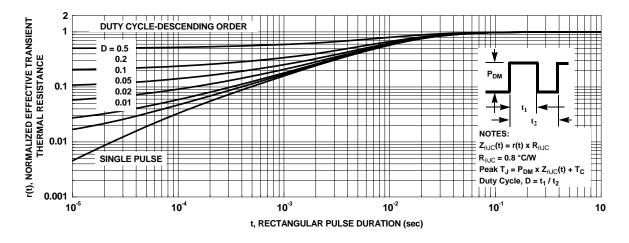
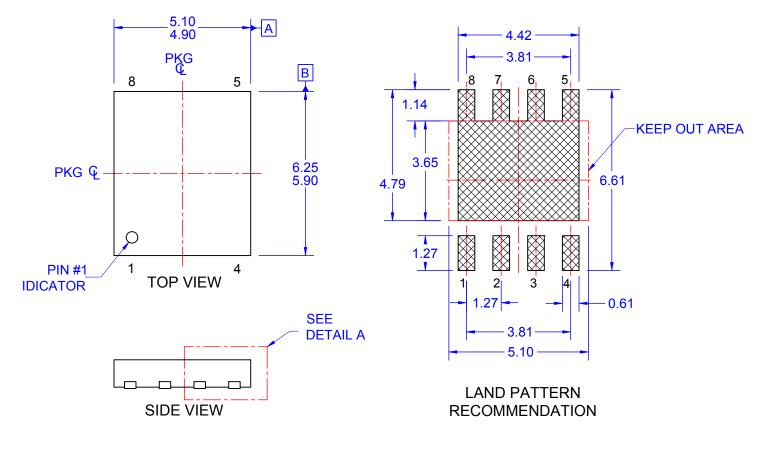
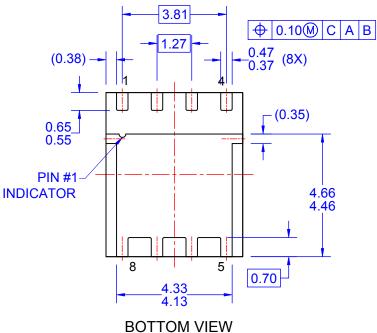
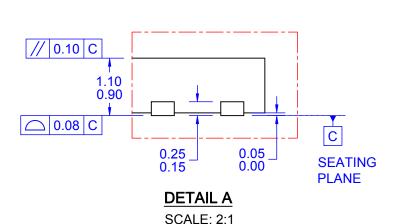


Figure 13. Junction-to-Ambient Transient Thermal Response Curve







NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F) DRAWING FILE NAME: PQFN08JREV3.



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