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June 2014

FDMC8026S

N-Channel PowerTrench® SyncFET™

30 V, 21 A, 4.4 mΩ

Features

- Max $r_{DS(on)}$ = 4.4 mΩ at V_{GS} = 10 V, I_D = 19 A
- Max $r_{DS(on)}$ = 5.2 mΩ at V_{GS} = 4.5 V, I_D = 17.5 A
- Advanced package and silicon combination for low $r_{DS(on)}$ and high efficiency
- SyncFET Schottky Body Diode
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

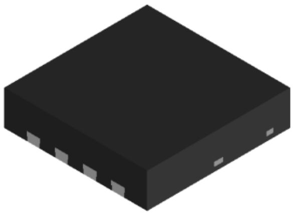
General Description

The FDMC8026S has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance.This device has the added benefit of an efficient monolithic schottky body diode.

Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/GPU low side switch
- Networking Point of Load low side switch
- Telecom secondary side rectification

Top



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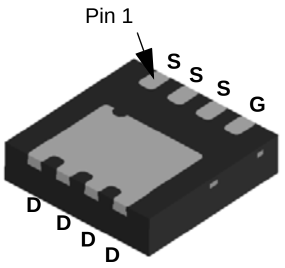
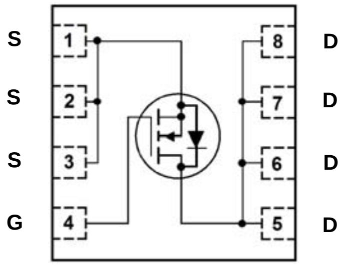




MLP 3.3x3.3

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 4)	±20	V
I_D	Drain Current -Continuous T_C = 25°C	21	A
	-Continuous T_A = 25°C (Note 1a)	19	
	-Pulsed	100	
E_{AS}	Single Pulse Avalance Energy (Note 3)	66	mJ
P_D	Power Dissipation T_C = 25°C	36	W
	Power Dissipation T_A = 25°C (Note 1a)	2.4	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8026S	FDMC8026S	MLP 3.3X3.3	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25 °C		26		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			500	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1 mA	1.2	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25 °C		-5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 19 A		3.8	4.4	mΩ
		V_{GS} = 4.5 V, I_D = 17.5 A		4.5	5.2	
		V_{GS} = 10 V, I_D = 19 A, T_J = 125 °C		4.5	5.8	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 19 A		106		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		2380	3165	pF
C_{oss}	Output Capacitance			885	1175	pF
C_{rss}	Reverse Transfer Capacitance			100	150	pF
R_g	Gate Resistance		0.1	0.7	2.5	Ω

Switching Characteristics

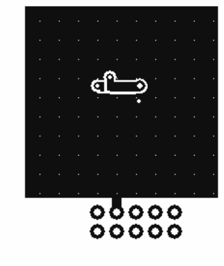
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 19 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		11	20	ns
t_r	Rise Time			5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			30	48	ns
t_f	Fall Time			4	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V V_{DD} = 15 V, I_D = 19 A		37	52	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V		18	25	nC
Q_{gs}	Gate to Source Charge			6		nC
Q_{gd}	Gate to Drain “Miller” Charge			6		nC

Drain-Source Diode Characteristics

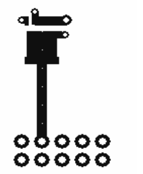
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)		0.6	0.8	V
		V_{GS} = 0 V, I_S = 19 A (Note 2)		0.8	1.2	
t_{rr}	Reverse Recovery Time	I_F = 19 A, di/dt = 300 A/μs		29	47	ns
Q_{rr}	Reverse Recovery Charge			33	53	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. E_{AS} of 66 mJ is based on starting T_J = 25 °C, L = 0.3 mH, I_{AS} = 21 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% tested at L = 3 mH, I_{AS} = 10.2 A.

4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

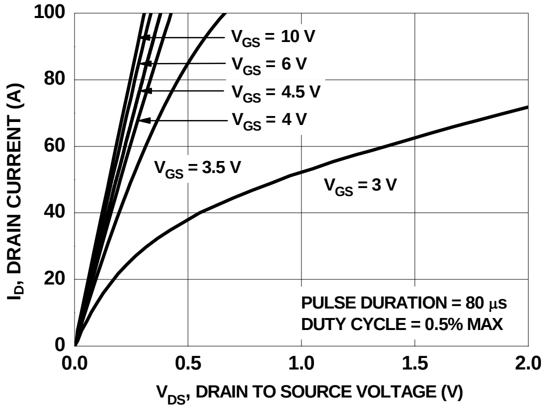


Figure 1. On Region Characteristics

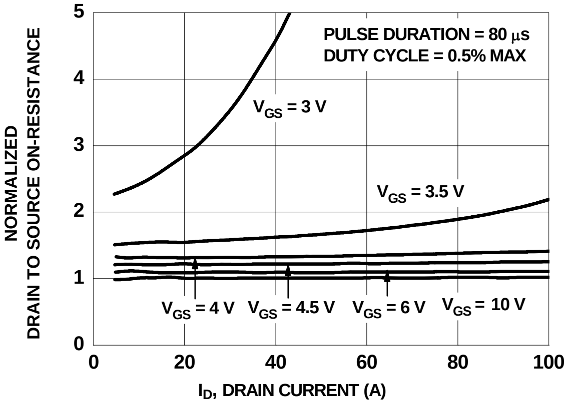


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

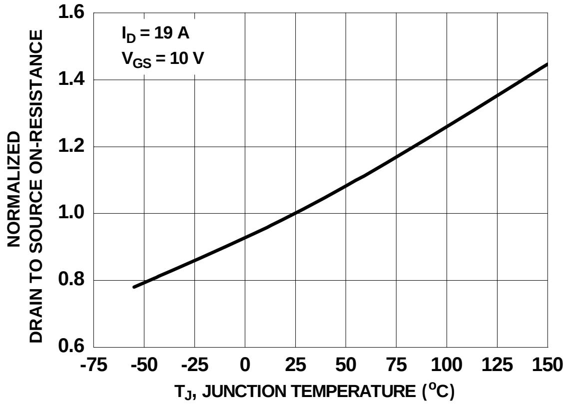


Figure 3. Normalized On Resistance vs. Junction Temperature

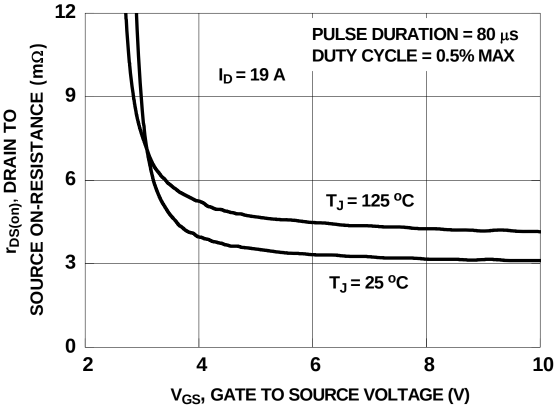


Figure 4. On-Resistance vs. Gate to Source Voltage

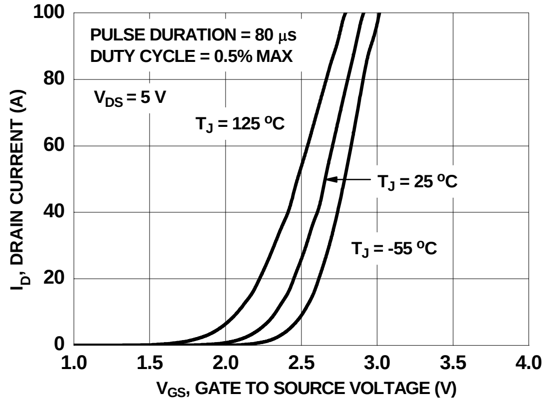


Figure 5. Transfer Characteristics

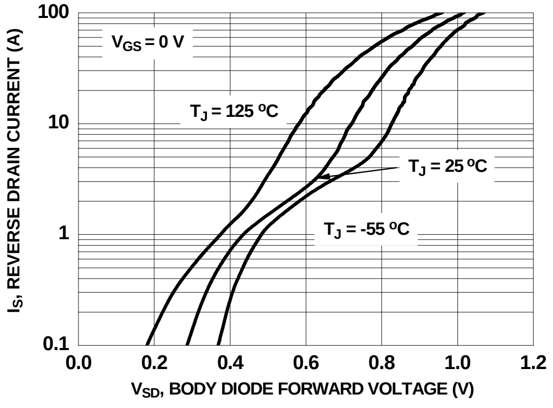


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

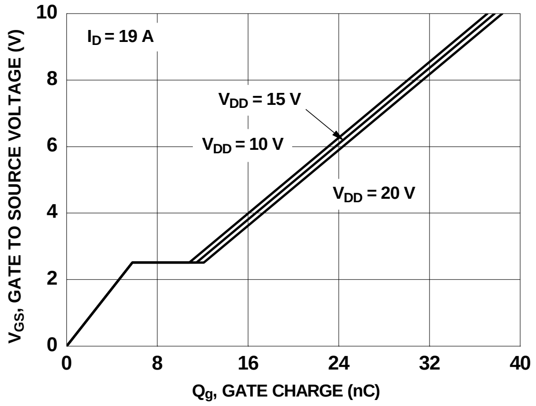


Figure 7. Gate Charge Characteristics

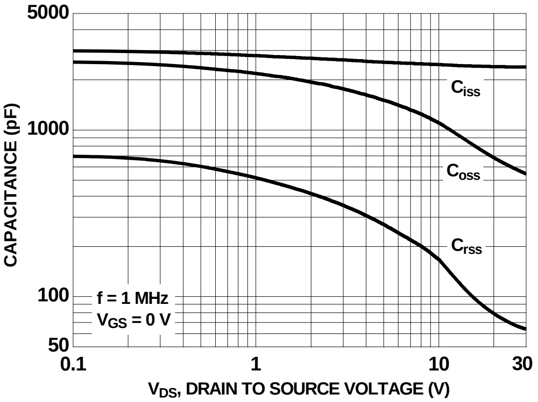


Figure 8. Capacitance vs. Drain to Source Voltage

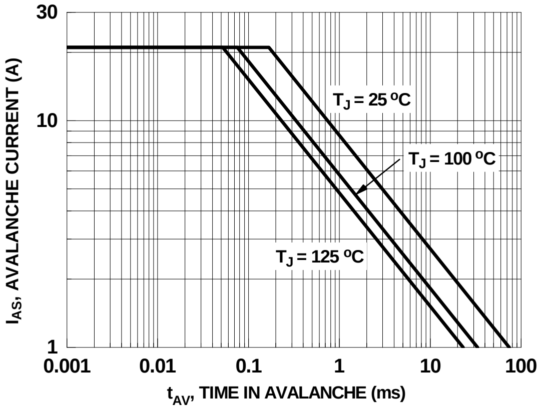


Figure 9. Unclamped Inductive Switching Capability

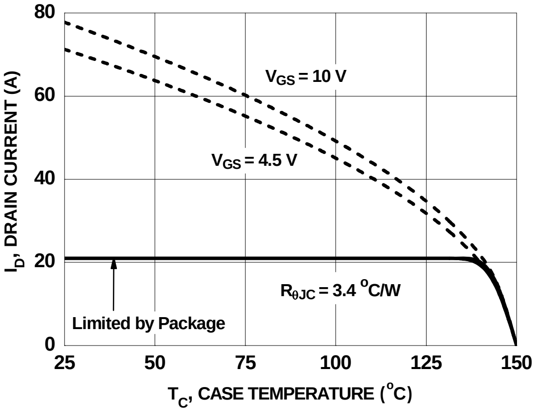


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

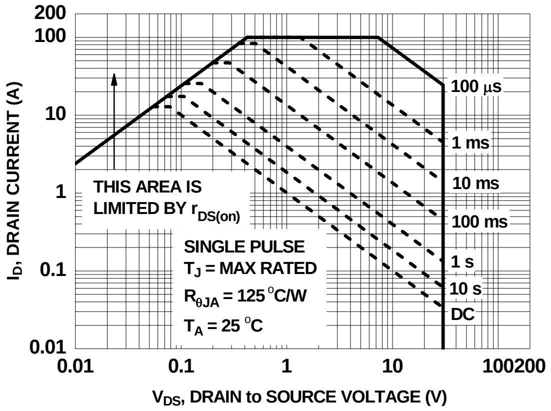


Figure 11. Forward Bias Safe Operating Area

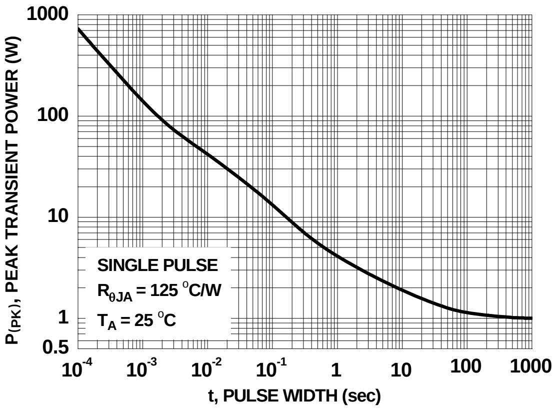


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

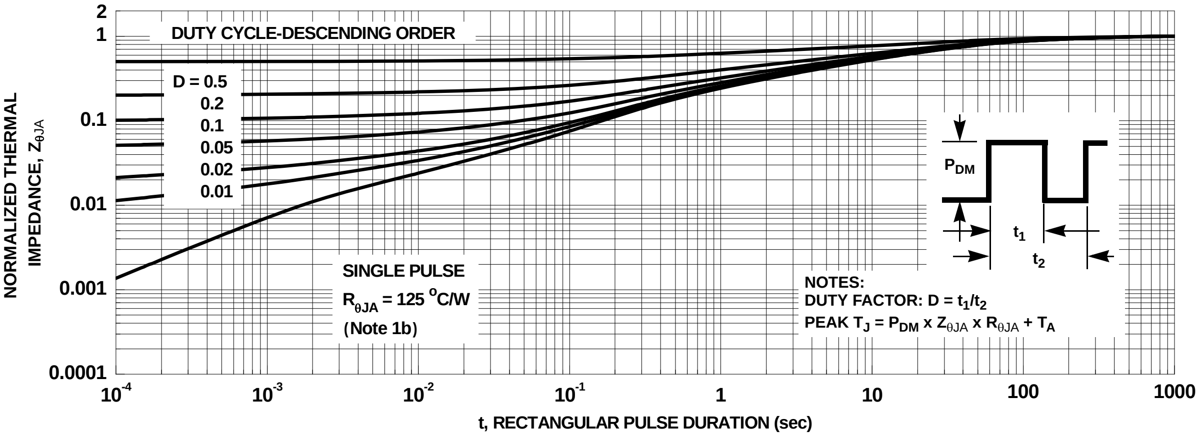


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET^{TM} Schottky body diode Characteristics

Fairchild's SyncFET^{TM} process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMC8026S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

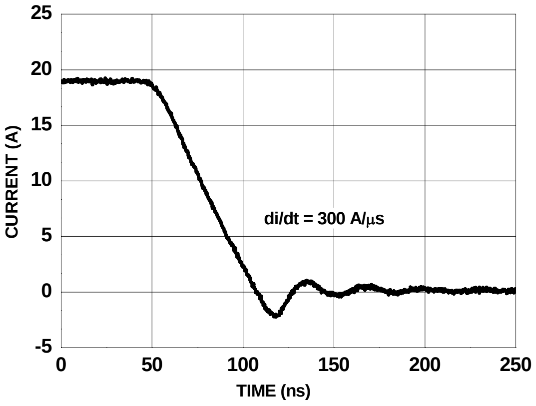


Figure 14. FDMC8026S SyncFET^{TM} Body Diode Reverse Recovery Characteristic

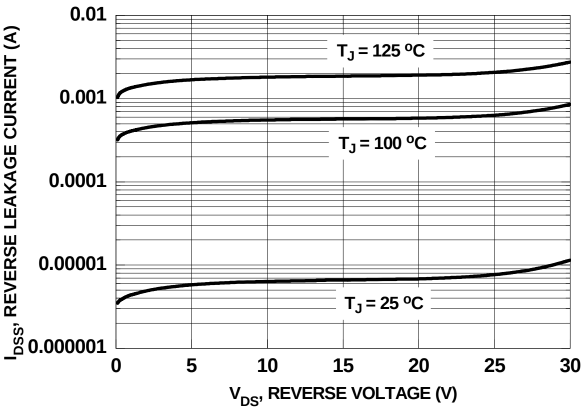
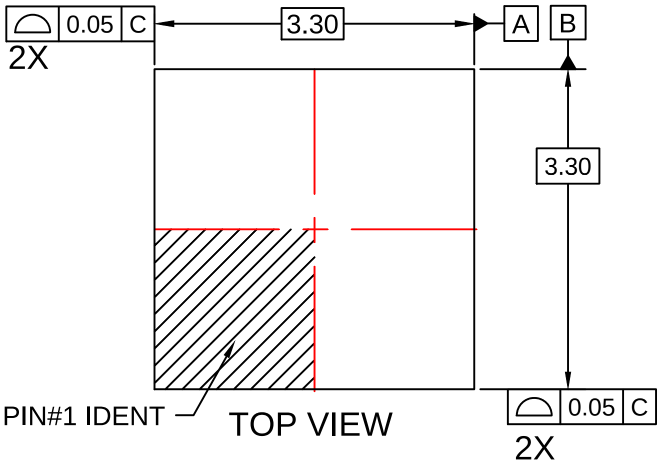
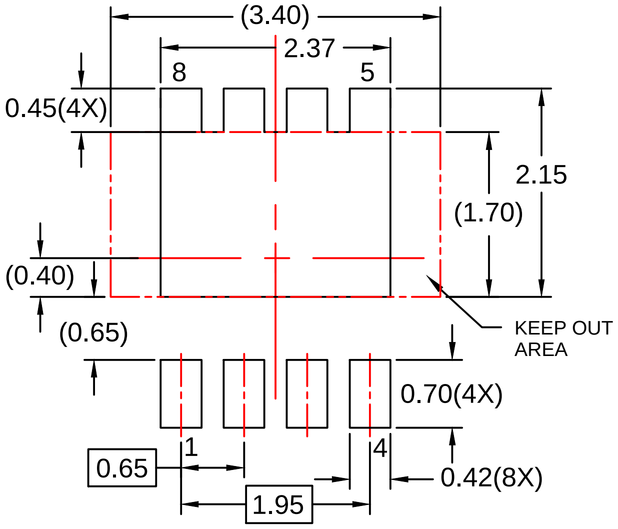


Figure 15. SyncFET^{TM} Body Diode Reverse Leakage vs. Drain-Source Voltage



TOP VIEW



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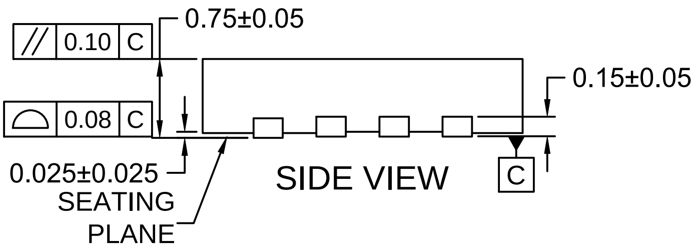
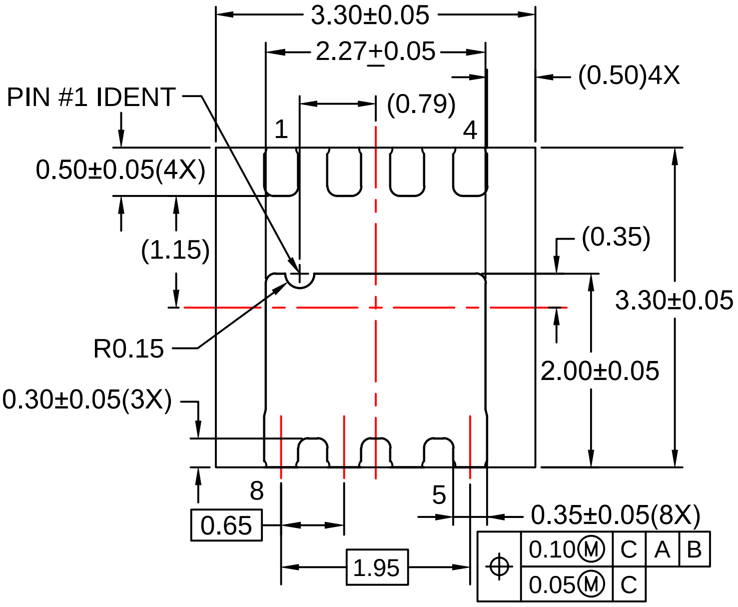


SIDE VIEW



BOTTOM VIEW

NOTES:

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многоканальный
+7 495 668 12 70
info@moschip.ru

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Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
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