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FSA3031 — Dual High-Speed USB2.0 with Mobile High-Definition Link (MHL™)

Features

- Low On Capacitance: 4.6 pF/6.75 pF MHL/USB (Typical)
- Low Power Consumption: 30 μ A Maximum
- Supports MHL Rev. 2.0
- Passes 1080 p/60 fps (3 Gbps) MHL Data Eye Diagram Mask Compliance
- MHL Data Rate: \geq 4.7Gbps with Ideal Input Source
- Packaged in 12-Lead UMLP (1.8 x 1.8 mm)
- Over-Voltage Tolerance (OVT) on all USB Ports Up to 5.25 V without External Components

Applications

- Cell Phones and Digital Cameras

IMPORTANT NOTE:

For additional performance information, please contact interface@fairchildsemi.com.

Description

The FSA3031 is a bi-directional, low-power, high-speed, 3:1, dual USB2.0 and MHL switch. Configured as a double-pole, triple-throw (DP3T) switch; it is optimized for switching between dual high- or full-speed USB and Mobile High-Definition Link sources (MHL™ Rev. 2.0 specification).

The FSA3031 contains special circuitry on the switch I/O pins, for applications where the V_{CC} supply is powered off ($V_{CC}=0$), that allows the device to withstand an over-voltage condition. This switch is designed to minimize current consumption even when the control voltage applied to the control pins is lower than the supply voltage (V_{CC}). This feature is especially valuable to mobile applications, such as cell phones; allowing direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, digital cameras, and notebook computers.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSA3031UMX	LX	-40 to +85°C	12-Lead, Ultrathin Molded Leadless Package (UMLP), 1.8 mm x 1.8 mm

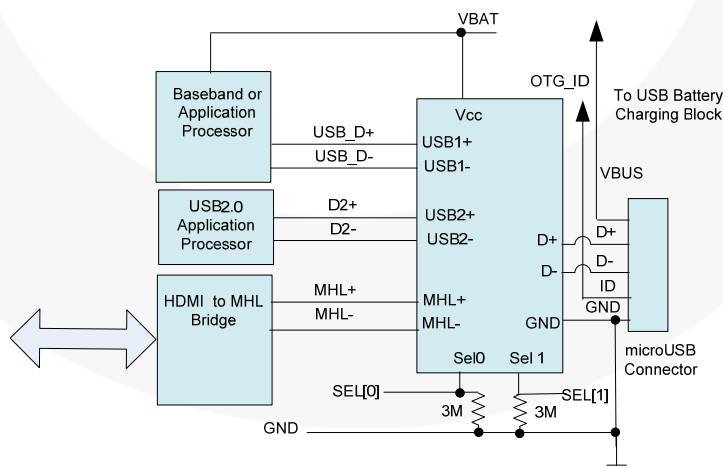


Figure 1. Typical Application

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Analog Symbol

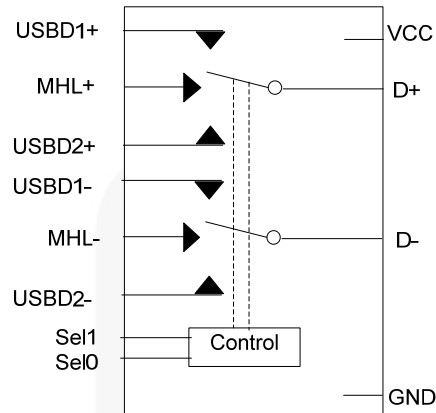


Figure 2. Analog Symbol

Table 1. Data Switch Select Truth Table

SEL1 ⁽¹⁾	SEL0 ⁽¹⁾	Function
0	0	D+/D- connected to USB1+/USB1-
0	1	D+/D- connected to USB2+/USB2-
1	0	D+/D- connected to MHL+/MHL
1	1	D+/D- high impedance

Note:

- Control inputs should never be left floating or unconnected. To guarantee default switch closure to the USB position, the SEL[0:1] pins should be tied to GND with a weak pull-down resistor (3 MΩ) to minimize static current draw.

Pin Configuration

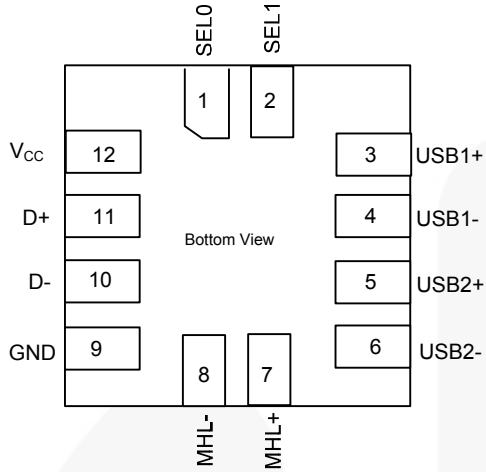


Figure 3. Pin Assignments

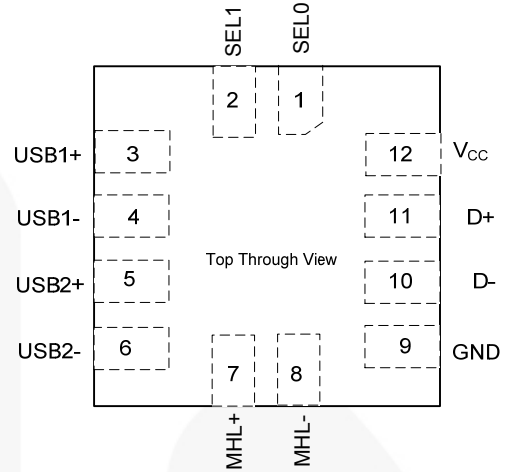


Figure 4. Top Through View

Pin Definitions

Pin#	Name	Description
1	SEL0	Data Switch Select
2	SEL1	Data Switch Select
3	USB1+	USB Differential Data (Positive) – Source 1
4	USB1-	USB Differential Data (Negative) – Source 1
5	USB2+	USB Differential Data (Positive) – Source 2
6	USB2-	USB Differential Data (Negative) – Source 2
7	MHL+	MHL Differential Data (Positive)
8	MHL-	MHL Differential Data (Negative)
9	GND	Ground
10	D-	Data Switch Output (Positive)
11	D+	Data Switch Output (Negative)
12	V _{CC}	Device Power from System

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V _{CC}	Supply Voltage		-0.5	6.0	V
V _{CNTRL}	DC Input Voltage (SEL[1:0]) ⁽²⁾		-0.5	V _{CC}	V
V _{SW} ⁽³⁾	DC Switch I/O Voltage ⁽²⁾	USB	-0.50	V _{CC}	V
		MHL	-0.50	V _{CC}	
I _{IK}	DC Input Diode Current		-50		mA
I _{OUT}	Switch DC Output Current (Continuous)	USB		60	mA
		MHL		60	mA
I _{OUTPEAK}	Switch DC Output Peak Current (Pulsed at 1m Duration, <10% Duty Cycle)	USB		150	mA
		MHL		150	mA
T _{STG}	Storage Temperature		-65	+150	°C
MSL	Moisture Sensitivity Level (JEDEC J-STD-020A)			1	
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		4	kV
	IEC 61000-4-2, Level 4, for D+/D- and V _{CC} Pins ⁽⁴⁾	Contact		8	
	IEC 61000-4-2, Level 4, for D+/D- and V _{CC} Pins ⁽⁴⁾	Air		15	
	Charged Device Model, JESD22-C101			2	

Notes:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
- V_{SW} refers to analog data switch paths (USB1, MHL, and USB2).
- Testing performed in a system environment using TVS diodes.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	2.5	4.5	V
t _{RAMP(VCC)}	Power Supply Slew Rate	100	1000	µs/V
θ _{JA}	Thermal Resistance		230	C°/W
V _{CNTRL}	Control Input Voltage (SEL[1:0]) ⁽⁵⁾	0	4.5	V
V _{SW(USB)}	Switch I/O Voltage (USB1/USB2 Switch Paths)	-0.5	3.6	V
V _{SW(MHL)}	Switch I/O Voltage (MHL Switch Path)	1.65	3.45	V
T _A	Operating Temperature	-40	+85	°C

Note:

- The control inputs must be held HIGH or LOW; they must not float.

DC Electrical Characteristics

All typical values are at $T_A=25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	$I_{IN}=-18\text{ mA}$	2.5			-1.2	V
V_{IH}	Control Input Voltage, High SEL[1:0]		2.5 to 4.5	1.0			V
V_{IL}	Control Input Voltage, Low SEL[1:0]		2.5 to 4.5			0.5	V
I_{IN}	Control Input Leakage, SEL[1:0]	$V_{SW}=0$ to 3.6 V, $V_{CNTRL}=0$ to V_{CC}	4.5	-0.5		0.5	μA
$I_{OZ(MHL)}$	Off-State Leakage for Open MHL Data Paths	$V_{SW}=1.65 \leq \text{MHL} \leq 3.45\text{ V}$, SEL[1:0]= V_{CC}	4.5	-0.5		0.5	μA
$I_{OZ(USB)}$	Off-State Leakage for Open USB Data Paths	$V_{SW}=0 \leq \text{USB} \leq 3.6\text{ V}$, SEL[1:0]= V_{CC}	4.5	-0.5		0.5	μA
$I_{CL(MHL)}$	On-State Leakage for Closed MHL Data Paths ⁽⁶⁾	$V_{SW}=1.65 \leq \text{MHL} \leq 3.45\text{ V}$, SEL0=GND, SEL1= V_{CC} , Other Side of Switch Float	4.5	-0.5		0.5	μA
$I_{CL(USB)}$	On-State Leakage for Closed USB Data Paths ⁽⁶⁾	$V_{SW}=0 \leq \text{USB} \leq 3.6\text{ V}$, SEL[1:0]=GND or SEL1=GND, SEL0= V_{CC} , Other Side of Switch Float	4.5	-0.5		0.5	μA
I_{OFF}	Power-Off Leakage Current (All I/O Ports)	$V_{SW}=0\text{ V}$ or 3.6 V, Figure 5	0	-0.5		0.5	μA
$R_{ON(USB)}$	HS Switch On Resistance (USB to D Path)	$V_{SW}=0.4\text{ V}$, $I_{ON}=-8\text{ mA}$, SEL[1:0]=GND or SEL1=GND, SEL0= V_{CC} , Figure 6	2.5		3.9	6.5	Ω
$R_{ON(MHL)}$	HS Switch On Resistance (MHL to D Path)	$V_{SW}=V_{CC}-1050\text{ mV}$, SEL0=GND, SEL1= V_{CC} , $I_{ON}=-8\text{ mA}$, Figure 6	2.5		5		Ω
$\Delta R_{ON(MHL)}$	Difference in R_{ON} Between MHL Positive-Negative	$V_{SW}=V_{CC}-1050\text{ mV}$, SEL0=GND, SEL1= V_{CC} , $I_{ON}=-8\text{ mA}$, Figure 6,	2.5		0.03		Ω
$\Delta R_{ON(USB)}$	Difference in R_{ON} Between USB Positive-Negative	$V_{SW}=0.4\text{ V}$, $I_{ON}=-8\text{ mA}$, SEL[1:0]=GND or SEL1=GND, SEL0= V_{CC} Figure 6	2.5		0.22		Ω
$R_{ONF(MHL)}$	Flatness for R_{ON} MHL Path	$V_{SW}=1.65$ to 3.45 V, SEL0=GND, SEL1= V_{CC} , $I_{ON}=-8\text{ mA}$, Figure 6	2.5		1		Ω
I_{CC}	Quiescent Current	$V_{CNTRL}=0$ or 4.5 V, $I_{OUT}=0$	4.5			30	μA
I_{CCT}	Delta Increase in Quiescent Current per Control Pin	$V_{CNTRL}=1.65\text{ V}$, $I_{OUT}=0$	4.5			18	μA
		$V_{CNTRL}=2.5\text{ V}$, $I_{OUT}=0$	4.5			10	

Note:

6. For this test, the data switch is closed with the respective switch pin floating.

AC Electrical Characteristics

All typical values are for $V_{CC}=3.3\text{ V}$ and $T_A=25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
t_{ONUSB}	USB Turn-On Time, SEL[1:0] to Output	$R_L=50\ \Omega$, $C_L=5\ \text{pF}$, $V_{SW(USB)}=0.8\ \text{V}$, $V_{SW(MHL)}=3.3\ \text{V}$, Figure 7, Figure 8	2.5 to 3.6		445	600	ns
t_{OFFUSB}	USB Turn-Off Time, SEL[1:0] to Output	$R_L=50\ \Omega$, $C_L=5\ \text{pF}$, $V_{SW(USB)}=0.8\ \text{V}$, $V_{SW(MHL)}=3.3\ \text{V}$, Figure 7, Figure 8	2.5 to 3.6		445	600	ns
t_{ONMHL}	MHL Turn-On Time, SEL[1:0] to Output	$R_L=50\ \Omega$, $C_L=5\ \text{pF}$, $V_{SW(USB)}=0.8\ \text{V}$, $V_{SW(MHL)}=3.3\ \text{V}$, Figure 7, Figure 8	2.5 to 3.6		445	600	ns
t_{OFFMHL}	MHL Turn-Off Time, SEL[1:0] to Output	$R_L=50\ \Omega$, $C_L=5\ \text{pF}$, $V_{SW(USB)}=0.8\ \text{V}$, $V_{SW(MHL)}=3.3\ \text{V}$, Figure 7, Figure 8	2.5 to 3.6		445	600	ns
t_{PD}	Propagation Delay ⁽⁷⁾	$C_L=5\ \text{pF}$, $R_L=50\ \Omega$, Figure 7, Figure 9	2.5 to 3.6		0.25		ns
t_{BBM}	Break-Before-Make Time ⁽⁷⁾	$R_L=50\ \Omega$, $C_L=5\ \text{pF}$, $V_{ID}=V_{MHL}=3.3\ \text{V}$, $V_{USB}=0.8\ \text{V}$, Figure 11	2.5 to 3.6		85		ns
$O_{IRR(MHL)}$	Off Isolation ⁽⁷⁾	$V_S=1\ \text{V}_{pk-pk}$, $R_L=50\ \Omega$, $f=240\ \text{MHz}$, Figure 12	2.5 to 3.6		-41		dB
$O_{IRR(USB)}$		$V_S=400\ \text{mV}_{pk-pk}$, $R_L=50\ \Omega$, $f=240\ \text{MHz}$, Figure 12	2.5 to 3.6		-36		dB
$Xtalk_{MHL}$	Non-Adjacent Channel ⁽⁷⁾ Crosstalk	$V_S=1\ \text{V}_{pk-pk}$, $R_L=50\ \Omega$, $f=240\ \text{MHz}$, Figure 13	2.5 to 3.6		-41		dB
$Xtalk_{USB}$		$V_S=400\ \text{mV}_{pk-pk}$, $R_L=50\ \Omega$, $f=240\ \text{MHz}$, Figure 13	2.5 to 3.6		-37		dB
BW	Differential -3db Bandwidth ⁽⁷⁾	$V_{IN}=1\ \text{V}_{pk-pk}$, MHL Path, Common Mode Voltage = $V_{CC} - 1.1\ \text{V}$, $R_L=50\ \Omega$, $C_L=0\ \text{pF}$, Figure 14	2.5 to 3.6		1.87		GHz
		$V_{IN}=400\ \text{mV}_{pk-pk}$, USB Path, Common Mode Voltage = $0.2\ \text{V}$, $R_L=50\ \Omega$, $C_L=0\ \text{pF}$, Figure 14			1.47		

Note:

7. Guaranteed by characterization.

USB High-Speed AC Electrical Characteristics

Typical values are at $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

Symbol	Parameter	Condition	$V_{CC}(V)$	Typ.	Unit
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output ⁽⁸⁾	$C_L=5\text{ pF}$, $R_L=50\ \Omega$, Figure 9	3.0 to 3.6	7	ps
t_J	Total Jitter ⁽⁸⁾	$R_L=50\ \Omega$, $C_L=5\text{ pF}$, $t_R=t_F=500\text{ ps}$ (10-90%) at 480 Mbps, PN7	3.0 to 3.6	18	ps

Note:

8. Guaranteed by characterization.

MHL AC Electrical Characteristics

Typical values are at $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

Symbol	Parameter	Condition	$V_{CC}(V)$	Typ.	Unit
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output ⁽⁹⁾	$R_{PU}=50\ \Omega$ to V_{CC} , $C_L=0\text{ pF}$	3.0 to 3.6	3	ps
t_J	Total Jitter ⁽⁹⁾	$f=2.25\text{ Gbps}$, PN7, $R_{PU}=50\ \Omega$ to V_{CC} , $C_L=0\text{ pF}$	3.0 to 3.6	23	ps

Note:

9. Guaranteed by characterization.

Capacitance

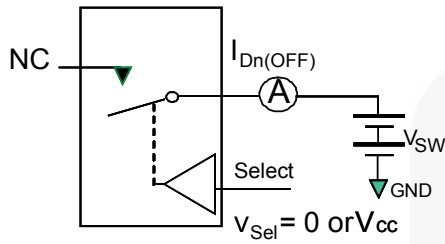
Typical values are at $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

Symbol	Parameter	Condition	Typ.	Max.	Unit
C_{IN}	Control Pin Input Capacitance ⁽¹⁰⁾	$V_{CC}=0\text{ V}$, $f=1\text{ MHz}$	2.5		pF
$C_{ON(USB)}$	USB Path On Capacitance ⁽¹⁰⁾	$V_{CC}=3.3\text{ V}$, $f=240\text{ MHz}$, Figure 15	6.75		pF
$C_{OFF(USB)}$	USB Path Off Capacitance ⁽¹⁰⁾	$V_{CC}=3.3\text{ V}$, $f=240\text{ MHz}$, Figure 13	2.5		pF
$C_{ON(MHL)}$	MHL Path On Capacitance ⁽¹⁰⁾	$V_{CC}=3.3\text{ V}$, $f=240\text{ MHz}$, Figure 15	4.6		pF
$C_{OFF(MHL)}$	MHL Path Off Capacitance ⁽¹⁰⁾	$V_{CC}=3.3\text{ V}$, $f=240\text{ MHz}$, Figure 13	2.5		pF

Note:

10. Guaranteed by characterization.

Test Diagrams



**Each switch port is tested separately

Figure 5. Off Leakage

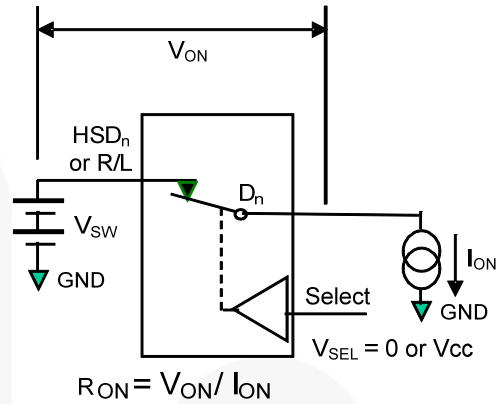
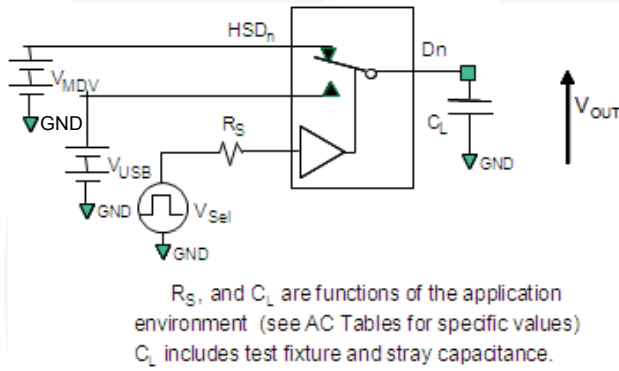


Figure 6. On Resistance



R_S and C_L are functions of the application environment (see AC Tables for specific values)
 C_L includes test fixture and stray capacitance.

Figure 7. AC Test Circuit Load

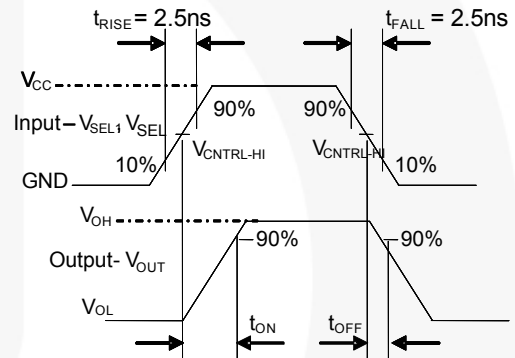


Figure 8. Turn-On / Turn-Off Waveforms

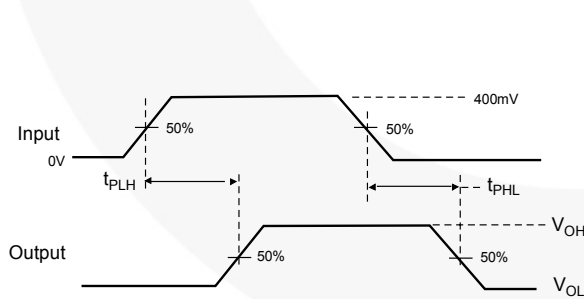


Figure 9. Propagation Delay ($t_{rF} = 500ps$)

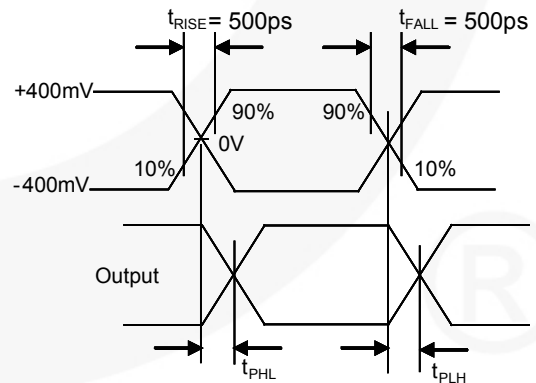


Figure 10. Intra-Pair Skew Test $t_{SK(P)}$

Test Diagrams

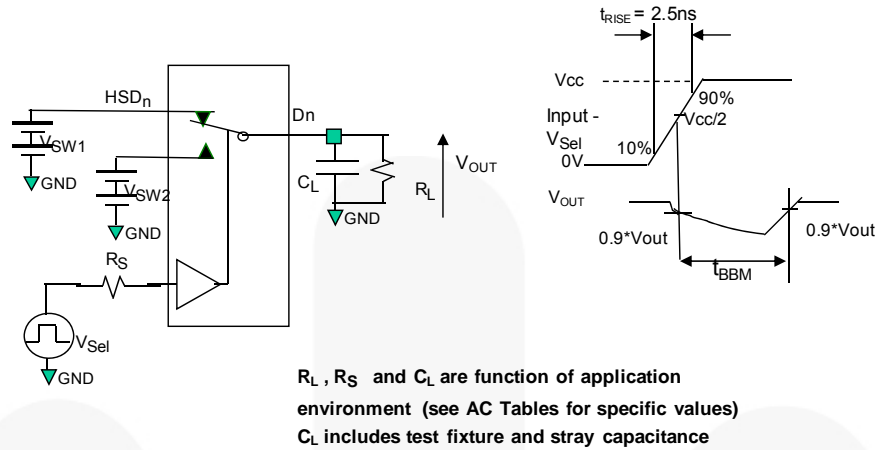


Figure 11. Break-Before-Make Interval Timing

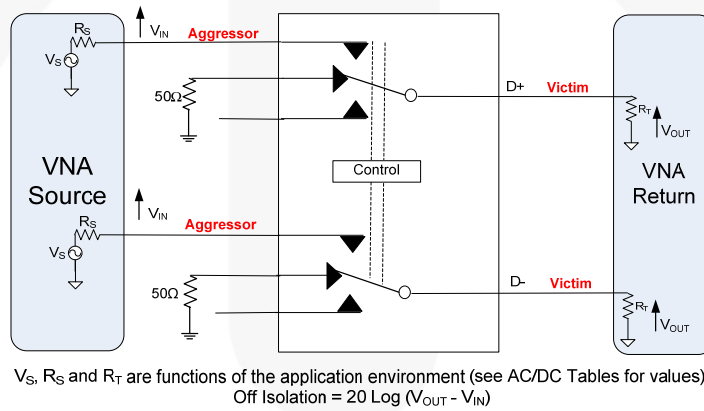


Figure 12. Channel Off Isolation (SDD21)

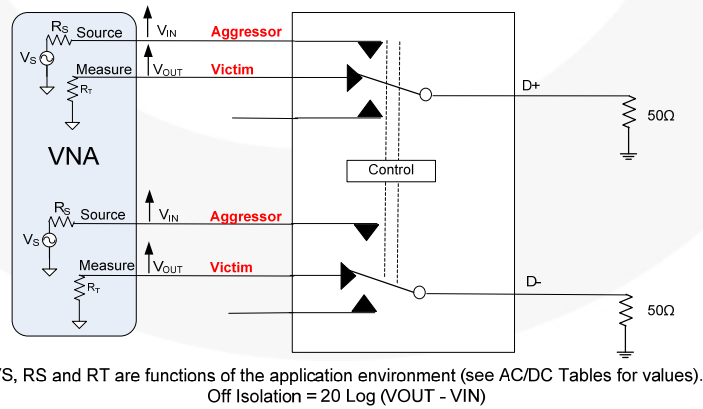


Figure 13. Non-Adjacent Channel-to-Channel Crosstalk (SDD21)

Test Diagrams

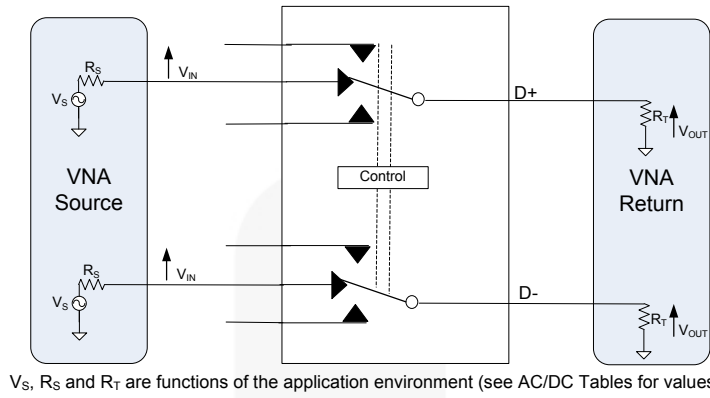


Figure 14. Insertion Loss (SDD21)

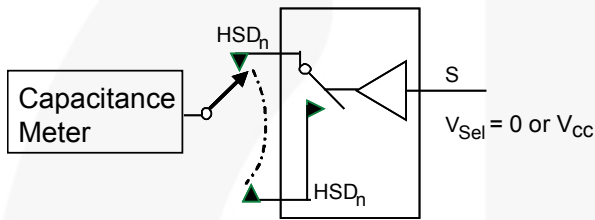


Figure 15. Channel Off Capacitance

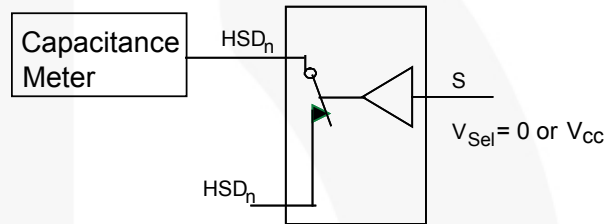


Figure 16. Channel On Capacitance

Note:

11. HSD_n refers to the high-speed data USB or MHL paths.

Functional Description

Insertion Loss

One of the key advantages of using the FSA3031 in mobile digital video applications is the small amount of insertion loss experienced by the received signal as it passes through the switch.

This results in minimal degradation of the received eye. One of the ways to measure the quality of the high data rate channels is using balanced ports and four-port differential S-parameter analysis, particularly SDD21.

Bandwidth is measured using the S-parameter SDD21 methodology. Figure 17 exhibits the 1.87 GHz (-3 db) BW of the MHL path, while Figure 18 exhibits the 1.47 GHz (-3 db) BW of the USB paths.

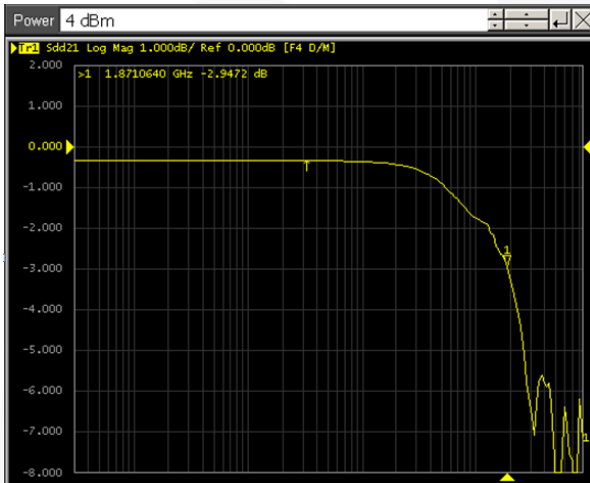


Figure 17. MHL Path SDD21 Insertion Loss Curve

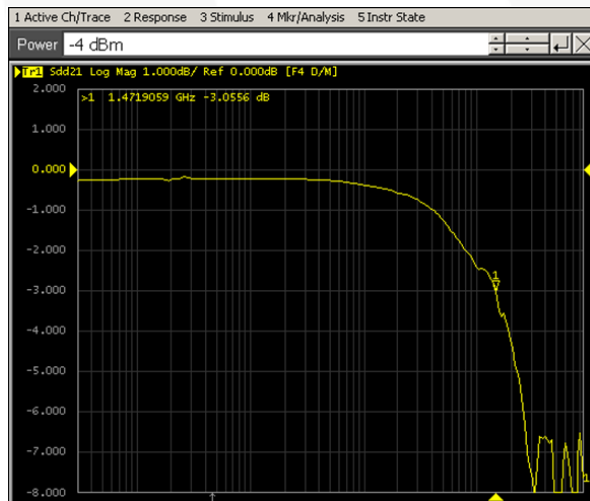


Figure 18. USB Path SDD21 Insertion Loss Curve

Typical Application

Figure 19 shows utilizing the VBAT connection from the micro-USB connector. The 3M resistors are used to ensure, for manufacturing test via the micro-USB connector, that the FSA3031 configures for connectivity to the baseband or application processor.

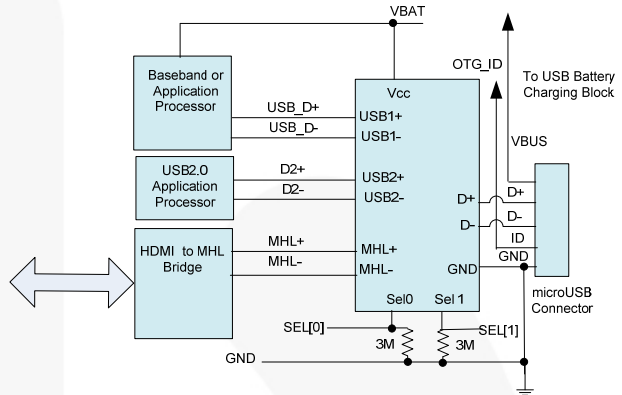
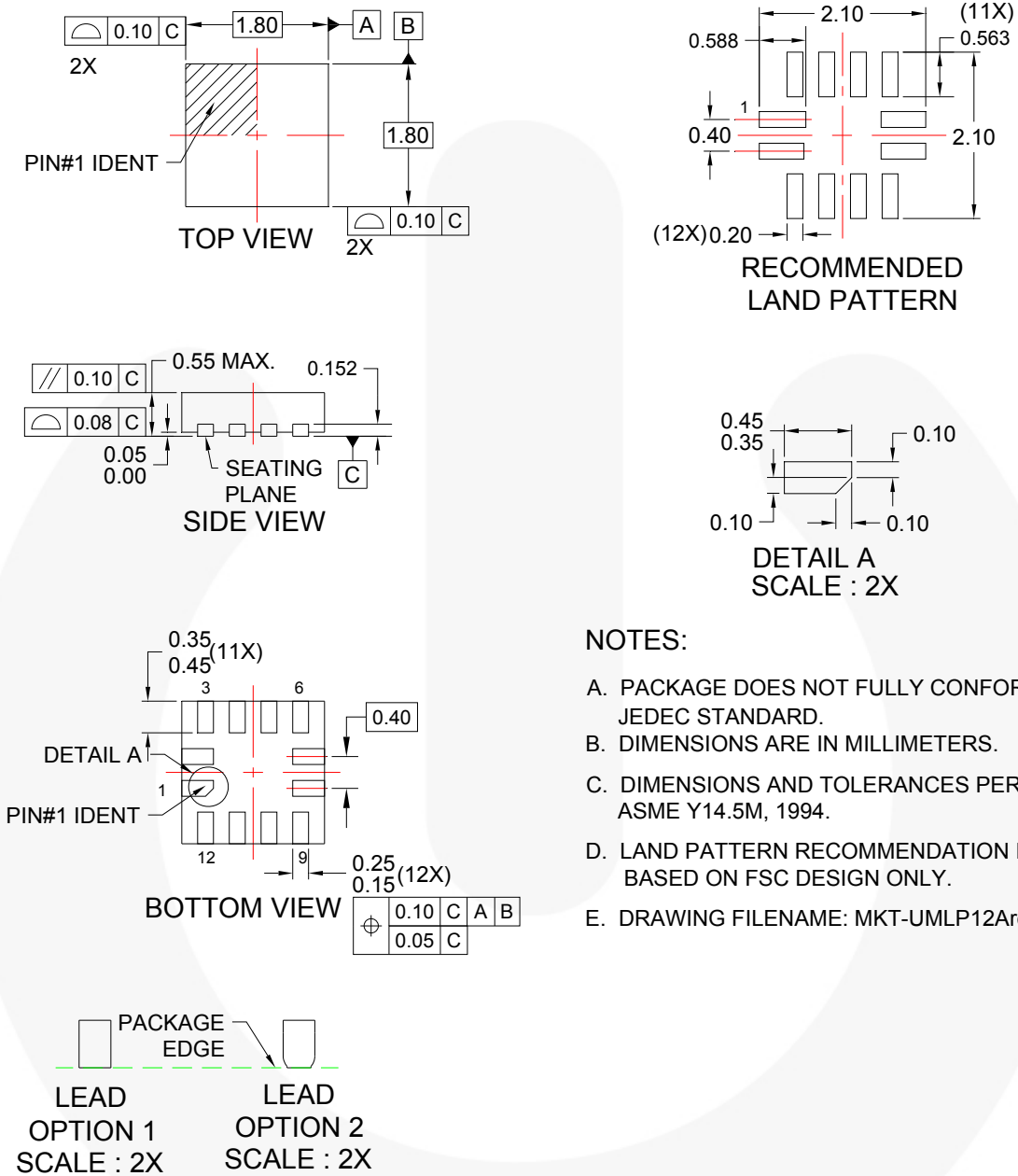


Figure 19. Typical Application

Physical Dimensions



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
- E. DRAWING FILENAME: MKT-UMLP12Arev4.

Figure 20. 12-Lead, Ultrathin Molded Leadless Package (UMLP)






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| BitSiC™ | GreenBridge™ | QFET® | TinyBuck™ |
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