HMC1023LP5E

v01.0113

72 MHz DUAL PROGRAMMABLE LOW PASS FILTER WITH DRIVER

Typical Applications

The HMC1023LP5E is ideal for:

- Baseband filtering before or after data converters for point-to-point fixed wireless and cellular infrastructure transceivers
- Software defined radio applications
- Anti-aliasing and reconstruction filters
- Test and measurement equipment
- ADC driver applications

Features

Low Noise Figure: 10 dB

High linearity:
In-Band Output IP3 > +30 dBm
In-Band Output IP2 > +60 dBm

Pre-programmed and/or Programmable Bandwidth: 5 MHz to 72 MHz. (Please see HMC1023LP5E Ordering Information)

Exceptional 3 dB Bandwidth Accuracy: ±2.5%

Programmable Gain: 0 or 10 dB

Integrated ADC Driver Amplifier

6th order Butterworth Magnitude & Phase Response

Automatic Filter Calibration

Externally Controlled Common Mode Output Level

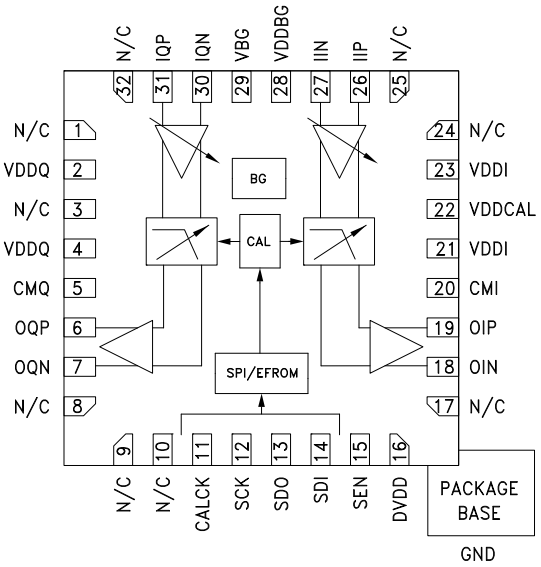
Filter Bypass Option

Pin & Register Compatible to HMC900LP5E

Read/Write Serial Port Interface (SPI)

32 Lead 5x5 mm SMT Package 25 mm²

Functional Diagram



General Description

The HMC1023LP5E is a 6th order, programmable bandwidth, fully calibrated, dual low pass filter. It features programmable 0 or 10 dB gain and supports arbitrary bandwidths from 5 MHz to 72 MHz. When calibrated, the bandwidth is accurate to +/-2.5%. Built-in filter bypass option enables wider bandwidths while maintaining programmed gain and common mode control settings.

Integrated ADC driver, programmable input impedance, and adjustable output common mode voltage from 0.9 V to 3 V with 2 Vppd signal, or lower than 0.9 V common mode with lower signal swing enables simple interface while achieving maximum performance. Programmable bias settings enable performance/power dissipation trade-off optimized for each application.

Filter calibration is accomplished with any reference clock rate from 20 to 80 MHz. One time programmable (OTP) memory offers unsurpassed flexibility allowing the user “set and forget” parameters like gain and bandwidth setting.

Housed in a compact 5x5 mm SMT QFN package, the HMC1023LP5E is pin and register compatible to the existing HMC900LP5E programmable bandwidth Low Pass Filter. It requires minimal external components and provides a low cost alternative to more complicated switched discrete filter architectures.

The 6th order Butterworth transfer function delivers superior stop band rejection while maintaining both a flat passband and minimal group delay variation.

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Table 1. Electrical Specifications

T_A = +25°C, VDDI, VDDQ, VDDCAL, VDDBG, DVDD = 5V +/-5%, GND = 0V, 400 Ω load unless otherwise stated.

Parameter	Conditions	Min.	Typ.	Max.	Units
Analog Performance					
Passband Gain [1]	min gain setting max gain setting		0 10		dB dB
3 dB corner frequency (fc) Programmable to any frequency in this range	[1]	5		72	MHz
	Bypass mode	75	100		MHz
3 dB corner frequency variation	uncalibrated			± 20	%
	calibrated		±2.5	± 3.5	%
3 dB corner frequency variation vs temperature	over -40°C to +85°C			±0.03	% / °C
Max passband gain error[2]	vs ideal 6th order LPF H(s)			±0.5	dB
Max passband group delay variation (group delay * 3 dB frequency fc) e.g. for 1.0 dB BW of 40 MHz (fc ~ 44.9 MHz): max group delay variation = 0.400/ 44.9 MHz = 8.9 ns	at 0.1 dB BW (~0.73 fc)			0.250	
	at 0.5 dB BW (~0.83 fc)			0.350	
	at 1.0 dB BW (~ 0.89 fc)			0.400	
	at 3.0 dB BW (at fc)			0.400	
Output Noise (f = 1 MHz)	min gain, fc = 5 MHz		22		nV/rtHz
	min gain, fc = 28 MHz		22		nV/rtHz
	max gain fc = 5 MHz		25		nV/rtHz
	max gain, fc = 28 MHz		25		nV/rtHz
Output noise (f > 10*fc)	min gain, fc = 5 MHz		8		nV/rtHz
	max gain, fc = 5 MHz		8		nV/rtHz
	min gain fc = 28 MHz		8		nV/rtHz
	max gain, fc = 28 MHz		8		nV/rtHz
Noise Figure (100 Ω source)	min gain		25		dB
	max gain		17		dB
Noise Figure (1 kΩ source)	min gain		19		dB
	max gain		12		dB
Input referred Passband IM3	half scale tones at 0.8fc and 0.6fc fc = 20 MHz fc = 72 MHz[2]		 -60 -50		 dBc dBc
Input referred Out of Band IM3	half scale tones at 1.2fc and 1.6fc. IM3 product at 0.8fc fc = 20 MHz fc = 72 MHz [2]		 -60 -50		 dBc dBc
Input referred Out of Band IM3	half scale tones at 2fc and 3fc. IM3 product at 0.5fc fc = 20 MHz fc = 72 MHz [2]		 -50 -45		 dBc dBc
Output IP3 (inband)	half scale tones at 0.8fc and 0.6fc fc = 20 MHz fc = 72 MHz	 25 17	 30 20		 dBm dBm
Output IP3 (out of band)	half scale tones at 1.2fc and 1.6fc. IM3 product at 0.8fc fc = 20 MHz fc = 72 MHz [2]	 25 17	 30 20		 dBm dBm
Output IP3 (out of band)	half scale tones at 2fc and 3fc. IM3 product at fc fc = 20 MHz fc = 72 MHz[2]	 25 17	 30 20		 dBm dBm
Output IP2 (inband)	half scale tones at 0.8fc and 0.6fc IM2 product at 0.2fc fc = 20 MHz fc = 72 MHz [2]	 55 55	 60 60		 dBm dBm

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Electrical Specifications, TA = +25°C *(Continued)*

Parameter	Conditions	Min.	Typ.	Max.	Units
Output IP2 (out of band)[2]	half scale tones at 1.2fc and 1.6fc. IM2 product at 0.4fc	60	65		dBm
Sideband Suppression (Uncalibrated)	complex signal measured at 0.8fc vs -0.8fc	35	45		dB
I/Q Channel Balance magnitude phase			 0.04 0.5		 dB °
I/Q Channel Isolation		60	80		dB
Analog I/O					
Differential Input Impedance	Programmable		1000 / 400 / 100		Ω
Full Scale Differential Input (400 Ω Differential Load)	min gain			2	Vppd
	max gain			0.613	Vppd
Full Scale Differential Input (100 Ω Differential Load)	min gain			0.5	Vppd
	max gain			0.156	Vppd
Input Common Mode Voltage Range		1		4	V
Full Scale Differential Output	400 Ω Differential Load			2	Vppd
Full Scale Differential Output	100 Ω Differential Load			0.5	Vppd
Output Voltage Range		0.5		Vdd-0.5	V
Output Common Mode Voltage Range		0.9		3	V
Digital I/O					
CALCK Frequency	Use doubler mode for clocks between 20 MHz and 40 MHz	20	40	80	MHz
CALCK Duty Cycle		40	50	60	%
SCLK Frequency			20	30	MHz
Digital Input Low Level (VIL)				0.4	V
Digital Input High Level (VIH)		1.5			V
Digital Output Low Level (VOL)				0.4	V
Digital Output High Level (VOH)		Vdd - 0.4			
Power Supply	Analog & Digital Supplies	4.75	5	5.25	V
Supply Current	Dependent on Bias		240		mA
Power on Reset			250		us

[1] The attenuation of the filter transfer function can be calculated directly at any frequency f as: attenuation = $10*\log_{10}(1+(f/f_0)^{\wedge(2*6)})$, where f_0 is the 3 dB bandwidth or corner frequency for the filter. Similarly, for a given maximum attenuation and 3 dB bandwidth, f_0, the frequency at which the attenuation is achieved can be calculated as: $f=(10^{\wedge(attenuation/10)} -1)^{\wedge(1/(2*6))} * f_0$. Note that for a 6th order Butterworth filter the 1 dB bandwidth is at ~89% of the filter bandwidth and 0.5 dB bandwidth is at 84% of the filter bandwidth.

[2] Specified distortion is measured with opamp_bias (Reg 02h[1:0]) settings recommended in Table 9. .

Table 2. Test Conditions

Unless otherwise specified, the following test conditions were used

Parameter	Condition
Temperature	+25 °C
Reg 06h Setting	150
Gain Setting	0 dB
bias settings (opamp_bias Reg 02h[1:0]/ drvr_bias Reg 02h[3:2])	00/10
Input Signal Level	2 Vppd
Input/Output Common Mode Level	2V
Output Load	200 Ω / Output
Supply	Analog: +5V, Digital +5V

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Figure 1. Filter Attenuation (all Bandwidths) [1]

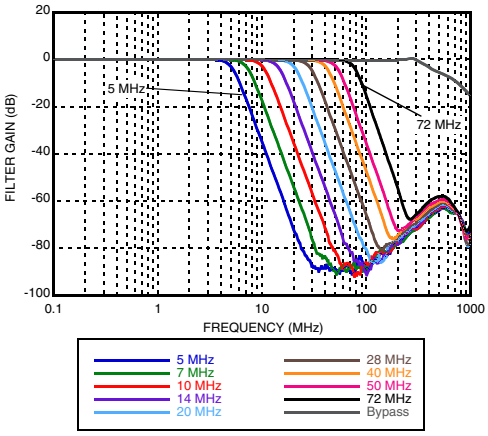


Figure 2. Filter Passband Gain Response

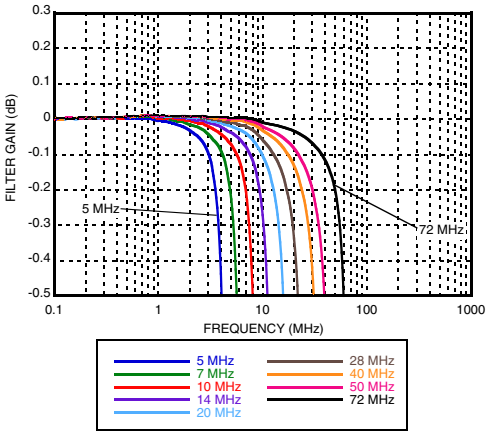


Figure 3. Filter Attenuation, 10dB Gain [1]

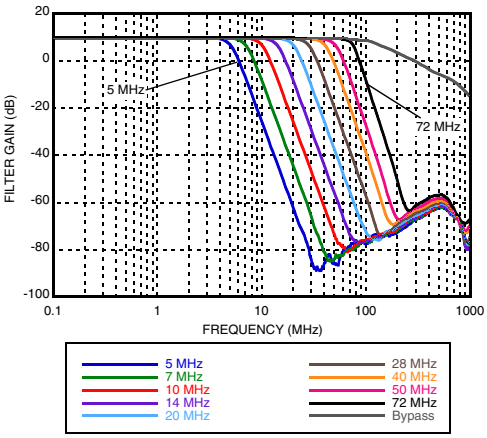


Figure 4. Filter 3 dB Cutoff vs Temperature, 10 MHz Bandwidth

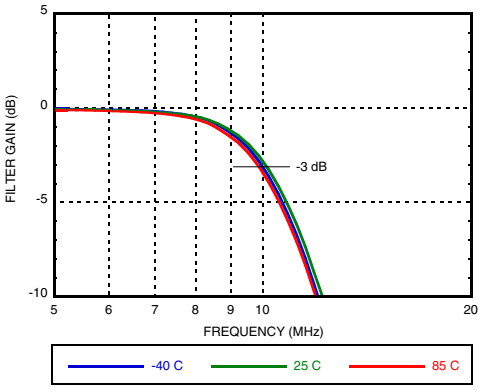


Figure 5. Noise Figure, 100 Ω Source Impedance, 1 kΩ Impedance Selected [2]

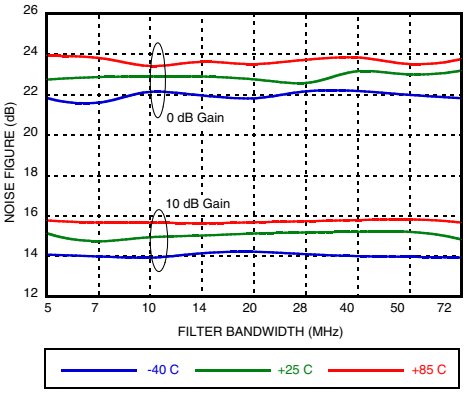
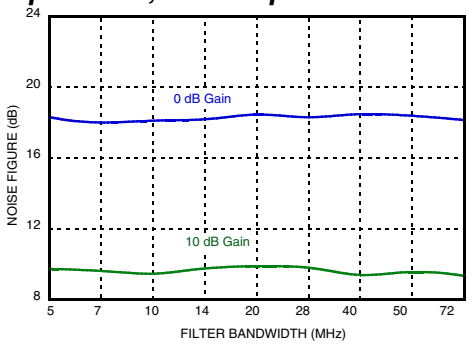


Figure 6. Noise Figure, 1 kΩ Source Impedance, 1 kΩ Impedance Selected [2]



[1] Degrated stop-band rejection at frequencies > 100 MHz caused by the test fixture.
[2] 1 kΩ input impedance into the HMC1023LP5E selected by writing Reg 02h[10]=0 and Reg 01h[9] = 0.

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Figure 7. Noise Figure, 1 kΩ Source Impedance, 100 Ω Impedance Selected

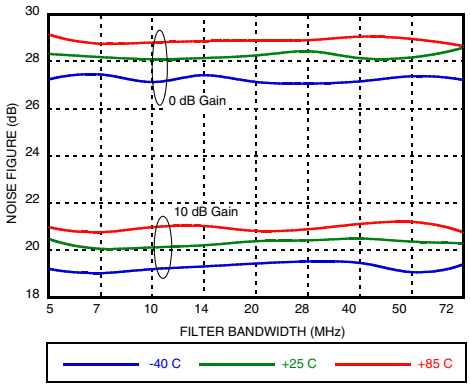


Figure 8. Filter Output Noise [3]

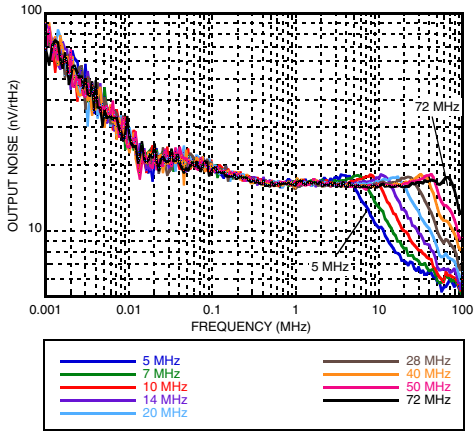


Figure 9. Uncalibrated Sideband Rejection, 0 dB Gain

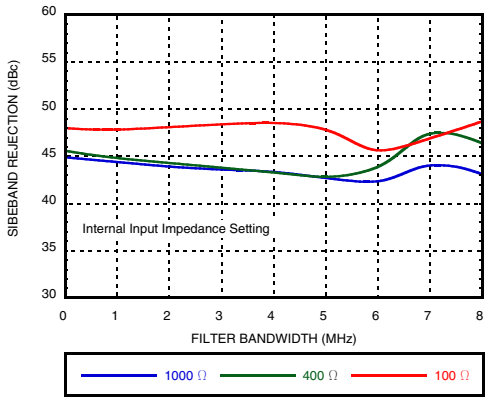


Figure 10. Uncalibrated Sideband Rejection, 10 dB Gain

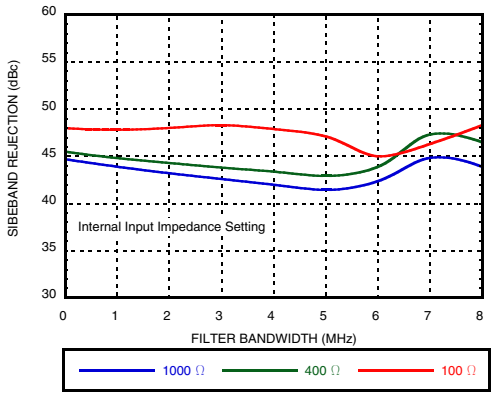


Figure 11. Arbitrary Bandwidth Setting 3 dB Cutoff Frequency Error [5]

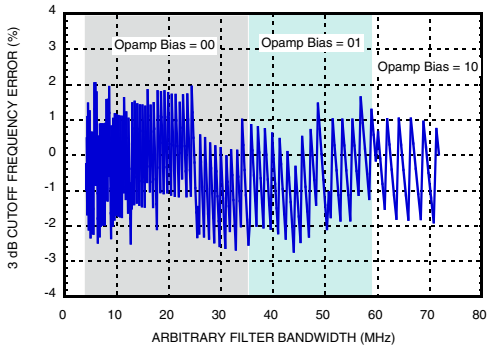
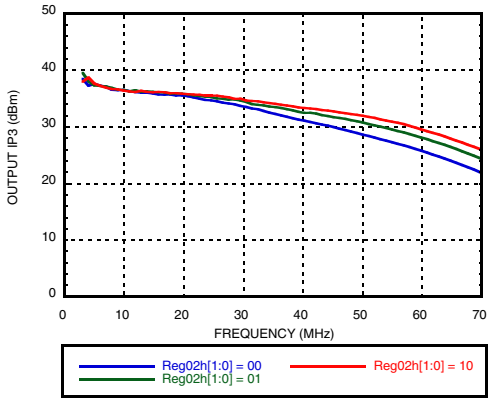


Figure 12. Output IP3, 72 MHz Bandwidth Setting, 0 dB Gain [6]



[3] 100 Ω source impedance used, and input impedanceo of HMC1023LP5E set to 1 kΩ
[4] 100 Ω input impedance into the HMC1023LP5E selected by writing Reg 02h[10]=1.
[5] Used recommended OpAmp bias settings (Reg 02h[1:0]) in Table 9.
[6] OIP3 and OIP2 measured from 100 Ω differential source into 400 Ω differential load. Used recommended OpAmp bias settings (Reg 02h[1:0]) in Table 9. OIP3 and OIP2 measurements can be translated from dBm into dBVrms as follows: IPx [dBVrms] = IPx [dBm] -4 dB.

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Figure 13. Output IP2, 72 MHz Bandwidth Setting, 0 dB Gain [7]

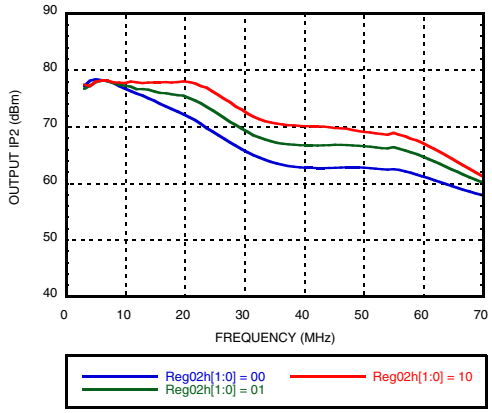


Figure 14. Output IP3, Filter Bypass Enabled, 0 dB Gain [7]

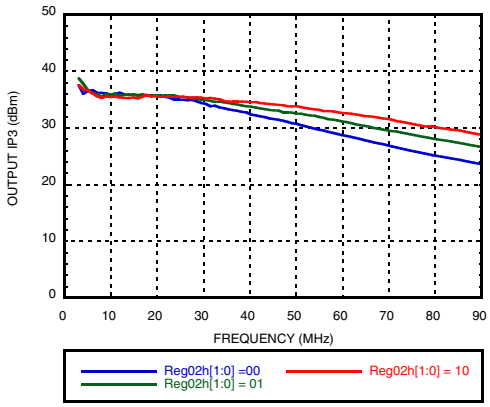


Figure 15. Output IP2, Filter Bypass Mode Enabled, 0 dB Gain [7]

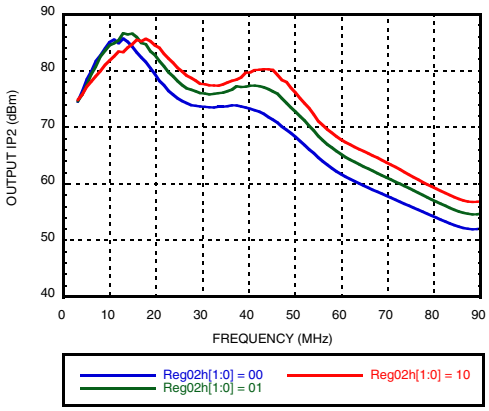


Figure 16. Output IP3, Filter Bypass Enabled, 10 dB Gain [7]

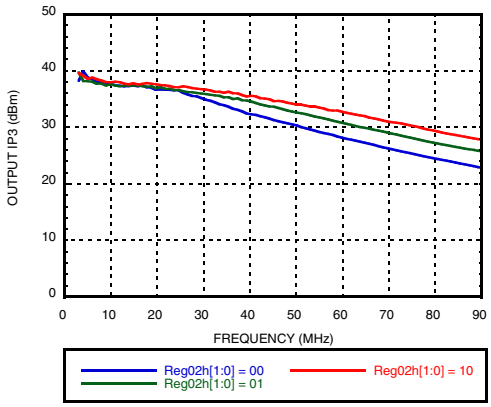


Figure 17. Output IP2, Filter Bypass Enabled, 10 dB Gain [7]

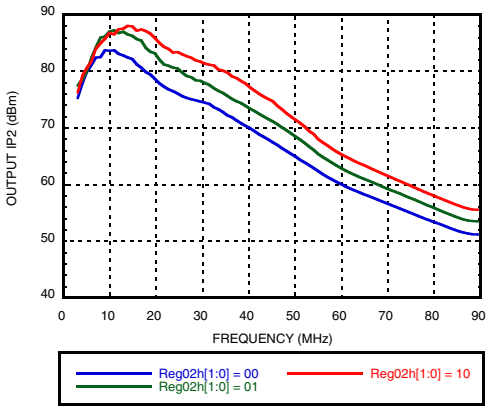
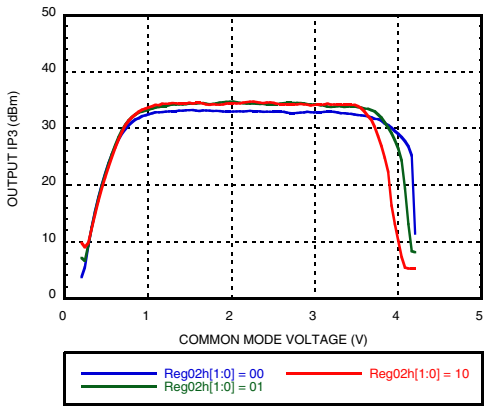


Figure 18. Output IP3 vs Output Common Mode Voltage, 30 MHz Input [8]



[7] OIP3 and OIP2 measured from 100 Ω differential source into 400 Ω differential load. Used recommended OpAmp bias settings (Reg 02h[1:0]) in Table 9. OIP3 and OIP2 measurements can be translated from dBm into dBVrms as follows: IPx [dBVrms] = IPx [dBm] -4 dB.
[8] 72 MHz Filter Bandwidth Selected. OIP3 and OIP2 measured from 100 Ω differential source into 400 Ω differential load. OIP3 and OIP2 measurements can be translated from dBm into dBVrms as follows: IPx [dBVrms] = IPx [dBm] -4 dB.

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Figure 19. Output IP2 vs Output Common Mode Voltage, 30 MHz Input [9]

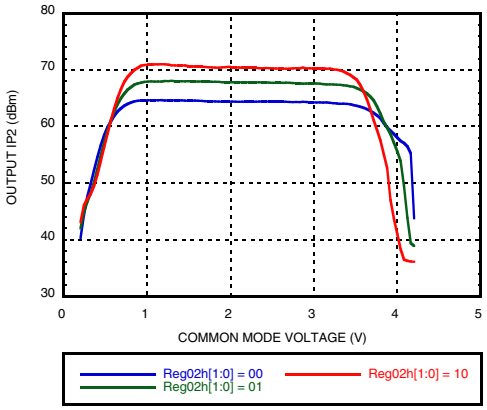


Figure 20. Output IP3 vs Output Common Mode Voltage, 50 MHz Input [9]

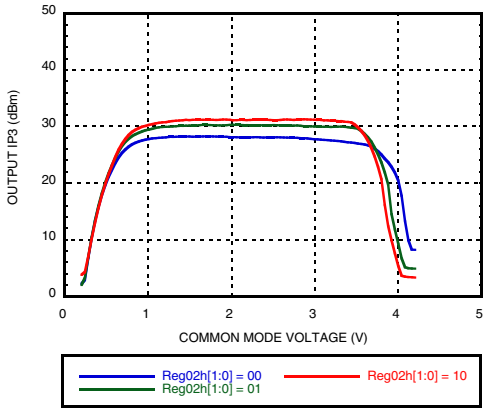


Figure 21. Output IP2 vs Output Common Mode Voltage, 50 MHz Input [9]

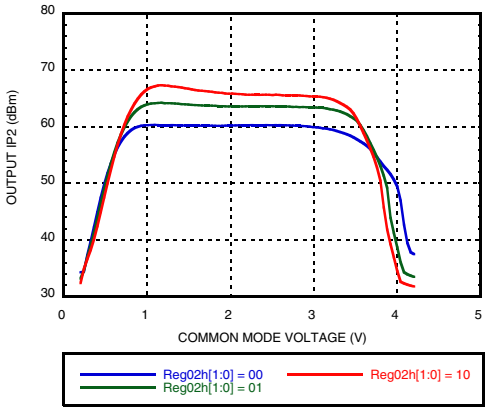


Figure 22. Output IP3 vs Output Common Mode Voltage, 70 MHz Input [9]

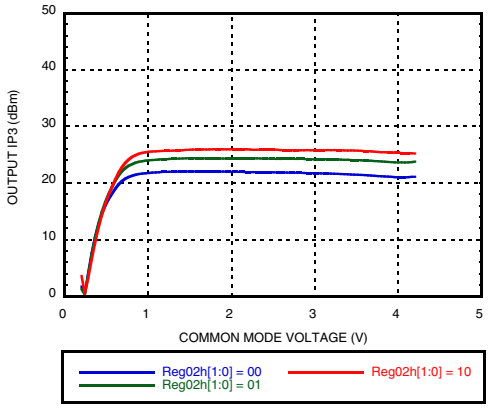


Figure 23. Output IP2 vs Output Common Mode Voltage, 70 MHz Input [9]

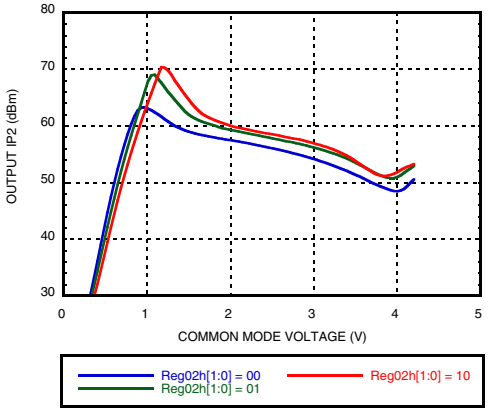
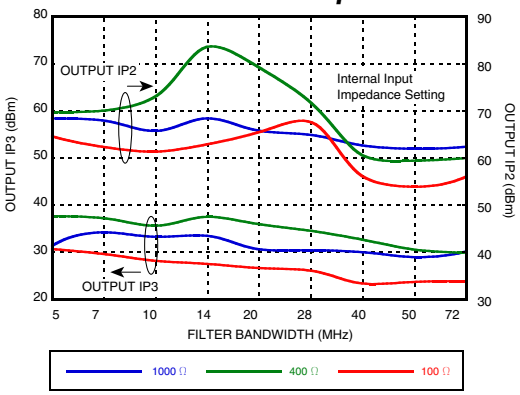


Figure 24. In-band Output IP3 & Output IP2 vs Filter Bandwidth & Impedance [10]



[9] 72 MHz Filter Bandwidth selected. OIP3 and OIP2 measured from 100 Ω differential source into 400 Ω differential load. OIP3 and OIP2 measurements can be translated from dBm into dBVrms as follows: IPx [dBVrms] = IPx [dBm] -4 dB

[10] OIP3 and OIP2 measured from 100 Ω differential source into 400 Ω differential load. Used recommended OpAmp bias settings (Reg 02h[1:0]) in Table 9. OIP3 and OIP2 measurements can be translated from dBm into dBVrms as follows: IPx [dBVrms] = IPx [dBm] -4 dB.

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72 MHz DUAL PROGRAMMABLE LOW PASS FILTER WITH DRIVER

Figure 25. In-band Output IP3 & Output IP2 vs Bandwidth & Temperature [11]

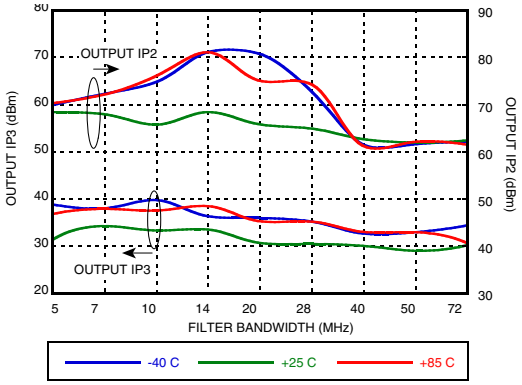


Figure 26. 5 MHz Bandwidth Filter Magnitude and Group Delay

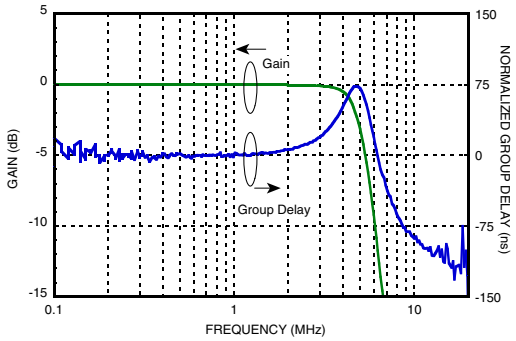


Figure 27. 72 MHz Bandwidth Filter Magnitude and Group Delay

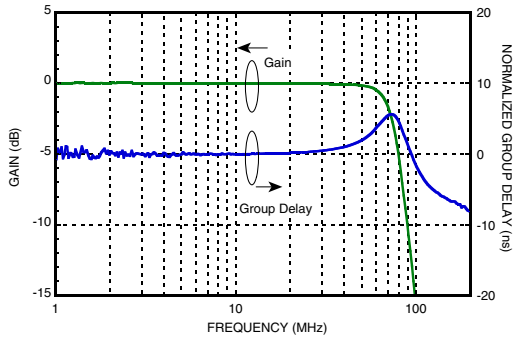


Figure 28. HMC1023LP5E Filter I/Q Channel Isolation

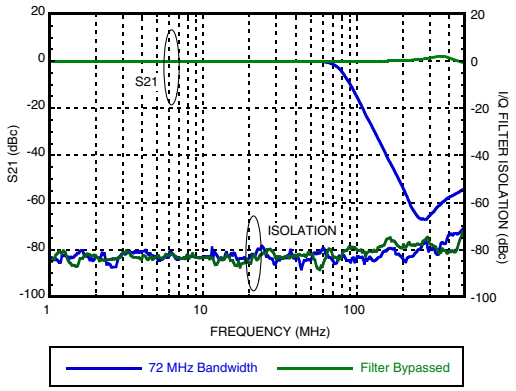


Figure 29. Input Impedance

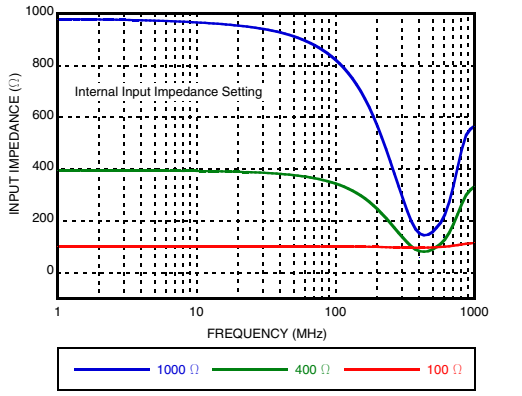
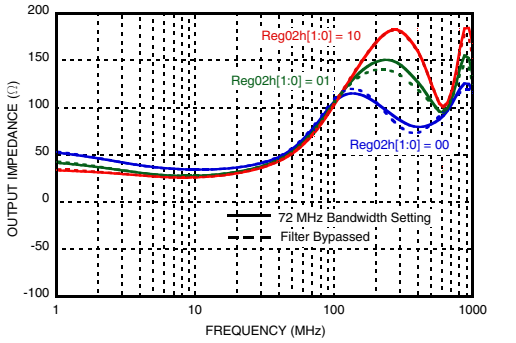


Figure 30. Output Impedance



[11] OIP3 and OIP2 measured from 100 Ω differential source into 400 Ω differential load. Used recommended OpAmp bias settings (Reg 02h[1:0]) in Table 9. OIP3 and OIP2 measurements can be translated from dBm into dBVrms as follows: IPx [dBVrms] = IPx [dBm] -4 dB

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Table 3. Absolute Maximum Ratings

Nominal 5V Supply to GND VDDCAL, VDDI, VDDQ, VDDBG, DVDD	-0.3 to 5.5 V
Common Mode Inputs Pins (CMI, CMQ)	-0.3 to 5.5 V
Input and Output Pins IIP, IIN, IQP, IQN, OIP, OIN, OQP, OQN	-0.3 to 5.5 V
Digital Pins SEN, SDI, SCK, SDO, CALCK SDO min load impedance	-0.3 to 5.5 V 1 kΩ
Operating Ambient Temperature Range	-40 to +85 °C
Storage Temperature	-65 to + 150 °C
Maximum Junction Temperature	150 °C
Thermal Resistance (Θ_{JC}) (junction to ground paddle)	10 °C/W
Reflow Soldering Peak Temperature Time at Peak Temperature	 260 °C 40 µs
ESD Sensitivity (HBM)	1 kV Class 1C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Table 4. Recommended Operating Conditions

Parameter	Condition	Min.	Typ.	Max.	Units
Temperature					
Junction Temperature				125	°C
Ambient Temperature		-40		85	°C
Supply Voltage					
VDDCAL, VDDI, VDDQ, VDDBG,DVDD		4.75	5	5.25	V

[1] Layout design guidelines set out in Qualification Test Report are strongly recommended.

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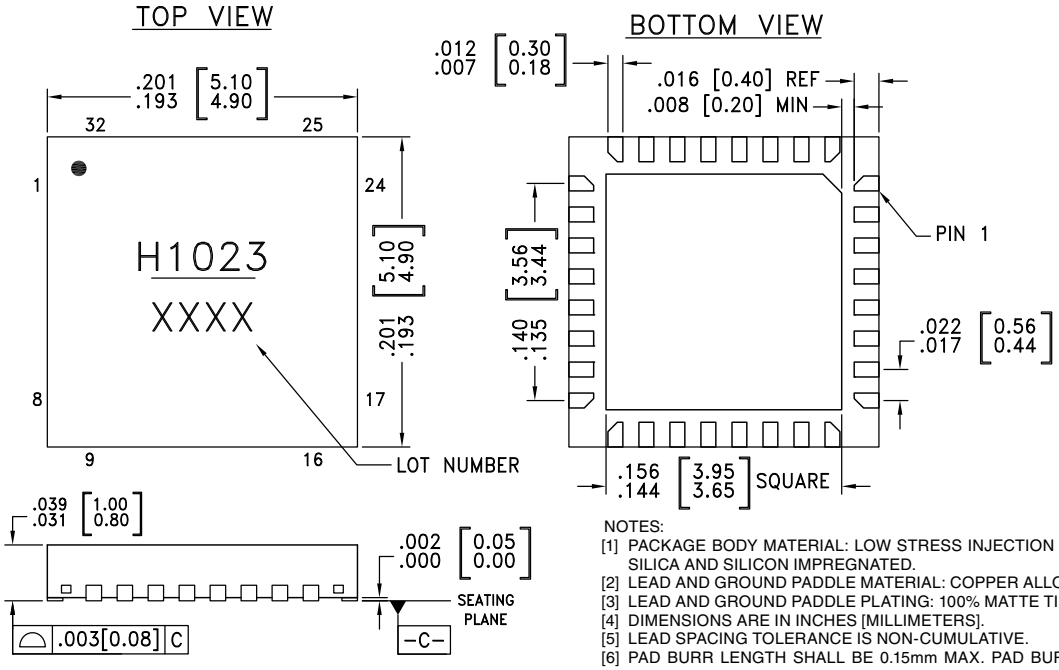
72 MHz DUAL PROGRAMMABLE LOW PASS FILTER WITH DRIVER

Outline Drawing



NOTES:
[1] PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
[2] LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
[3] LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
[4] DIMENSIONS ARE IN INCHES [MILLIMETERS].
[5] LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
[6] PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25m MAX.
[7] PACKAGE WARP SHALL NOT EXCEED 0.05mm
[8] ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GOUND.
[9] REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Table 5. Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating [1]	Package Marking [2]
HMC1023LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H1023 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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Table 6. Pin Descriptions

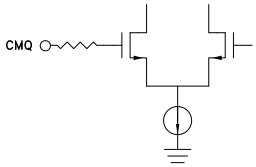
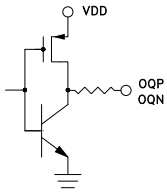
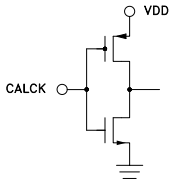
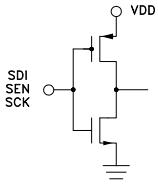
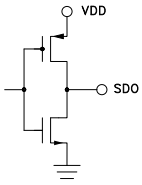
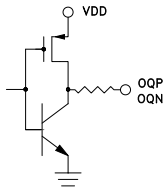
Pin Number	Function	Description	Interface Schematic
1, 3, 8 - 10, 17, 24, 25, 32	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
2, 4	VDDQ	Quadrature (Q) Channel 5V Supply. Must be locally decoupled to GND	
5	CMQ	Quadrature (Q) channel output common mode level	
6, 7	OQP, OQN	Quadrature (Q) channel positive and negative differential outputs	
11	CALCK	Calibration clock input	
12, 14, 15	SCK, SDI, SEN	SPI Data clock, data input and enable respectively.	
13	SDO	SPI Data Output	
16	DVDD	Digital 5V Supply. Must be locally decoupled to GND.	
18, 19	OIN, OIP	Inphase (I) channel negative and positive differential outputs respectively	

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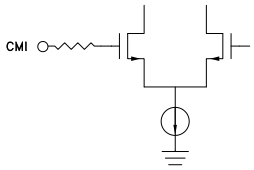
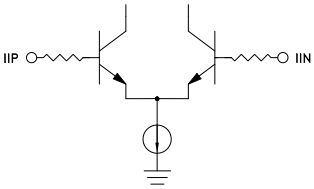
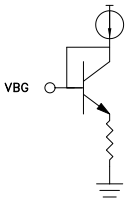
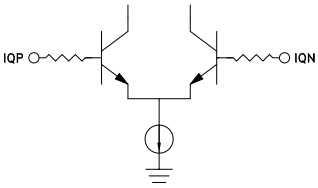
Table 6. Pin Descriptions *(Continued)*

Pin Number	Function	Description	Interface Schematic
20	CMI	Inphase (I) channel output common mode level	
21, 23	VDDi	Inphase (I) Channel 5V Supply. Must be locally decoupled to GND	
22	VDDCAL	Calibration 5V Supply. Must be locally decoupled to GND	
26, 27	IIP, IIN	Inphase (I) channel positive and negative differential inputs respectively	
28	VDDBG	Bias 5V Supply. Must be locally decoupled to GND.	
29	VBG	1.2V Bandgap output (testing only)	
30, 31	IQN, IQP	Quadrature (Q) channel negative and positive differential inputs respectively	

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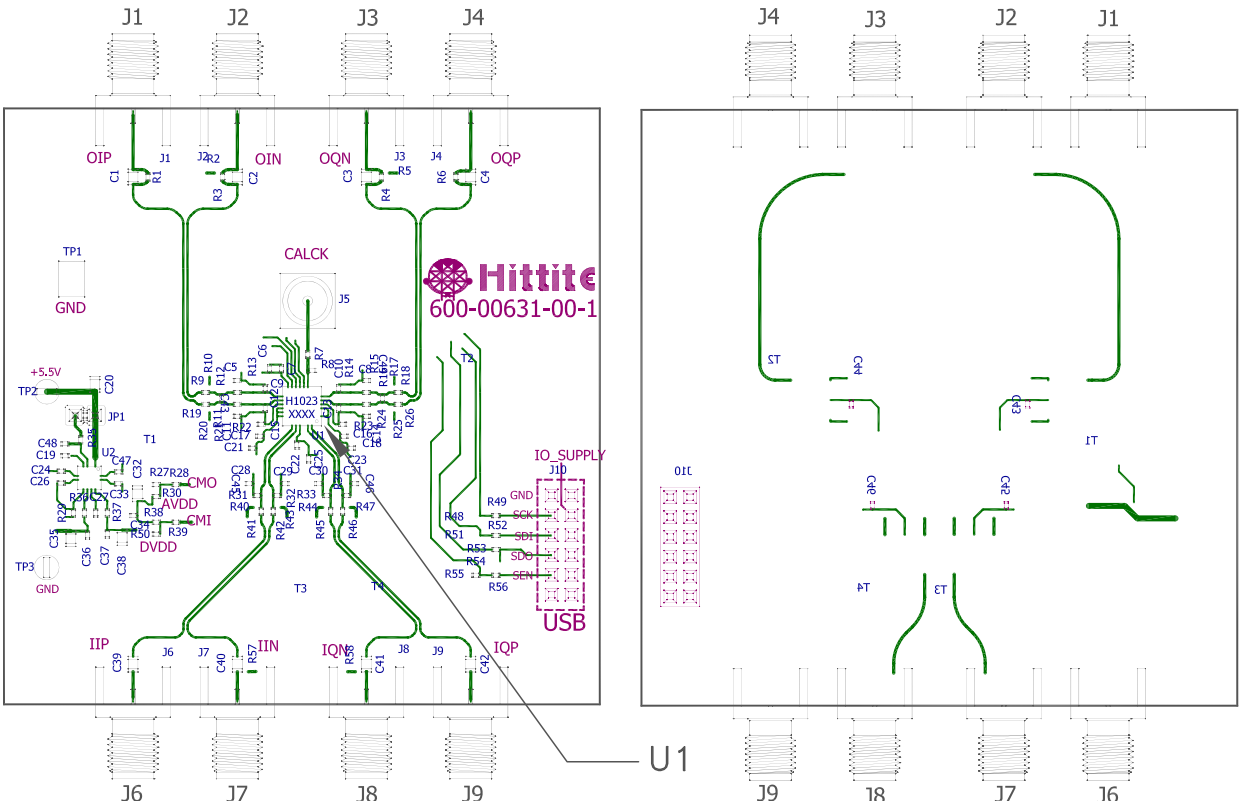
Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohms impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Table 7. Evaluation Order Information

Item	Contents	Part Number
Evaluation Kit	HMC1023LP5E Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software)	EKIT01-HMC1023LP5E

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Evaluation PCB Schematic

To view Evaluation PCB Schematic please visit www.hittite.com and choose HMC1023LP5E from the "Search by Part Number" pull down menu to view the product splash page.

Evaluation Setup

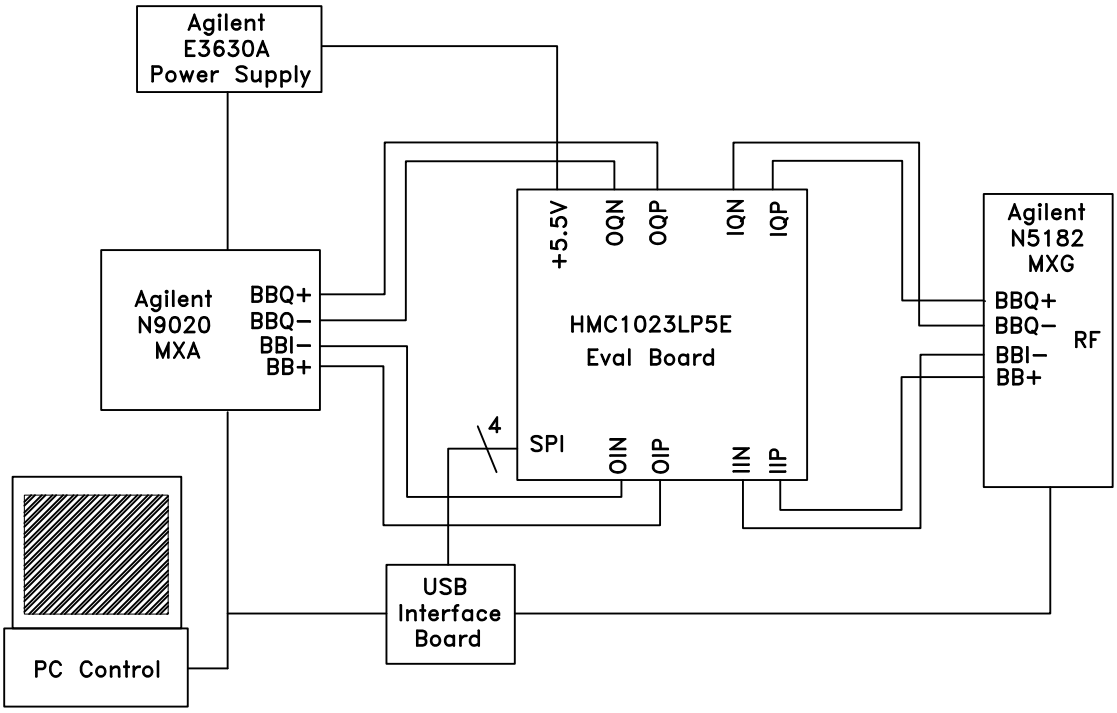

Figure 31. Characterization Setup Block Diagram

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HMC1023LP5E Usage Information

The HMC1023LP5E addresses different filter applications such as fixed frequency or variable bandwidth implementations dependent on the part selected (see HMC1023LP5E Ordering Information) and the control provided to the HMC1023LP5E. These modes provide the user with different filter options depending on the system implementation.

An overview of these trade-offs are shown below.

Table 8. HMC1023LP5E Modes of Operation

Function	Unprogrammed HMC1023LP5E-00000	Pre-programmed HMC1023LP5E-BBBGL	SPI Req'd	CALCK Req'd	Comments
Fixed Bandwidth Filter	Yes	Yes	No	No	
Default Bandwidth and Gain setting after Power On Reset (POR)	Default Bandwidth and Gain as defined by register defaults. (5 MHz /0dB gain)	Bandwidth and Gain as defined by pre-programming at factory.			Pre-programmed gain and bandwidth are defined when ordering the part. See HMC1023LP5E Ordering Information.
Typical Corner Frequency Accuracy at Default Bandwidth	+/- 20 %	+/- 2.5 %			Accuracy is with respect to bandwidth after POR.
Variable Bandwidth Filter	Yes	Yes	Yes	No	Full control over HMC1023LP5E requires access via the digital serial port (SPI).
Default Bandwidth and Gain setting after Power On Reset (POR)	Default Bandwidth and Gain as defined by register defaults. (5 MHz /0dB gain)	Bandwidth and Gain as defined by pre-programming at factory.			Pre-programmed gain and bandwidth are defined when ordering the part. See HMC1023LP5E Ordering Information.
Typical Corner Frequency Accuracy at Default Bandwidth	+/- 20 %	+/- 2.5 %			Accuracy is with respect to bandwidth after POR.
Typical Corner Frequency Accuracy at all other Bandwidths	+/- 20 %	+/- 5.0 %			Accuracy is with respect to the desired bandwidth. See "Filter Bandwidth Setting" for information regarding changing the bandwidth after when calibration is not possible.
Variable Bandwidth Filter (with ability to execute User Calibration to calibrate filter bandwidth)	Yes	Yes	Yes	Yes	Full control over HMC1023LP5E requires access via the digital serial port (SPI). Filter calibration requires valid calibration clock (via CALCK pin). See "RC Calibration Circuit"
Default Bandwidth and Gain setting after Power On Reset (POR)	Default Bandwidth and Gain as defined by register defaults. (5 MHz /0dB gain)	Bandwidth and Gain as defined by pre-programming at factory.			Pre-programmed gain and bandwidth are defined when ordering the part. See "HMC1023LP5E Ordering Information 20".
Typical Corner Frequency Accuracy after POR (before User Calibration)	+/- 20 %	+/- 2.5 %			Accuracy is with respect to bandwidth after POR.
Typical Corner Frequency Accuracy after User Calibration at **calibrated** bandwidth	+/- 2.5 %	+/- 2.5 %			Accuracy is with respect to calibrated bandwidth. User Calibration requires access to the HMC1023LP5E via the digital serial port (SPI) and requires a valid calibration clock (via CALCK pin).
Typical Corner Frequency Accuracy after User Calibration at **non calibrated** bandwidths	+/- 5.0 %	+/- 5.0 %			Accuracy is with respect to the desired bandwidth. User Calibration requires access to the HMC1023LP5E via the digital serial port (SPI) and requires a valid calibration clock (via pin CALCK). See "Filter Bandwidth Setting" for information regarding changing the bandwidth after calibration when further calibration is not possible.

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HMC1023LP5E Application Information

Accurate, arbitrary, user defined bandwidths, programmable gain, and flexible programmable IO interface provide the HMC1023LP5E with unmatched flexibility. This flexibility together with market leading performance, in terms of linearity, Noise Figure, and bandwidth accuracy enable a universal solution capable of supporting numerous radio standards, frequencies, and/or bandwidths with a single hardware platform.

The HMC1023LP5E is relevant in both transmitter and receiver applications (Figure 32 and Figure 33). In transmitter applications the HMC1023LP5E serves as an anti-aliasing filter that rejects Digital-to-Analog Converter aliases and ensures the desired transmitted spectral mask. In receiver applications the HMC1023LP5E serves as an Analog-to-Digital converter driver, an anti-aliasing filter, and a blocker rejection filter all in one.

In both transmitter and receiver applications, excellent 6th order butterworth filter response with virtually no pass-band ripple and exceptional +/-2.5% bandwidth accuracy enables simple modem designs that need not utilize complex adaptive equalization schemes to compensate for filter ripple and group delay variation.

In such applications, together with Hittite's Wideband PLLVCOs, the HMC1023LP5E enables truly wideband multi-standard multi-carrier hardware platforms, software configurable to the demands of each particular application.

Compared to discrete filters, the HMC1023LP5E saves valuable board area and cost. Typically higher order discrete filters are required to achieve comparable rejection as the HMC1023LP5E due to the inherent error tolerances in the value of each individual component. In addition, discrete filters are fixed in bandwidth, typically requiring multiple band specific hardware versions that tends to increase the cost relative to supporting only one hardware version for all bands supported by the HMC1023LP5E.

The HMC1023LP5E overcomes the matching problem that discrete filters present with respect to baseband signal processing. The matched dual filter paths provide excellent gain and phase balance between the two channels eliminating the image problem which results from poor matching.

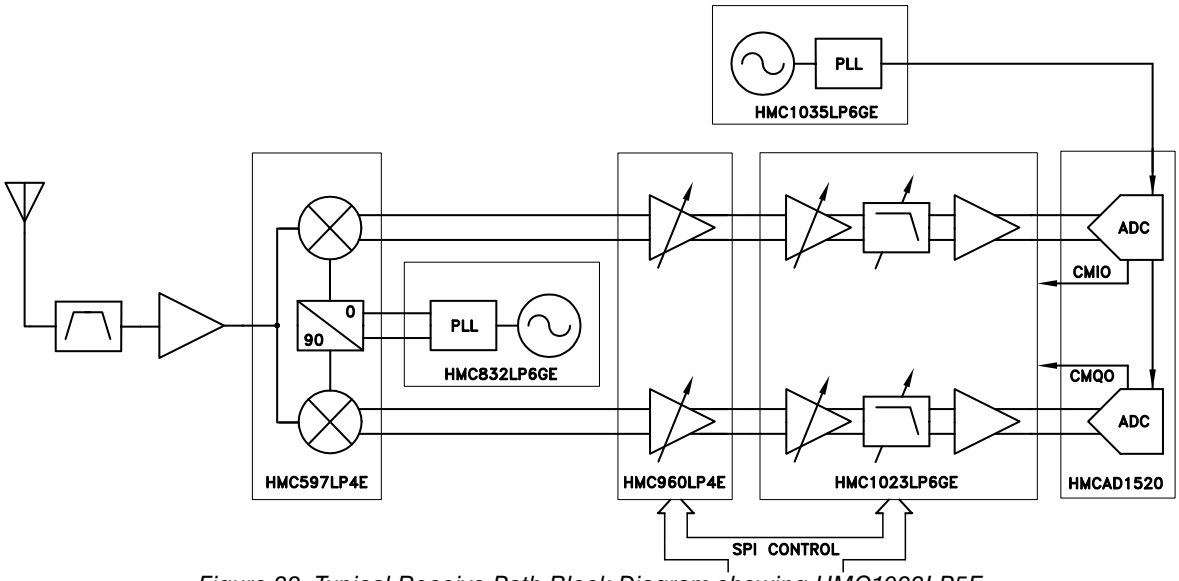

Figure 32. Typical Receive Path Block Diagram showing HMC1023LP5E

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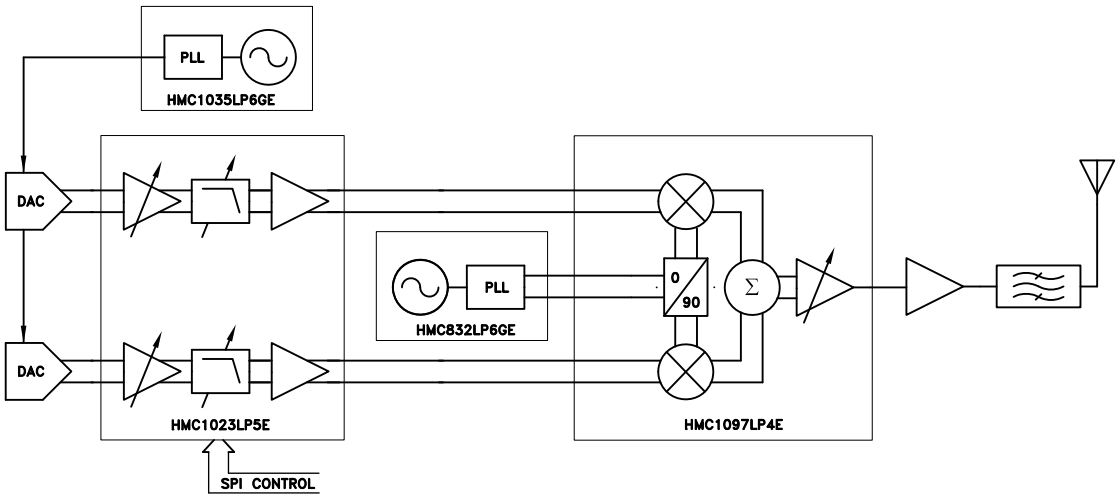

Figure 33. Typical Transmit Path Block DiagramHMC1023LP5E Ordering Information

Input Interface

Input stage features a programmable input impedance (100 Ω / 400 Ω / 1 kΩ differential, or 50 Ω / 200 Ω / 500 Ω single-ended) that is configured via Reg 01h[9] and Reg 02h[10]. Programmable impedance enables a configurable interface, tailored to the requirements of the component driving the HMC1023LP5E. It enables maximum Noise Figure (NF) performance regardless of the device driving the HMC1023LP5E. NF of the HMC1023LP5E with various input impedance settings is provided in Figure 5, Figure 6 and Figure 7. Actual input impedance over frequency is shown in Figure 29.

Wide input common mode voltage range further simplifies input interface. The HMC1023LP5E does not require any configuration for input common mode voltage as long as the part is operated within the specifications outlined in Table 1.

The HMC1023LP5E does not require any specific impedance at the input. Input interface should be designed according to the demands of the device driving the HMC1023LP5E, while programmable input impedance of the HMC1023LP5E permits optimal matching and/or NF performance. Both ac-coupled and dc-coupled interfaces are supported at the input.

Output Interface

Output common mode voltage of the HMC1023LP5E is set via CMI and CMQ pins for the in-phase and quadrature outputs respectively. Wide output common mode voltage range simplifies interface with numerous devices. The HMC1023LP5E's 0.9 V to 3 V output common mode voltage range is specified with a 2 Vppd output signal swing. Lower common mode output voltage is supported with lower signal swing. The key requirement is that the signal swing in combination with common mode voltage does not go below 0.5 V single-ended. Hence, as an example a 0.7 V output common mode voltage level is supported with 0.8 Vppd signal swing. Figure 18 to Figure 23 show the effect of output common mode voltage on linearity performance (Output IP2 & Output IP3) of the HMC1023LP5E. The plots indicate that even for a large output signal swing of 2 Vppd, the HMC1023LP5E typically maintains high linearity performance below 0.9 V nominal output common mode limit. Figure 34 shows measured output common mode voltage as a function of input common mode setting on CMI & CMQ pins. The plot is generated with 2 Vppd output signal and shows that output common mode voltage follows the settings on CMI & CMQ pins well beyond the rated 0.9 V to 3 V.

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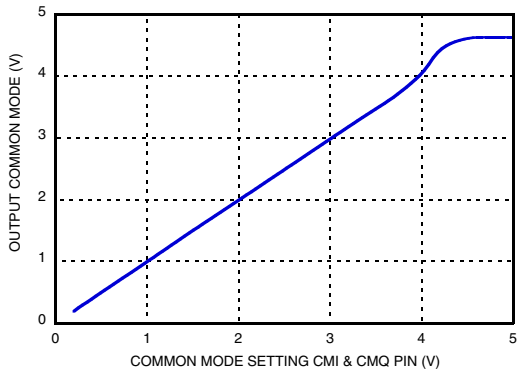

Figure 34. Output vs. Input Common Mode Voltage

Output impedance of the HMC1023LP5E is nominally 10 Ω single-ended or 20 Ω differential. The HMC1023LP5E does not require any special impedance matching at the output. The output of the HMC1023LP5E is an OpAmp driver capable of driving small and large loads alike. Output interface of the HMC1023LP5E should be designed according to the demands of the device the HMC1023LP5E is driving.

Linearity, Bandwidth Accuracy, and Current Consumption

As shown in Figure 25, the HMC1023LP5E is a high linearity device, typically exhibiting in excess of 30 dBm Output IP3, and over 60 dBm Output IP2 throughout the operating range of the part. To maintain maximum performance as measured by linearity (Output IP2 and Output IP3) and bandwidth accuracy it is recommended to use OpAmp bias settings (Reg 02h[1:0]) outlined in Table 9. Table 9 shows that higher OpAmp bias setting, and thereby higher current consumption is required to maintain maximum linearity performance as well as bandwidth accuracy (< 2.5% bandwidth error) at bandwidth settings ≥ 10 MHz. Figure 12 to Figure 23 show the effect of OpAmp bias setting (Reg 02h[1:0]) on linearity (OIP2 and OIP3) performance of the HMC1023LP5E.

Table 9. HMC1023LP5E Bias Table

Coarse Bandwidth (MHz)	Coarse Bandwidth Setting (Reg 02h[9:6])	Recommended OpAmp Bias Setting For Best Performance Reg 02h[1:0]	HMC1023LP5E Typical Current Consumption (mA)
5	0000	00	172
7	0001	00	172
10	0010	00	172
14	0011	01	227
20	0100	01	227
28	0101	01	227
40	0110	01	227
50	0111	01	227
72	1000	10	260

Figure 12 to Figure 23 show that the higher OpAmp bias setting typically increases linearity OIP3 & OIP2 by 5 to 10 dB at high bandwidth setting. However, they also show that the HMC1023LP5E maintains excellent linearity performance (~60 dBm OIP2 & ~30 dBm OIP3), even at minimum OpAmp bias setting (Reg 02h[1:0] = 0).

Figure 35 shows typical calibrated filter bandwidth error (accuracy) vs OpAmp bias setting (Reg 02h[1:0]). It shows that higher OpAmp bias is required at filter bandwidth settings ≥ 10 MHz in order to achieve ≤ +/-2.5 % bandwidth accuracy. However it also shows that excellent bandwidth accuracy (≤ +/-5.5 %) is achievable at all filter bandwidth settings with even the lowest OpAmp bias setting (Reg 02h[1:0]).

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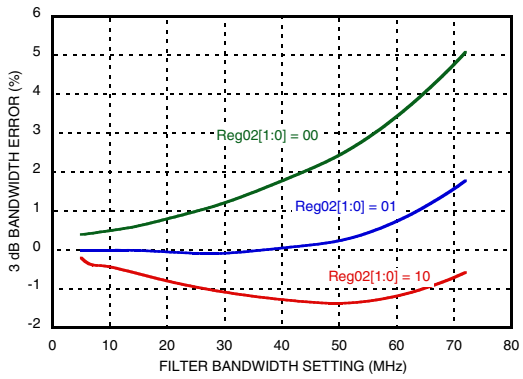

Figure 35. Calibrated HMC1023LP5E Bandwidth Error vs. OpAmp Bias (Reg 02h[1:0])

Hence for applications in which current consumption is an important performance criteria it is possible to reduce the HMC1023LP5E current consumption by ~90 mA or ~450 mW at a cost of ~5 dB lower linearity performance and lower, but still excellent bandwidth accuracy performance of ≤ +/-5.5 %.

Non-Volatile One Time Programmable (OTP) Memory

The HMC1023LP5E includes OTP (One Time Programmable) memory that enables the user to program the default configuration of the HMC1023LP5E on start-up. The programmable settings are shown in Reg 0Ah they include:

- Bandwidth
- Filter bypass enable
- Gain
- Input impedance (100 Ω or 1kΩ differential), 400 Ω differential is also available but can only be set via SPI interface.
- OpAmp bias
- Driver bias

Once the OTP memory is programmed, by default on power-up, the HMC1023LP5E enters the state programmed in OTP memory. However, even after the OTP memory is programmed HMC1023LP5E retains full functionality, and can be re-configured to any other state via Serial Port Interface. Therefore the configuration burned in OTP memory is only a default configuration of the HMC1023LP5E on power up, which can be changed to any user defined configuration after power-up using the SPI.

Detailed instructions on programming the OTP memory are provided in "One Time Programmable Memory (OTP)" section.

Filter Programming & Calibration

Detailed description of filter bandwidth programming is provided in "Filter Bandwidth Setting" section. To achieve the rated accuracy, each HMC1023LP5E device requires calibration at least once. Once calibrated, the settings are always valid for that particular HMC1023LP5E.

Filter calibration requires an input clock. More information about calibration clock and calibration procedure is provided in "RC Calibration Circuit" section. The calibration clock is only required during calibration. It is not required for the operation of the HMC1023LP5E.

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HMC1023LP5E Ordering Information

The HMC1023LP5E is available as product that is either un-programmed or pre-programmed. Programming is available to a variety of filter bandwidths (defined in this context as the 3dB bandwidth).

Other options available for pre-programmed product include the single path gain and bias state as described below. Gain and bias settings are described in Reg 02h.

When placing an order for the HMC1023LP5E please observe the following guidelines.

1. To order the un-programmed standard part please place order using the part number HMC1023LP5E-000000.
2. To order a pre-programmed HMC1023LP5E please determine the part number as described below and then contact Hittite Sales at sales@hittite.com or call (978) 250-3343.

   2.1 Minimum quantity order for the pre-programmed HMC1023LP5E-BBBGLL is 500 pieces.
3. Pre-Programmed part number description: HMC1023LP5E-BBBGL.

   3.1 'BBB' represents a three digit number from the Table 10 that represents the desired bandwidth setting (3 dB bandwidth) from 5 MHz to 72 MHz (for example BBB = 050 specifies a 5 MHz corner frequency).

   3.2 'G' represents the gain setting of either 0 dB (G = 0) or 10 dB (G = 1).

   3.3 'LL' represents the OpAmp bias setting of the HMC1023LP5E. For more information please see "Linearity, Bandwidth Accuracy, and Current Consumption" section.

For example, to order the HMC1023LP5E pre-programmed for 72 MHz 3 dB frequency, 10 dB gain, and standard low '00' OpAmp bias setting please specify part number HMC1023LP5E-720100.

Table 10. Custom Part Frequency Options

BBB frequency for custom part (actual frequency is BBB x 0.1 MHz)									
050	069	093	128	171	229	307	411	554	709
052	070	095	131	175	235	315	422	565	720
053	071	098	134	179	240	322	432	576	
054	073	100	137	180	246	330	443	587	
056	075	102	140	184	253	338	454	598	
057	076	105	141	188	259	347	465	609	
058	078	108	144	193	265	355	476	621	
060	080	110	148	198	272	364	488	632	
061	082	113	151	203	278	373	500	643	
063	084	116	155	208	280	382	510	654	
064	086	119	159	213	285	392	521	665	
066	088	121	163	218	292	400	532	676	
068	091	124	167	224	300	401	543	687	

For additional information or inquiries please contact Hittite Apps Support at apps@hittite.com.

[1] The Output IP2 and Output IP3 for the two linearity settings are shown in Figure 13 and Figure 14. High linearity setting improves linearity for bandwidths greater than 30 MHz at the cost of increased current consumption (additional 25 mA).

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Theory of Operation

The HMC1023LP5E consists of the following functional blocks

1. Input Gain Stage
2. 6th Order Butterworth LPF
3. Output Driver
4. RC Calibration Circuit
5. Bias Circuit
6. One Time Programmable Memory
7. Serial Port interface
8. Built in Self Test (RC-BIST)

Input Gain Stage

The HMC1023LP5E input stage consists of a programmable 0 or 10 dB gain stage which in turn drives the 6th order LPF. A block diagram showing input impedance of the I channel is presented below, Q channel is similar.

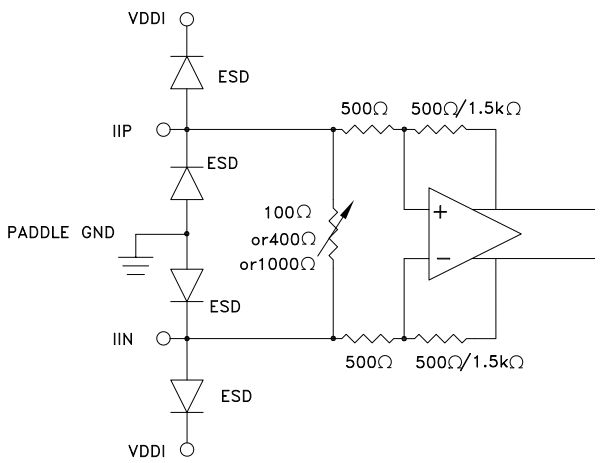

Figure 36. Input Stage Block Diagram

6th Order Low Pass Filter (LPF)

The LPF allows for coarse bandwidth tuning by varying the capacitive elements in the filter, while the fine bandwidth tuning is accomplished by varying the resistors. Note that all Op-Amps in the LPF are class AB for minimum power consumption in the filter while maintaining excellent distortion characteristics even in large signal swing conditions.

The attenuation due to the LPF can be calculated for any frequency, f, from the standard Butterworth transfer function for a 6th order filter. Specifically the attenuation of the filter, in dB, can be calculated as:

$$\text{attenuation} = 10*\log_{10}(1+(f/f_c)^{(2*6)})$$

where f_c is the 3 dB bandwidth or corner frequency for the filter.

Note that for a 6th order Butterworth filter the 1 dB bandwidth is 90% of f_c, and the 0.3 dB bandwidth is 80% of f_c.

Filter Bandwidth Setting

The 3 dB bandwidth of the HMC1023LP5E is programmable anywhere within the range from 5 MHz to 72 MHz. When calibrated, filter bandwidth is accurate to within +/-2.5% of the programmed bandwidth, if not calibrated it is accurate to within +/-20% of the programmed bandwidth.

The calibration of HMC1023LP5E is required to be executed only once for each individual HMC1023LP5E. Once

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executed, if the calibration settings are remembered, they are always valid for a specific HMC1023LP5E.

Please note that best bandwidth accuracy is achieved when the HMC1023LP5E is calibrated at its typical operating temperature. Programmed bandwidth varies 0.03 %/°C.

Filter Bandwidth Configuration

The HMC1023LP5E bandwidths are configured using Coarse Bandwidth Settings in Reg 02h[9:6], and Fine Bandwidth Settings in Reg 03h[3:0]. Coarse Bandwidth Settings select from a choice of coarse bandwidth options in Table 11, and the Fine Bandwidth Settings further refine the selected coarse bandwidth settings according to Table 12.

In all cases, once the Reg 02h[9:6] and/or Reg 03h[3:0] have been programmed it is required to set Reg 01h[4]=1 in order to instruct the HMC1023LP5E to use provided settings.

After calculating the settings for a given device they can be stored permanently in the non volatile memory (See "One Time Programmable Memory (OTP)" for more information).

Uncalibrated Bandwidth Configuration

When not calibrated, the coarse bandwidth is selected via Reg 02h[9:6] according to the desired coarse bandwidth setting in Table 11.

Example: to select bandwidth of 14 MHz simply write Reg 02h[9:6] = '0011'b, then write Reg 01h[4]=1 to instruct the HMC1023LP5E to use provided settings.

If desired, it is possible to tune to an arbitrary bandwidth choice not provided in Table 11. In that case nearest coarse bandwidth is selected via Reg 02h[9:6] according to Table 11, and the bandwidth is further refined via Reg 03h[3:0] according to Table 12, where

$$\text{Reg 03h}[3:0] = f_{WANTED} / f_{BW_norm_coarse_typ},$$

where $f_{BW_norm_coarse_typ}$ corresponds to the selected typical coarse bandwidth setting in Table 11, programmed via Reg 02h[9:6].

Example: to select the bandwidth of 13 MHz, select the closest typical value in Table 11, and program Reg 02h[9:6] accordingly (ie. Reg 02h[9:6] = '0011'b), then Reg 03h[3:0] = $f_{WANTED} / f_{BW_norm_coarse_typ}$ *= 13 MHz/14 MHz = 0.9286. Hence from Table 12, Reg 03h[3:0] = '0100'. Finally, write Reg 01h[4]=1 to instruct the HMC1023LP5E to use provided settings.*

In all cases, when uncalibrated the bandwidth is accurate to within +/-20% of the programmed bandwidth.

Calibrated Bandwidth Configuration

The calibration of HMC1023LP5E is required to be executed only once for each individual HMC1023LP5E. Once executed, if the calibration settings are remembered, they are always valid for that specific HMC1023LP5E. Detailed instructions of how to calibrate the HMC1023LP5E are available in RC Calibration Circuit section.

When calibrated the programmed bandwidth is accurate to +/-2.5%. The HMC1023LP5E calibrated bandwidth can be programmed in two ways, Automatic or Manual.

The automatic calibration supports only Coarse Bandwidth Settings in Table 11, whereas the Manual calibration supports arbitrary bandwidths from 5 MHz to 72 MHz. In both cases the bandwidth is accurate to within +/-2.5%.

Calibrated Automatic Bandwidth Configuration

In Automatic bandwidth setting the user simply selects from a choice of Coarse Bandwidths in Table 11 via Reg 02h[9:6], and the HMC1023LP5E automatically programs Reg 03h[3:0] during calibration so that the selected bandwidth is accurate to within +/-2.5%.

Example: to select bandwidth of 14 MHz simply write Reg 02h[9:6] = '0011'b, then write Reg 01h[4]=1 to instruct the HMC1023LP5E to use provided settings.

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Calibrated Manual Bandwidth Configuration

Manual bandwidth setting enables arbitrary user defined bandwidths between 5 MHz and 72 MHz accurate to within +/-2.5%. The coarse bandwidth is selected from Table 11 via Reg 02h[9:6], and that bandwidth is further refined using selections in Table 12 via Reg 03h[3:0].

Initially the calibration result is read from Reg 09h[23:0]. Then required Coarse Bandwidth selection is calculated as follows:

$$f_{BW_norm_coarse} = f_{WANTED} * (\text{Reg 09h}[23:0] + 153600)/10370000 \quad \text{(EQ 1)}$$

where f_{WANTED} is the desired arbitrary bandwidth. The Coarse Bandwidth nearest to calculated $f_{BW_norm_coarse}$ is selected from Table 11 and written to Reg 02h[9:6].

To calculate the Fine Bandwidth Setting fine_tune_ratio is calculated as shown in (EQ 2):

$$\text{fine_tune_ratio} = f_{BW_norm_coarse} / f_{BW_norm_coarse_typ} \quad \text{(EQ 2)}$$

where the $f_{BW_norm_coarse}$ is given in (EQ 1), and $f_{BW_norm_coarse_typ}$ is the nearest corresponding bandwidth in Table 11. Then Fine Bandwidth Setting is selected from a nearest column in Table 12 that corresponds to the calculated fine_tune_ratio and programmed to Reg 03h[3:0].

*Example: to select the bandwidth of 13 MHz, initially read Reg 09h[23:0] (in this example Reg 09h[23:0] = 10470000). Then according to (EQ 1), $f_{BW_norm_coarse}$ = 13 MHz * (10470000 + 153600)/10370000 = 13.318 MHz. Select the closest typical value in Table 11 to 13.318 MHz and program Reg 02h[9:6] accordingly (ie. Reg 02h[9:6] = '0011'b), then Reg 03h[3:0] = f_{WANTED} / $f_{BW_norm_coarse_typ}$ = 13.317917 MHz/14 MHz = 0.95128. Hence from Table 12, Reg 03h[3:0] = '0101'. Finally, write Reg 01h[4]=1 to instruct the HMC1023LP5E to use provided settings.*

Please note that the HMC1023LP5E Evaluation Software distributed with HMC1023LP5E Evaluation Kits implements this Calibrated Arbitrary Bandwidth algorithm.

Table 11. Normalized Bandwidth Look up Table

coarse_bandwidth_code[3:0]	$f_{BW_norm_coarse}$		
	min (MHz)	typ (MHz)	max (MHz)
0000	3.948	5	6.050
0001	5.527	7	8.470
0010	7.896	10	12.100
0011	11.054	14	16.940
0100	15.792	20	24.200
0101	22.109	28	33.880
0110	31.584	40	48.400
0111	39.480	50	60.500
1000	56.851	72	87.120

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Table 12. Calibration Code Look up Table

fine_bandwidth_code [3:0]	fine_tune_ratio		
	min (MHz/MHz)	typ (MHz/MHz)	max (MHz/MHz)
0000	0.790	0.803	0.818
0001	0.818	0.832	0.846
0010	0.846	0.862	0.878
0011	0.878	0.893	0.909
0100	0.909	0.926	0.943
0101	0.943	0.959	0.976
0110	0.976	0.994	1.012
0111	1.012	1.030	1.048
1000	1.048	1.063	1.078
1001	1.078	1.097	1.116
1010	1.116	1.136	1.155
1011	1.155	1.183	1.210

To reprogram the HMC1023LP5E to any other bandwidth simply repeat the steps above.

Filter Bandwidth Setting After Calibration

In cases where ctune is unknown but the calibrated and programmed bandwidth is known, it is possible to estimate the value of ctune based on the values of Coarse Bandwidth Code and Fine Bandwidth Code and the corresponding values in Table 11 and Table 12.

For example, if the 3 dB bandwidth for the HMC1023LP5E was factory pre-programmed to a customer defined requirement of 34 MHz and Reg 02h[9:6] = “0110” (Coarse Bandwidth Code) and Reg 03h[3:0] = “0010” (Fine Bandwidth Code), as determined from Reg 0Ah for a pre-programmed part or from Reg 02h & Reg 03h for a non programmed part, then ctune can be estimated as follows:

1. Lookup the nominal coarse bandwidth and fine bandwidth frequencies.
   a. From Table 11 the nominal coarse frequency is 40 MHz
   b. From Table 12 the nominal fine normalized frequency is 0.862 MHz/ MHz or simply 0.862
2. Estimate ctune as:

$$ctune=(40\ MHz * 0.862\ )/\ 34\ MHz = 1.0141$$

This value of ctune can now be used to calculate any arbitrary filter frequency as described above.

RC Calibration Circuit

The RC Calibration block uses a known user supplied clock to measure an on chip RC time constant. This measurement is representative of the uncorrected corner frequency error for a given bandwidth for the HMC1023LP5E.

Calibration is normally done at room temperature. Refer to “Table 1. Electrical Specifications” for further details on the variation of the 3 dB cutoff point with temperature. Typically programmed bandwidth varies 0.03 %/ºC.

With this information, the HMC1023LP5E can correctly fine tune the LPF by adjusting the resistors in the LPF to center the corner frequency to the desired bandwidth.

To calibrate the HMC1023LP5E proceeds as follows:

1. Apply a clock signal of frequency between 20 MHz and 100 MHz on the CALCK pin (pin 11) of the HMC1023LP5E. The clock signal only needs to be applied during the calibration procedure and is not

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required at other time. Please note that an integrated clock doubler must be enabled for clock frequencies less than 40 MHz. To enable the clock doubler simply write Reg 01h[5] = 1.

2. Write the applied clock signal period to Reg 05h[14:0] in picoseconds.
3. Enable the RC calibration circuit by writing Reg 01h[1] = 1.
4. Write Reg 06h[8:0] = 152d = 96h.
5. Write Reg 04h = 0 to initialize the calibration cycle.

The HMC1023LP5E indicates that the calibration is in process when Reg 08h [4]=1. When Reg 08h [4]=0 calibration has finished. When complete, the calibration Fine Bandwidth Value can be retrieved from Reg 08h[3:0] Once calibrated the HMC1023LP5E automatically writes the calibrated fine Fine Bandwidth values to Reg 03h[3:0] (ie. Reg 03h[3:0] = Reg 08h[3:0]) as explained in Calibrated Automatic Bandwidth Configuration section. If desired, the calibration results can be overridden via Reg 03h [3:0], as explained in Calibrated Manual Bandwidth Configuration section.

Output Driver

The HMC1023LP5E output driver consists of a differential class AB driver which is designed to drive typical ADC loads directly or can drive up to 200 Ω in parallel with 50 pF to AC ground per differential output. Note that the output common mode of the driver is controlled directly via the CMI/CMQ pin and can be set as per "Table 1. Electrical Specifications". Also note, that driver loading does not impact filter transfer responses.

A block diagram showing output connections is presented below.

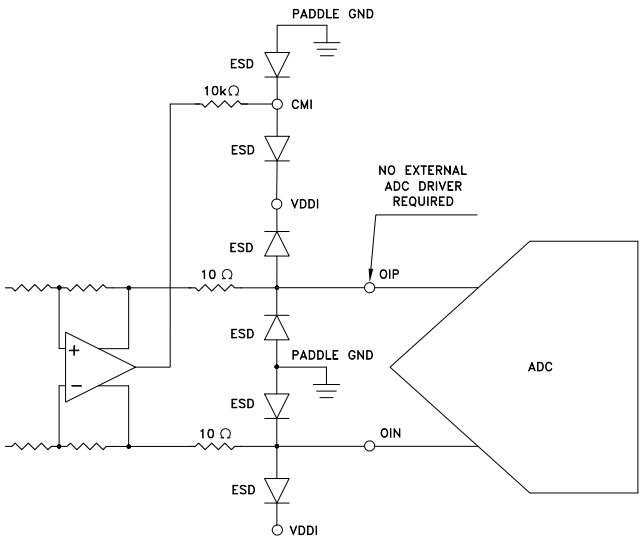

Figure 37. Output Driver Block Diagram

Bias Circuit

A band gap reference circuit generates the reference currents used by the different sections. The bias circuit is enabled or disabled as required with the I or Q channel as appropriate.

One Time Programmable Memory (OTP)

The HMC1023LP5E features one time programmable memory which can be programmed by the end user or ordered from the factory precalibrated.

The OTP memory is programmed via the standard 4 wire serial port (SPI) as follows:

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1. enable OTP write mode (see Reg 0Bh bit 0 enables OTP programming).
2. read the status of the OTP active flag (see Reg 08h, bit 5 is the OTP active flag). The Write Pulse Status (OTP active flag) must be 0 to allow the OTP to be programmed.
3. write the OTP bit address to be set (Reg 0Ch). This address is a 4 bit number representing the address of the bit to be programmed. Note that when programming a bit we change its state from 0 to 1 and this operation cannot be reversed. OTP bit addresses can be found in Reg 08h.
4. start the OTP Write operation. Write any data to the OTP strobe register (Reg 0Dh).
5. read the status of the OTP active flag (Reg 08h, bit 5 is the OTP active flag). If bit 5 is set then the Write pulse is still high. Repeat until bit 5 is 0 which indicates that the write pulse is finished.
6. Repeat steps 3 to 5 to program the remaining desired bits.

   Note that bit 13 OTP_prg_flag must be set by the user to use OTP values.
7. When completed, disable OTP write mode (Reg 0Bh).

Power on Reset and Soft Reset

The HMC1023LP5E has a built in Power On Reset and also a serial port accessible Soft Reset. Power On Reset is accomplished when power is cycled to the HMC1023LP5E, while Soft Reset is accomplished via the SPI by writing Reg 00h[5] = 1 followed by writing Reg 00h[5] = 0. All chip registers will be reset to default states approximately 250us after power up.

Serial Port Interface

The HMC1023LP5E features a four wire SPI. Four wires (SEN,SCK,SDI,SDO) are necessary to implement a SPI Read/Write functionality, while a Write only functionality can be implemented with 3 wires (SEN,SCK,SDI). The HMC1023LP5E SPI features a 3-bit Chip_ID that enables operation of up to 8 devices on the same SPI bus. Chip_ID of HMC1023LP5E is set to '101'b.

Please note that every SPI operation is both a Read and a Write. Data is written to the HMC1023LP5E on the SDI line, and read from the HMC1023LP5E on the SDO line every Read/Write cycle, as shown in Figure 38. Every SPI write the HMC1023LP5E returns the data contained in the register whose address is specified in Reg 00h[4:0] prior to the Write/Read cycle.

Hence to read from a particular HMC1023LP5E register, it is necessary to initially write the address of that register to Register 0 (ie. Reg 00h[4:0] = REG_ADDR, where REG_ADDR is the address of the register to be read on the next Read/Write cycle). The desired register will be read on the next (2nd) Write/Read cycle. If nothing additional is desired to be written to the HMC1023LP5E on the 2nd Write/Read cycle, simply rewrite Reg 00h[4:0] = REG_ADDR on the second Read/Write cycle to conclude the register read.

In summary, the Read cycle uses indirect addressing where Reg 00h contains the pointer to the address of the register to be Read. Note that in any SPI cycle the Write data is stored in the register at the end of the cycle when SEN goes high. This means that the address pointer (Reg 00h[4:0]) must be set prior to the Read/Write cycle in which the desired data is read.

Typical serial port operation can be run with SCK at speeds up to 30 MHz.

Serial Port WRITE Operation

The host changes the data on the falling edge of SCK and the HMC1023LP5E reads the data on the rising edge.

A typical WRITE cycle is shown in Figure 38. It is 32 clock cycles long.

1. The host sets Serial Port Enable (SEN) low and places the MSB of the data on Serial Data Input (SDI) followed by a rising edge on SCK.
2. HMC1023LP5E reads SDI (MSB first) on the 1st rising edge of SCK after SEN.

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3. HMC1023LP5E registers the data bits, D23:D0, on the next 23 rising edges of SCK (total of 24 data bits).
4. Host places the 5 register address bits, A4:A0, on the next 5 falling edges of SCK (MSB to LSB) while the HMC1023LP5E reads the address bits on the corresponding rising edge of SCK.
5. Host places the 3 chip address bits, CA2:CA0=[101], on the next 3 falling edges of SCK (MSB to LSB). Note the HMC1023LP5E chip address is fixed as “5d” or “101b”.
6. SEN goes from low to high after the 32nd rising edge of SCK. This completes the WRITE cycle.
7. HMC1023LP5E also exports data back on the Serial Data Out (SDO) line. For details see the section on READ operation.

Serial Port READ Operation

The Read data is available on SDO line. This line itself is tri-stated when the device is not being addressed. However when the device is active and has been addressed by the SPI, the HMC1023LP5E controls the SDO line and exports data on this line during the next SPI cycle.

HMC1023LP5E changes the data to the host on the rising edge of SCK and the host reads the data from HMC1023LP5E on the falling edge.

A typical READ cycle is shown in Figure 38. Read cycle is 32 clock cycles long. To specifically read a register, **the address of that register must be written to dedicated** Reg 00h. This requires two full cycles, one to write the required address, and a 2nd to retrieve the data. A read cycle can then be initiated as follows;

1. The host sets SEN line low, followed by a rising edge SCK.
2. HMC1023LP5E reads SDI (MSB first) on the 1st rising edge of SCK after SEN is set low.
3. HMC1023LP5E registers the data bits in the next 23 rising edges of SCK (total of 24 data bits). **The LSBs of the data bits represent the address of the register that is intended to be read.**
4. Host places the 5 register address bits on the next 5 falling edges of SCK (MSB to LSB) while the HMC1023LP5E reads the address bits on the corresponding rising edge of SCK. **For a read operation this is “00000”b.**
5. Host places the 3 chip address bits <101> on the next 3 falling edges of SCK (MSB to LSB). Note the HMC1023LP5E chip address is fixed as “5d” or “101b”.
6. SEN goes from low to high after the 32th rising edge of SCK. This completes the first portion of the READ cycle, in which the address of the register to be read on the next Read/Write cycle is written to Reg 00h.
7. The host sets SEN line low, followed by a rising edge SCK.
8. HMC1023LP5E places the 24 data bits, 5 address bits, and 3 Chip_ID bits, on the SDO, on each rising edge of the SCK, commencing with the first rising edge beginning with MSB.
9. The host sets SEN line high after reading the 32 bits from the SDO output. The 32 bits consists of 24 data bits, 5 address bits, and the 3 chip id bits.
10. This completes the READ cycle.

Note that the second Read/Write cycle is also both a Read and a Write. Hence if it is not desired to write anything new to the HMC1023LP5E on the second Read/Write cycle simply rewrite the same data to Reg 00h that was written on the previous cycle.

Serial Port Bus Operation with Multiple Devices

The SPI bus architecture supports multiple devices on the same SPI bus. Each HMC1023LP5E on the bus requires a dedicated SEN line to enable the appropriate device.

The SDO line is normally driven by the HMC1023LP5E during and after an SPI read/write which is addressed directly to the HMC1023LP5E (chip address = 5d or ‘101’b). A write to the HMC1023LP5E where chip address is set to any value other than 5d or ‘101’b is required in order to ensure that the SDO pin remains tri-stated by the HMC1023LP5E

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after accessing the HMC1023LP5E. Such a write will not result in any change in the HMC1023LP5E configuration because of the incorrect chip address.

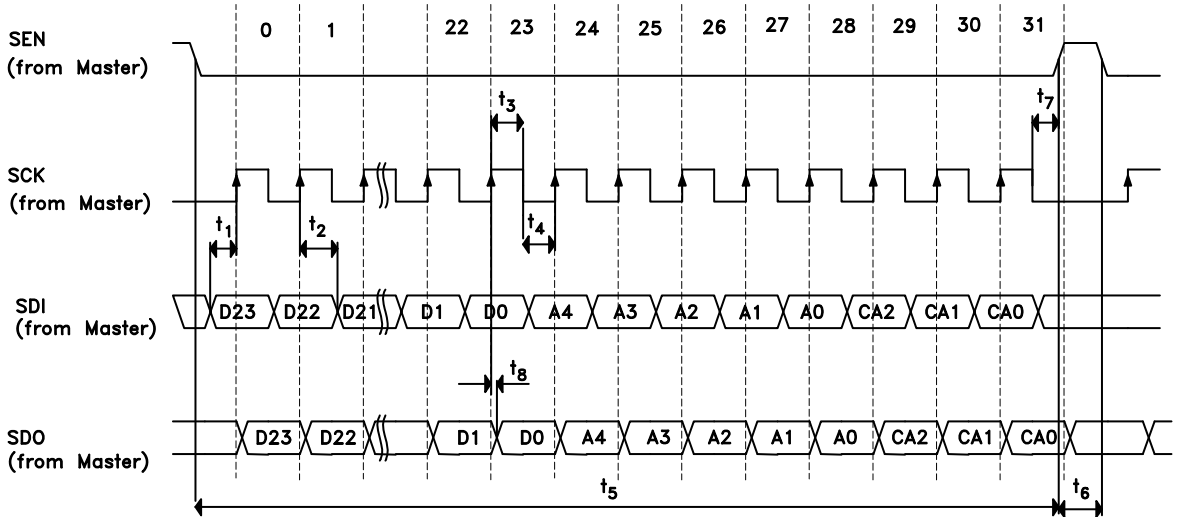

Figure 38. SPI Timing Diagram

Table 13. Main SPI Timing Characteristics

DVDD = 5V ±5%, GND = 0V

Parameter	Conditions	Min	Typ	Max	Units
t_1	SDI to SCK Setup Time	8			nsec
t_2	SDI to SCK Hold Time	8			nsec
t_3	SCK High Duration [a]	10			nsec
t_4	SCK Low Duration	10			nsec
t_5	SEN Low Duration	20			nsec
t_6	SEN High Duration	20			nsec
t_7	SCK to SEN [b]	8			nsec
t_8	SCK to SDO Out[c]			8	nsec

a. The SPI is relative insensitive to the duty cycle of SCK.

b. SEN must rise after the 32nd falling edge of SCK but before the next rising SCK edge. If SCK is shared amongst several devices this timing must be respected.

c. Typical load to SDO 10pF, max 20pF

Built In Self Test (RC-BIST)

The HMC1023LP5E RC Calibration state machine features built in self test (RC-BIST) to facilitate improved device testing.

The RC-BIST can be exercised as follows:

1. Apply reset to the chip via a power cycle (hard reset) or via the SPI (soft reset). Soft reset is accomplished by writing Reg 00h = 20h, followed by writing Reg 00h = 0h.
2. Setup the RCCAL input parameters if desired. Note that the RC-BIST will work with the default settings from power up however test coverage will improve if the following SPI registers are also accessed:
   a. program the RC clock period (Reg 05h).

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b. program the measurement adjustment setting (Reg 06h).

c. program the threshold adjustment settings.

3. enable BIST mode (Reg 0Eh).
4. start the BIST by writing any data to the BIST strobe register (Reg 04h). Note that the BIST will take 2^{18} ~ 260k clock cycles to complete.
5. read the result of the BIST test. Read the value in the BIST Out register (Reg 0F). Bit 16 is the busy flag and will be set when the BIST is still running. When this bit is reset then the BIST output value in bits 15:0 are valid.

   Note that the value of the BIST output must be compared to the expected result depending on values programmed into the registers in step 2.

The BIST procedure can be repeated as desired to ensure adequate test coverage for the RC Calibration engine. The suggested register settings to maximize test coverage with BIST is provided below.

Table 14. Test Conditions

Register Settings	Expected Result
Reg 05h[14:0]=65, Reg 06h[8:0]=255, Reg10h[4:0] to eg1Ah[4:0]=0d or 0h	Reg 0Fh[15:0]=36092, Reg 09h[23:0]=14942167
Reg 05h[14:0]=32702, Reg 06h[8:0]=36, Reg10h[4:0] to Reg1Ah[4:0]=31d or 1Fh	Reg 0Fh[15:0]=55027, Reg 09h[23:0]=14143649
Reg 05h[14:0]=10922, Reg 06h[8:0]=170, Reg10h[4:0] to Reg1Ah[4:0]=10d or Ah	Reg 0Fh[15:0]=28618, Reg 09h[23:0]=8907563
Reg 05h[14:0]=21845, Reg06h[8:0]=853, Reg10h[4:0] to Reg1Ah[4:0]=21d or 15h	Reg oFg[15:0]=16368, Reg 09h[23:0]=3396981

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Register Map

Table 15. Reg 00h - Chip_ID (Read Only)

Bit	Name	Width	Default	Description
[23:0]	Chip_ID	24	D7780	HMC1023LP5E Chip_ID.

Table 16. Reg 00h - Read Address (Write Only)

Bit	Name	Width	Default	Description
[4:0]	Register Read Address	5	-	Address of the register to be read on the next read/write cycle.
[5]	Soft Reset	1	-	Soft Reset. 1: Soft reset. It is recommended to set this bit to 0 after soft reset event (ie. after writing Reg 00h[5] = 1) 0: No change
[23:6]	Not Defined	1	-	Don't Care.

Table 17. Reg 01h - Enable

Bit	Name	Width	Default	Description
[0]	OTP_DontUse	1	0	Default use stored OTP values (only if OTP is programmed)
[1]	cal_enable	1	0	Enable RC Calibration circuit
[2]	filter_I_enable	1	1	Enable I channel gain stage, filter, and driver
[3]	filter_Q_enable	1	1	Enable Q channel gain stage, filter, and driver
[4]	force_cal_code	1	0	Force calibration setting to use SPI values (Reg 03h - Calibration)
[5]	doubler_enable	1	0	0-- Doubler Disabled. RC Calibration clock 40 MHz<RC calibration clock<80 MHz 1 -- Doubler Enabled. RC Calibration clock 20 MHz<RC calibration clock<40 MHz Note: calibration clock duty cycle must be within 50% +/- 10%
[8:6]	reserved	3	000	
[9]	LSB_Zinput_select	1	0	Sets the I and Q channel input impedances together with Reg 01h[9]. Reg 02h[10] Reg 01h[9] impedance 0 0 1000 Ω (default) 0 1 400 Ω 1 x 100 Ω (Reg 02h[10] and One Time Programmable memory Reg 0Ah[15] select between 100 Ω and 1000/400 Ω)
[23:10]	unused			

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Table 18. Reg 02h - Settings

Bit	Name	Width	Default	Description
[1:0]	opamp_bias[1:0]	2	01	Opamp bias setting. 00 -- min bias 11 -- max bias opamp_bias[1:0]=01 standard bias (characterized value) opamp_bias[1:0]=10 high linearity bias
[3:2]	drvr_bias[1:0]	2	10	Driver bias setting. 00 -- min bias 11 -- max bias drvr_bias[1:0]=10 standard bias (characterized value)
[4]	gain_10dB	1	0	VGA gain setting. 0: 0dB VGA gain 1: 10dB VGA gain
[5]	bypass_filter	1	0	Filter bypass setting. 0: Filter bypass disabled 1: Filter bypass enabled
[9:6]	coarse_bandwidth_code[3:0]	4	0000	Sets filter coarse tuning range 0000 - 5 MHz 0001 - 7 MHz 0010 - 10 MHz 0011 - 14 MHz 0100 - 20 MHz 0101 - 28 MHz 0110 - 40 MHz 0111 - 50 MHz 1000 - 72 MHz
[10]	MSB_Zinput_select	1	0	Sets the I and Q channel input impedances together with Reg 01h[9]. Reg 02h[10] Reg 01h[9] impedance 0 0 1000 Ω (default) 0 1 400 Ω 1 x 100 Ω (Reg 02h[10] and One Time Programmable memory Reg 0Ah[15] select between 100 Ω and 1000/400 Ω)
[23:11]	unused			

Table 19. Reg 03h - Calibration

Bit	Name	Width	Default	Description
[3:0]	fine_bandwidth_code[3:0]	4	0000	fine bandwidth setting override bits (register 01 bit 4, force_cal_code, must be set). 0000 - Minimum frequency 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 - Maximum frequency
[23:4]	unused			

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Table 20. Reg 04h - Calibration/RC-BIST Strobe

Calibration strobe register is used only to initialize a calibration cycle. Writing any value to this register serves to request a new calibration cycle.

Note that this register is also used to start the Built In Self Test (RC-BIST) mode and this is used to test the fault coverage of the RC calibration engine.

Bit	Name	Width	Default	Description
[23:0]	Request calibration	1	0	Writing to any bit in this register starts a calibration cycle.

Table 21. Reg 05h - Clk Period

Bit	Name	Width	Default	Description
[14:0]	clock_period[14:0]	15	0000h	Sets the clock period for the RC calibration circuit. Clock period entered is in pico seconds. i.e. 1/40 MHz clock =25000ps= 110000110101000b=61A8h
[23:15]	unused			

Table 22. Reg 06h - Measure Adjust

Correction value used to adjust RC Calibration result. Value is in 1.024ns increments.

Bit	Name	Width	Default	Description
[8:0]	meas_adj[8:0]	9	000h	Correction value to ADD to counter output before counter is decoded for calibration setting. Number is in 2's complement format. Note this applies to all settings universally.
[23:9]	unused			

Table 23. Reg 07h Unused

Table 24. Reg 08h - Calibration Status (read only)

Bit	Name	Width	Default	Description
[3:0]	fine_bandwidth_code[3:0]	4	0000	fine_bandwidth_setting (must run a calibration cycle to get valid data) Valid states are 0000 to 1011 (see Table 3. Reg 03h - Calibration)
[4]	cal_busy	1		Calibration active flag
[5]	OPT _write_busy	1		OTP write active flag
[23:6]	unused			

Table 25. Reg 09h - Calibration Count (read-only)

Bit	Name	Width	Default	Description
[23:0]	count_read[23:0]	24		Output of calibration counter in pico seconds (unadjusted)

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Table 26. Reg 0Ah - OTP Values (read-only)

Bit	Name	Width	Default	Description
[3:0]	OTP_fine_bandwidth_ code[3:0]	4		Non volatile fine_bandwidth_code[3:0]. Definition is same as per “Reg 03h - Calibration”
[6:4]	OTP_course_bandwidth_ code[2:0]	3		Non volatile version of SPI values found in Reg 02h[6:8]
[7]	OTP_Gain_10dB	1		Non volatile version of SPI values found in “Reg 02h - Settings”
[8]	OTP_bypass_filter	1		
[10:9]	OTP_opamp_bias[1:0]	2		
[12:11]	OTP_drvr_bias[1:0]	2		
[13]	OTP_prg_flag	1		This flag must be set if the OTP values are to be used and must be set by the user. If not set, this flag overrides bit 0 of Reg 01h.
[14]	OTP_Coarse_Bandwidth[3]			Non volatile version of SPI values found in Reg 02h[9]
[15]	OTP__Zinput_select	1		Non volatile version of SPI value found in Reg 02h[10]
[23:16]	unused			

Table 27. Reg 0Bh - OTP Write Enable

Bit	Name	Width	Default	Description
[0]	EFR_Write_enable	1	0	Enables OTP Programming
[23:1]	unused			

Table 28. Reg 0Ch - OTP Write

OTP address register is used in programming of OTP.

Bit	Name	Width	Default	Description
[3:0]	OTP Address	4	0	Address of OTP bit to be set
[23:4]	unused			

Table 29. Reg 0Dh - OTP Write Pulse

OTP strobe register is used in programming of OTP.

Bit	Name	Width	Default	Description
[23:0]	reserved	1	0	reserved

Table 30. Reg 0Eh - RC-BIST Enable

Bit	Name	Width	Default	Description
[0]	enable_RCBIST_mode	1	0	RC-BIST mode enable
[23:1]	unused			

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Table 31. Reg 0Fh - RC-BIST Out

Bit	Name	Width	Default	Description
[15:0]	crc_BIST[15:0]	16	0	RC-BIST CRC check result
[16]	crc_RC-BIST_busy_flag	1	0	RC-BIST busy flag. Indicates that BIST cycle is not completed and data crc_BIST[15:0] is invalid
[23:17]	unused			

Table 32. Reg 10h to Reg1A - Window Threshold

OTP strobe register is used in programming of OTP.

Bit	Name	Width	Default	Description
[23:0]	reserved			reserved

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9