# 1.0  Introduction

### 1.1 Overview

AMIS-492x0 Fieldbus MAU (media access unit) is a transceiver chip for low speed FOUNDATION Fieldbus® and Profibus® PA devices.  The AMIS-49200 was originally designed to be a near pin-for-pin replacement of the Yokogawa μSAA22Q MAU.  "Near pin-for-pin" means that associated component values may change, but no board changes are required.  A micro-leadframe package option (NQFP) is also available, the AMIS-49250.

### 1.2 Definitions, Acronyms and Abbreviations

| | |
|---|---|
| IC | - Integrated circuit |
| ESD | - Electrostatic discharge |
| FF | - FOUNDATION Fieldbus |
| LQFP | - Low profile quad flat pack |
| Manchester | - Communications encoding scheme implemented in FOUNDATION Fieldbus |
| MAU | - Medium attachment unit |
| MDS | - Medium dependent sub-layer |
| NQFP | - "Near chip-scale" quad flat pack |
| μSAA22Q | - Name of Yokogawa's MAU IC |

### 1.3 References

- Fieldbus Medium Attachment Unit (MAU) Chip, μSAA22Q, Yokogawa Electric Corporation, June 12, 1998, Document No.: SS-96-01 (Rev.3).
- Fieldbus Standard for Use in Industrial Control Systems Part 2: Physical Layer Specification and Service Definition, Amendment to Clause 22 ISA/SP50 –1996-544B, dS50.02, Part 2, Draft Standard.
- Profibus PA specifications EN 50170 (formerly DIN 19245) covers all of Profibus and includes PA (31.25 kbps Intrinsically Safe Physical Layer), references IEC 61158-2.

# AMIS-492x0

## 2.0 AMIS-492x0 Fieldbus MAU Description

### 2.1 Features

AMIS-492x0 Fieldbus MAU is a transceiver IC for low speed FOUNDATION Fieldbus and Profibus PA devices.  It incorporates the following features:

- All node power can be supplied by the bus, via the AMIS-492x0
- Current consumption 500uA (typ)
- VCC voltage: 6.2V to 4.75V
- VDD voltage: 5.5V to 2.7V
- Compatible to IEC 1158-2 and ISA 50.02
- Shunt regulator
- Voltage reference (internal only)
- Series regulator
- Band-pass filter
- Slew rate control
- Segment current control
- Low voltage detection
- Carrier detect
- Data rate: 31.25kbps voltage mode
- Dual voltage supply 3-6.2V
- 44-pin LQFP/NQFP package
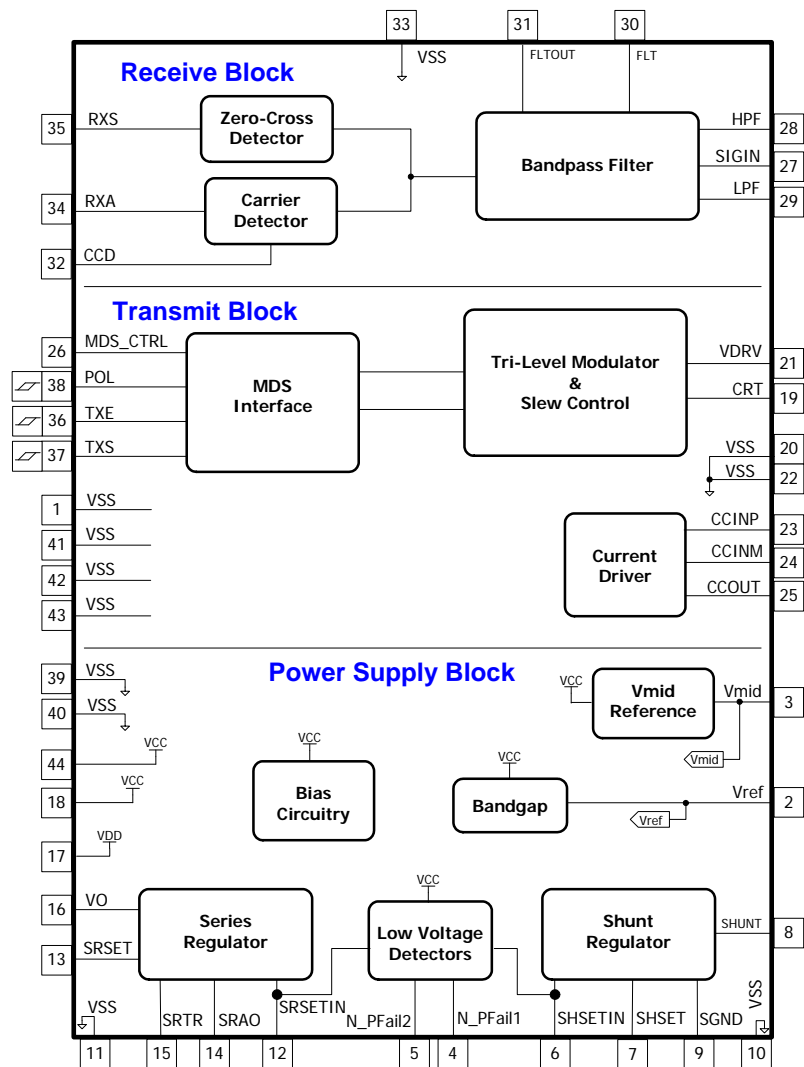
# AMIS-492x0

## 2.2 Block Diagram



*Figure 1: AMIS-492x0 Fieldbus MAU Block Diagram*

# AMIS-492x0

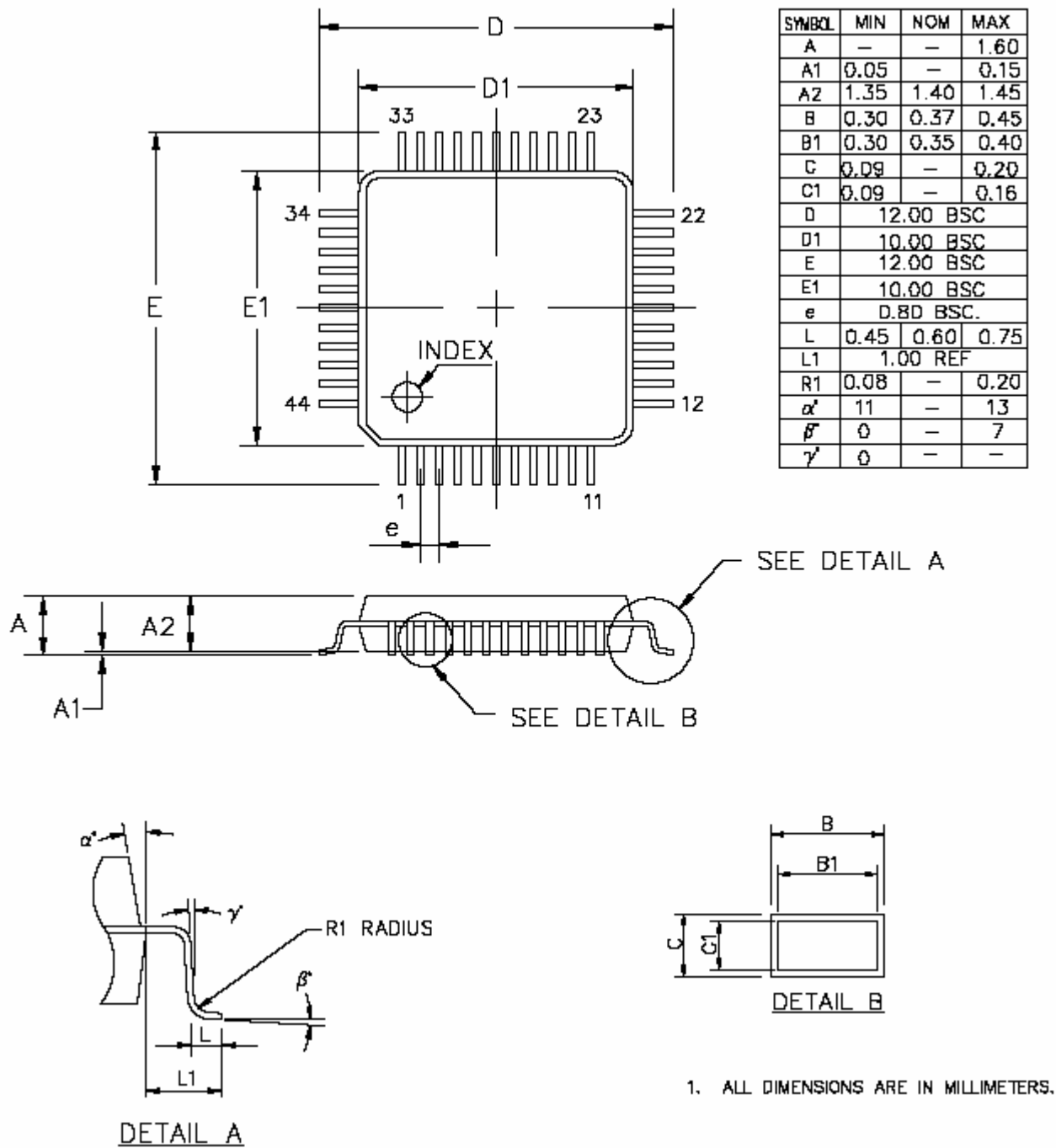## 2.3 Package Information

The IC is packaged as shown below.

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| B | 0.30 | 0.37 | 0.45 |
| B1 | 0.30 | 0.35 | 0.40 |
| C | 0.09 | — | 0.20 |
| C1 | 0.09 | — | 0.16 |
| D | 12.00 BSC | | |
| D1 | 10.00 BSC | | |
| E | 12.00 BSC | | |
| E1 | 10.00 BSC | | |
| e | 0.80 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| R1 | 0.08 | — | 0.20 |
| $\alpha$ | 11 | — | 13 |
| $\beta$ | 0 | — | 7 |
| $\gamma$ | 0 | — | — |

33  23

34  22

E  E1

INDEX

44  12

1  11

e

SEE DETAIL A

A  A2

A1

SEE DETAIL B

R1 RADIUS

DETAIL A

B

B1

C  C1

DETAIL B

1. ALL DIMENSIONS ARE IN MILLIMETERS.

*Figure 2: AMIS-49200 Package Dimensions (44-pin LQFP)*

# AMIS-492x0



| SYMBOL | COMMON DIMENSIONS | | | NOTE |
|---|---|---|---|---|
| | MIN. | NOM. | MAX. | |
| A | 0.80 | 0.85 | 0.90 | |
| A1 | 0.00 | 0.01 | 0.05 | 10 |
| A2 | 0.60 | 0.65 | 0.70 | |
| A3 | | 0.20 REF. | | |
| D | | 7.00 BSC | | |
| D1 | | 6.75 BSC | | |
| E | | 7.00 BSC | | |
| E1 | | 6.75 BSC | | |
| 0 | 0 | - | 12° | |
| P | 0.24 | 0.42 | 0.60 | |
| Q | 0.30 | 0.40 | 0.65 | 8,11 |
| R | 0.13 | 0.17 | 0.23 | 8,11 |

| SYMBOL | PITCH VARIATION | | | NOTE |
|---|---|---|---|---|
| | MIN. | NOM. | MAX. | |
| e | | 0.50 BSC | | |
| N | | 44 | | 3 |
| Nd | | 11 | | 3 |
| Ne | | 11 | | 3 |
| L | 0.30 | 0.40 | 0.50 | |
| b | 0.18 | 0.23 | 0.30 | 4 |
| D2 | 5.40 | 5.50 | 5.60 | 12 |
| E2 | 5.40 | 5.50 | 5.60 | 12 |

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED
   BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE
   PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS NOT TO SCALE.

7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
10. APPLIED ONLY FOR TERMINALS.
11. Q AND R APPLIES ONLY FOR STRAGHT TIEBAR SHAPES.
12. EXPOSED PAD VARIATION

*Figure 3: AMIS-49250 Package Dimensions (44-pin NQFP)*

# AMIS-492x0

Table 1: Pin Numbers and Signal Description

| Signal Name | Pin No. | I/O (Note 1) | Description |
|---|---|---|---|
| VSS | 1 | Ground | Connect to ground |
| VREF | 2 | AO | Internal bandgap voltage (1.18V) |
| VMID | 3 | AO | 2V bias voltage for AC signals |
| N_PFAIL1 | 4 | AI/O | Power fail alarm at VCC input. This pin is an open-drain output of negative logic. |
| N_PFAIL2 | 5 | AI/O | Power fail alarm at VDD input. This pin is an open-drain output of negative logic. |
| SHSETIN | 6 | AI | Feedback (non-inverting) input for the shunt regulator |
| SHSET | 7 | AO | Divided voltage of VCC input.  Feeding this voltage to SHSETIN pin results in 5V voltage at VCC. |
| SHUNT | 8 | AI | Control pin of the shunt regulator. Its sink current (25mA max) is controlled so that the voltage at SHSETIN is equal to $V_{REF}$ (1.18V). |
| VSS/ SGND | 9 | Ground | The current absorbed by SHUNT pin (25mA max) is fed to this pin, which must be connected to the ground level |
| VSS | 10 | Ground | Ground |
| VSS | 11 | Ground | Ground |
| SRSETIN | 12 | AI | Feedback (inverting) input for the series regulator. The series regulator controls its output (SRAO) to make this input voltage is equal to VREF (1.18V). |
| SRSET | 13 | AO | Divided voltage of VO output. Feeding this voltage into SRSETIN pin results in 3V at VO pin. |
| SRAO | 14 | AO | Output pin of an operational amplifier for the series regulator |
| SRTR | 15 | AI | Gate of a PMOS transistor for the series regulator |
| VO | 16 | AO | Output pin of the series regulator (20mA max) |
| VDD | 17 | Digital supply | Supply voltage input for digital block |
| VCC | 18 | Analog supply | Analog supply voltage |
| CRT | 19 | AI/O | Current integration to limit output slew rate |
| VSS | 20 | Ground | Ground |
| VDRV | 21 | AO | Output of an operational amplifier for slew rate control. This signal can be fed to current driver. |
| VSS | 22 | Ground | Ground |
| CCINP | 23 | AI | Non-inverting input of an operational amplifier for transmission current driver |
| CCINM | 24 | AI | Inverting input of an operational amplifier for transmission current driver |
| CCOUT | 25 | AO | Output of an operational amplifier for transmission current driver |
| MDS_CTRL | 26 | AI | For POL = VDD MDS_CTRL should = VSS<br>For POL = VSS MDS_CTRL can be tied to VDD or used as a not reset to control when transmit communications will be enabled |
| SIGIN | 27 | AI | Input pin of the band-pass filter. This pin is connected to VMID bias level with 270K resistor. |
| HPF | 28 | AI | Feedback signal of high-pass filter.  This pin is connected to the output of an op-amp for high pass filter with 75K resistor. |
| LPF | 29 | AI | Non-inverting input of an operational amplifier for the low-pass filter |
| FLT | 30 | AI | Input pin of low-pass filter for feedback. This pin is connected to the output of the high-pass filter through 20kΩ and the non-inverting input of the low-pass filter through 54kΩ resisters. |
| FLTOUT | 31 | AO | Output of the operational amplifier for the low-pass filter.  This signal is internally connected to non-inverting input to form a voltage-follower. |
| CCD | 32 | AO | Current integration (for carrier detect circuit) |
| VSS | 33 | Ground | Ground |

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Table 1: Pin Numbers and Signal Description (Continued)

| Signal Name | Pin No. | I/O(Note 1) | Description |
|---|---|---|---|
| RXA | 34 | DO | MDS-MAU interface signal for received signal activity. This pin is a push-pull output. |
| RXS | 35 | DO | MDS-MAU interface signal for received signal.  This pin is a push-pull output. |
| TXE | 36 | DIS | MDS-MAU interface signal for enable signal transmission (Schmitt Trigger input) |
| TXS | 37 | DIS | MDS-MAU interface signal for signal to be transmitted (Schmitt Trigger input) |
| POL | 38 | DIS | Selects polarity of TxE input.  When this pin is connected to GND, TxE is active high.  When this pin is connected to VDD, TxE is active low. |
| VSS | 39 | Ground | Ground |
| VSS | 40 | Ground | Ground |
| VSS | 41 | Ground | Connect to ground |
| VSS | 42 | Ground | Connect to ground |
| VSS | 43 | Ground | Connect to ground |
| VCC | 44 | Analog supply | Analog supply voltage |

Note:
1.   AI = Analog Input, AO = Analog Output, AI/O = Analog Input/Output,  DIS = CMOS Digital Input (Schmitt Trigger),
      DO = CMOS Digital Output.

# 3.0 Electrical Characteristics

## 3.1 Operating Conditions

Unless otherwise noted, all block and sub-block specifications apply over the operating temperature (-40 to 85$^o$C).

Table 2: Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| Analog block supply voltage | $V_{CC}$ | -0.3 | 6.5 | V | |
| Digital block supply voltage | $V_{DD}$ | -0.3 | 6.0 | V | |
| Digital input pin voltage | $V_{IN}$ | -0.3 | $V_{DD}$ + 0.3 | V | (TxS, TxE and POL pins) |
| Digital output pin voltage | $V_{OUT}$ | -0.3 | $V_{DD}$ + 0.3 | V | (RxS and RxA pins) |
| Input pin current | $I_{IN}$ | - | ±5 | mA | Not for shunt pin |
| Output pin current | $I_{OUT}$ | - | 30 | mA | For shunt, SGND and VO |
| ESD, Human Body Model | | | 2,250 | V | |
| ESD, Machine Model | | | 250 | V | |
| ESD, Charged Device Model | | | 1,000 | V | |
| Storage temperature | $T_{Storage}$ | -55 | 125 | °C | |

Table 3: Normal Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Analog supply voltage | VCC | 4.75 | 5 | 6.2 | V | Supply voltages are configurable, or can be supplied from off-chip |
| Digital supply voltage | VDD | 2.7 | 3 | VCC - 1.1V | V | |
| Storage temperature | $T_{Operating}$ | -40 | | 85 | °C | |
| Current consumption | ICC | | 500 | 800 | µA | 25°C, SHUNT current = 1mA, No current from series regulator |

# AMIS-492x0

Table 4: CMOS Input Specifications

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | $0.7 \bullet V_{DD}$ | $V_{DD}$ | V |
| Input low voltage | $V_{IL}$ | 0 | $0.3 \bullet V_{DD}$ | V |
| Input high current | $I_{IH}$ | | 1 | µA |
| Input low current | $I_{IL}$ | | -1 | µA |
| Schmitt negative threshold | Vt- | $0.2 \bullet V_{DD}$ | | V |
| Schmitt positive threshold | Vt+ | | $0.8 \bullet V_{DD}$ | V |
| Schmitt hysteresis | Vh | 1 | | V |

## 3.2 Power Supply Blocks

Table 5: Regulator Specifications

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Shunt Regulator** | | | | | | |
| Output voltage | $V_{CC}$ | 4.85 | 5.0 | 5.15 | V | Preset, $I_{SH}$ = 1 to 5mA |
| | | 4.75 | | 6.2 | V | External setting |
| Sink current | $I_{SH}$ | 0.001 | | 25 | mA | Internal pass transistor N-ch and pad |
| Load capacitance | $C_{SH}$ | 5 | | | µF | |
| Load regulation | | 0 | 1.6 | 4 | % | $I_{SH}$ = 1 to 25mA |
| Temperature coefficient | $TC_{Vcc}$ | | | ±200 | ppm/°C | No load capacitance |
| **Series Regulator** | | | | | | |
| Input voltage | $V_{CC}$ | 4.75 | | 6.2 | V | Internally tied to $V_{CC}$ pin |
| Output voltage | $V_O$ | 2.91 | 3.0 | 3.09 | V | Preset, $I_{SR}$ = 0 |
| | | 2.85 | | 3.5 | V | External setting and N-JFET |
| Output current | $I_{SR}$ | | | 20 | mA | Internal pass transistor P-ch and pad |
| Load capacitance | $C_{SR}$ | 5 | | | µF | For stability use Cap w/ ESR |
| Load regulation | | 0 | 2 | 4 | % | $I_{SR}$ = 0 to 20mA |
| Temperature coefficient | $TC_{Vo}$ | | ±200 | | ppm/°C | |
| **Low Voltage Detectors (applies to N_PFail1 and N_PFail2)** | | | | | | |
| Threshold | $V_{TH9}$ | 85 | 90 | 95 | % Vref | SxSETIN > $V_{TH9}$ (output: L → H) |
| Hysteresis | $V_{HYS5}$ | .012 | .025 | .038 | V | SxSETIN < ($V_{TH9}$ - $V_{HYS5}$) (output: H → L ) |
| Output sink current | $I_{OL}$ | 30 | | 135 | µA | $V_{OL}$= 0.4V (open drain) |
| Output leakage current | $I_L$ | | | 1 | µA | $V_{OH}$ = 5V |

Table 6: Voltage Reference Specifications

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Bandgap Voltage Reference** | | | | | | |
| Output voltage tolerance | $V_{REF}$ | 1.157 | 1.185 | 1.205 | V | Equates to: +/- 2 percent |
| Temperature drift | | | 50 | | ppm/°C | |
| Hysteresis [1] | $V_{REFHYS}$ | - | 100 | - | µV | Note 1 |
| Supply voltage | $V_{CCREF}$ | 4.75 | 5 | 6.2 | V | |
| Load current | $I_{REFOUT}$ | - | - | 0 | µA | No load during operation |
| **$V_{MID}$ voltage reference** | | | | | | |
| Output voltage | $V_{MID}$ | 1.95 | 2.0 | 2.05 | V | |
| Output current | $I_{MID}$ | -30 | | 100 | µA | |
| Load capacitance | $C_{MID}$ | 0.01 | 0.1 | 1 | µF | DVC6000F uses 1uF |
| Temperature coefficient | $TC_{MID}$ | | | ± 200 | ppm/°C | |

Notes:
1. Hysteresis is defined as the change in the 25°C reading after 85°C to 25°C cycle and –40°C to 25°C cycle.

# AMIS-492x0

## 3.3 Transmitter Blocks

Table 7: MDS-MAU Interface

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **MDS-MAU Interface** | | | | | | |
| POL input pin | POL | | | | V | |
| TxE input pin | TxE | See Schmitt Trigger input specs | | | V | |
| TxS input pin | TxS | | | | V | |

Note: The associated MDS chip must handle the jabber detect function.

Table 8: Tri-level Modulator

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Tri-level Modulator and Slew Control** | | | | | | **(Output is at VDRV)** |
| Output voltage | $V_O$ | $V_{MID}$ | | 3.02 | V | |
| Load current | $I_O$ | -35 | | +120 | μA | $|\Delta V|$ 10mV |
| Output for silence [1] | $V_S$ | $V_{MID}$+0.485 | $V_{MID}$+0.500 | $V_{MID}$+0.515 | V | TXE disabled |
| Output for high level [1] | $V_H$ | $V_S$+0.380 | $V_S$+0.400 | $V_S$+0.420 | V | TXE active |
| Output for low level [1] | $V_L$ | $V_S$-0.420 | $V_S$-0.400 | $V_S$-0.380 | V | TXE active |
| Asymmetry of $V_H$ and $V_L$ | $\Delta V_{HL}$ | -0.02 | | 0.02 | V | |
| Rise and fall times [2] | tf, tr | | 4.7 | | μsec | Note 2 ($C_{RT}$= 22pF) |

Notes:
1. Nominal values are: $V_S$ = 2.5V, $V_H$ = 2.9V and $V_L$ = 2.1V.
2. By adding an external capacitor between the CRT pin and ground, slew rate at VDRV output can be controlled. The controlling equation is tf or tr = 2us + (0.123us/pF * $C_{RT}$). $C_{RT}$ is nominally 22pF, yielding tf = tr =4.7us. The constant comes from an internal capacitor. The hot side of the capacitor and the CRT pin should have a guard pattern around them to avoid unnecessary interference.

Table 9: Current Control Amplifier

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Current Control Amplifier** | | | | | | **(Output is at CCOUT)** |
| Input common mode voltage range | $V_{CM}$ | 0 | | $V_{CC}-1$ | V | |
| Output voltage swing | $V_O$ | 1 | | $V_{CC}-0.5$ | V | |
| Load current | $I_o$ | -2300 | | 100 | μA | |
| Input offset voltage | $V_{OS}$ | -3 | | +3 | mV | |
| Slew rate | SR | | 0.54 | | V/μs | $C_L$= 10pf $R_L$= 200k |
| Gain bandwidth product | GBW | | 1.15 | | MHz | |
| Phase margin | PM | | 66 | | Deg | |

# AMIS-492x0

## 3.4 Receiver Block

Table 10: Receiver Sub-blocks

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Band Pass Filter** | | | | | | |
| Input voltage | $V_{BP}$ | 1 | | 4 | V | SIGIN pin to GND |
| Output voltage swing | FLTOUT | 1 | | 4 | V | |
| Output slew rate | SR | | 0.6 | | V/µs | |
| Input offset voltage | $V_{OS}$ | | | ± 5 | mV | |
| Filter resistors [1] | RF1 | 60 | 75 | 90 | kΩ | |
| | RF2 | 216 | 270 | 324 | kΩ | |
| | RF3 | 16 | 20 | 24 | kΩ | |
| | RF4 | 43 | 54 | 65 | kΩ | |
| **Carrier Detector** | | | | | | |
| Threshold voltage | $V_{TH+}$ | 40 | 50 | 60 | mV | Relative to $V_{MID}$ |
| | $V_{TH-}$ | -60 | -50 | -40 | mV | |
| Output high voltage | $V_{OH}$ | $V_{DD}$-0.6 | | | V | $I_{OH}$ = 0mA |
| Output low voltage | $V_{OL}$ | | | 0.3 | V | $I_{OL}$ = 0mA |
| Output high current | $I_{OH}$ | 50 | | | µA | $V_{DD}$-$V_O$ ≤ 0.6V |
| Output low current | $I_{OL}$ | 50 | | | µA | $V_O$ ≤ 0.6V |
| Output rising time | $t_R$ | | 0.3 | | µs | $C_L$ = 10pF |
| Output leak current | $t_F$ | | 0.3 | | µs | $C_L$ = 10pF |
| **Zero-cross Detector** | | | | | | |
| Threshold voltage | $V_{TH+}$ | $V_{MID}$+0.025 | $V_{MID}$+0.040 | $V_{MID}$+0.058 | V | No carrier |
| | $V_{TH-}$ | $V_{MID}$ | $V_{MID}$ | $V_{MID}$ | V | Carrier active |
| Output high voltage | $V_{OH}$ | $V_{DD}$-0.6 | | | V | $I_{OH}$ = 0mA |
| Output low voltage | $V_{OL}$ | | | 0.3 | V | $I_{OL}$ = 0mA |
| Output high current | $I_{OH}$ | 50 | | | µA | $V_{DD}$-$V_O$ ≤ 0.6V |
| Output low current | $I_{OL}$ | 50 | | | µA | $V_O$ ≤ 0.6V |
| Output rising time | $t_R$ | | 0.3 | | µs | $C_L$ = 10pF |
| Output leak current | $t_F$ | | 0.3 | | µs | $C_L$ = 10pF |

Note:
1. The band pass filter is made up of a two pole high pass filter in series with a two pole low pass filter. The filter consists of four resistors internal to AMIS-492x0, and four external capacitors. The active part of each filter is an amplifier connected in a follower configuration.

# AMIS-492x0

## 4.0 Theory of Operation

### 4.1 Overview

The AMIS-492x0 incorporates two different power supply circuits. Both derive their power from the bus. Using the internal configuration, the shunt regulator is set for 5V and the series regulator is set for 3V. Users can modify either power supply by adding external components. The AMIS-492x0 Fieldbus can also monitor these power supply voltages and generate power-fail signals if they fall below a specified value. Please refer to the AMIS-492x0 Fieldbus MAU Reference Design Application Note for ways to adjust the shunt and series voltage regulators.

The AMIS-492x0 Fieldbus MAU transmits a Manchester-encoded signal provided from a standard MDS-MAU interface. The output driver makes it possible to design various signal circuits, which depend on the power requirements of your device. The slew rate of the signal can be controlled to minimize unnecessary radiation as specified in IEC/ISA standards.

The AMIS-492x0 Fieldbus MAU has a built-in band pass filter which makes it easy to design your own receiver. The receive block operates on a Manchester-encoded signal. It decodes the signal and verifies proper amplitude with a zero-cross and carrier detect circuit, respectively. Detected signals are then passed on to a controller with the standard MDS-MAU interface.

### 4.2 Power Supply Block

The power supply block contains four sub-blocks:

1.  A shunt regulator - for establishing a supply voltage of $V_{CC}$ (typ. = 5V) used by the analog circuitry
2.  A series regulator - for establishing a supply voltage of $V_{DD}$ (typ. = 3V) used for digital circuitry
3.  Two low voltage detectors - for monitoring the two supply voltages
4.  A bandgap voltage reference - which is used internally for generating a bias level for AC signals

#### 4.2.1. Shunt Regulator

The shunt regulator controls its sink current to the SHUNT pin so that the voltage applied to the SHSETIN pin is equal to $V_{REF}$. The $V_{CC}$ input is divided by an internal network to provide a voltage equal to Vref at the SHSET pin. If SHSET and SHSETIN pins are tied together, and $V_{CC}$ and SHUNT pins are connected to a power source of high impedance (e.g., current mirror circuit of signal driver), the shunt regulator provides 5V power to itself and external circuits. A capacitor of 5μF or larger capacity is necessary to stabilize this regulator. Figure 13 shows C10 (22μF) connected to Pin 8 to accomplish stabilization.

It is possible to increase the $V_{CC}$ voltage up to 6.2V by dividing $V_{CC}$ with an external network to supply the appropriate voltage to SHSETIN pin. In this case, SHSET pin must be kept open. The output voltage is determined by the following equation:

$$V_{CC} = V_{REF} \times (1 + R_1 / R_2)$$
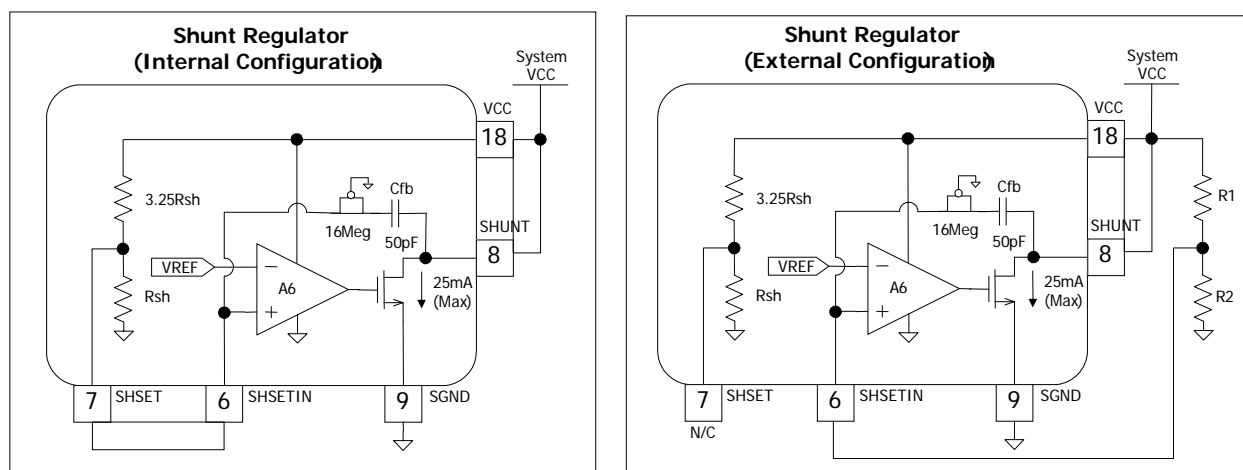


*Figure 4: Shunt Regulator*

# AMIS-492x0

The SHUNT pin is normally connected to $V_{CC}$.  It is possible to insert a resister between $V_{CC}$ and SHUNT to measure the shunt current.  Its value should be small enough to keep $V_{DS}$ (voltage between SHUNT pin and SGND pin) larger than 2.5V (i.e., resistor must be less than 100Ω.).

Since the internal transistor can sink as much as 25mA, no additional circuit is necessary in most cases.  Note that the drain current must not exceed 25mA because no protection is implemented for the internal transistor.  If you do not need the shunt regulator, you should connect SHUNT and SHSETIN pins to GND and open SHSET pin. Then $V_{CC}$ must be supplied from another source.

## 4.2.2. Series Regulator

The series regulator produces a regulated voltage at the $V_O$ pin from $V_{CC}$.  If you connect SRAO and SRTR pins together, the internal amplifier will regulate the input voltage at SRSETIN pin to equal $V_{REF}$.  An internal feedback signal is generated to produce a voltage equal to $V_{REF}$ at pin SRSET.  If you connect SRSET and SRSETIN pins, the series regulator supplies 3V at pin $V_O$.  A capacitor ($C_D$ in Figure 5) of 5μF or larger capacity is necessary to stabilize this regulator. The capacitor is expected to have an ESR resistor for the circuit to be stable. If the capacitor is low, a series resistor with the cap load will help stabilize the circuit).
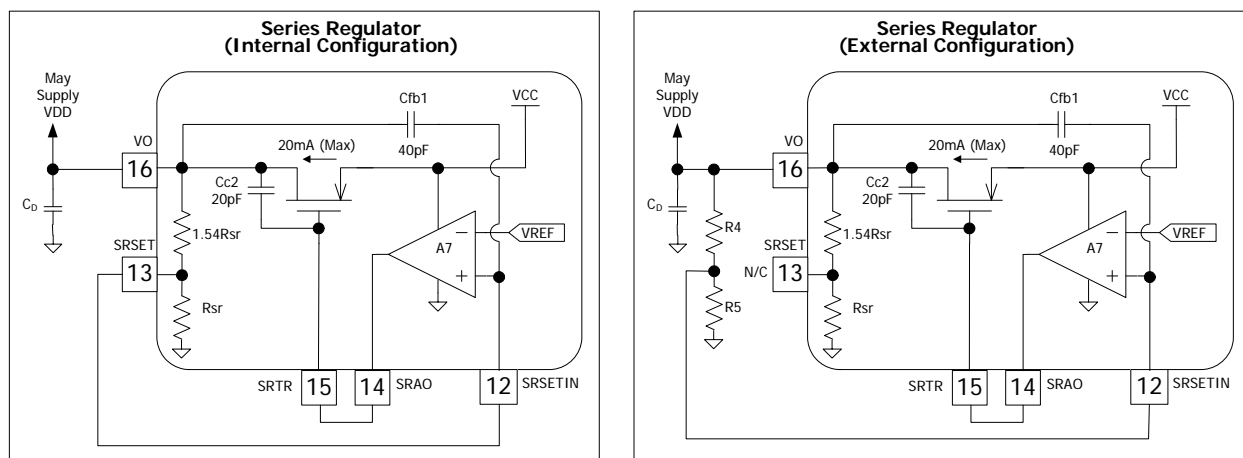


*Figure 5: Series Regulator*

The supply current must not exceed 20mA because no current limiting is applied to the internal transistor.  You can increase $V_O$ voltage up to 3.5V by dividing $V_O$ with an external network to supply the appropriate voltage to pin SRSETIN.  In this case, pin SRSET must be kept open.  The drain-source voltage of the internal transistor must be larger or equal to 2V.  If this condition is not satisfied, you may need an external P-channel JFET to create the desired low voltage-drop regulator. The output voltage is determined by the following equation.

$$VO = VREF \times (1 + R4/R5)$$

## 4.2.3. Low Voltage Detectors

Low voltage detectors are included to monitor supply voltages and generate "power fail" signals.  The low voltage alarms are detected by sensing the voltage on pins SHSETIN and SRSETIN.  These pins also provide feedback for the shunt and series regulators.  If the voltage on the SHSETIN pin is lower than the threshold, VTH9 (90 percent VREF), N_PFAIL1 goes low.  Typically SHSETIN monitors the analog rail voltage VCC.  If the voltage on the SRSETIN pin is lower than the threshold, VTH9, N_PFAIL2 goes low.  Typically SRSETIN monitors the digital rail voltage VDD.

Both outputs are open drain, so a resistor will be required.  If you do not use one of these pins, it should be connected to GND.  You can also add capacitors to delay these signals.  In this case, sink current must not exceed the maximum value.

If you do not wish to use one of the low voltage detectors its corresponding output pin should be connected to GND.

# AMIS-492x0
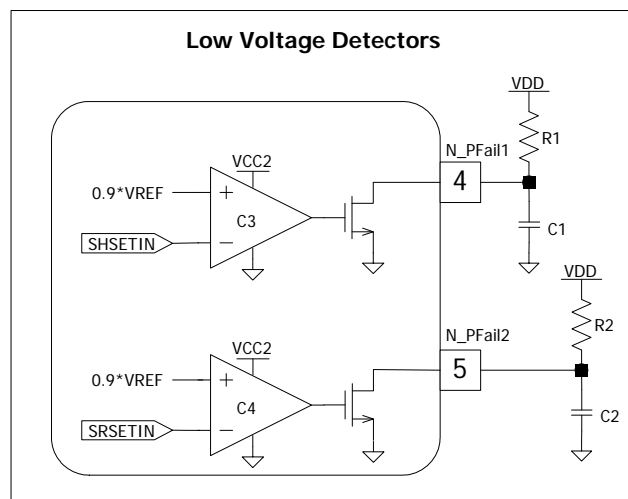


*Figure 6: Low Voltage Detectors*

If you do not use one of the regulators, the corresponding alarm signal can potentially be used to monitor another signal.  For example, if the series regulator is not used, SRAO should be left open, SRTR tied to VCC, VO grounded and SRSET left open.  Then SRSETIN can be the input for monitoring another voltage signal with N_PFAIL2.

### 4.2.4. Voltage Reference

The voltage reference circuitry generates two voltage signals, VREF and VMID.  VREF comes from a bandgap circuit and is used as the reference voltage for all circuits in the AMIS-492x0 Fieldbus MAU.  The typical value for VREF is 1.185V.  See Figure 7.

An operational amplifier is regulating VMID to provide a bias (common) level for the AC signals.  Its typical voltage is 2V.  A capacitor larger than 0.01μF is necessary on VMID to remove high-frequency ripple.
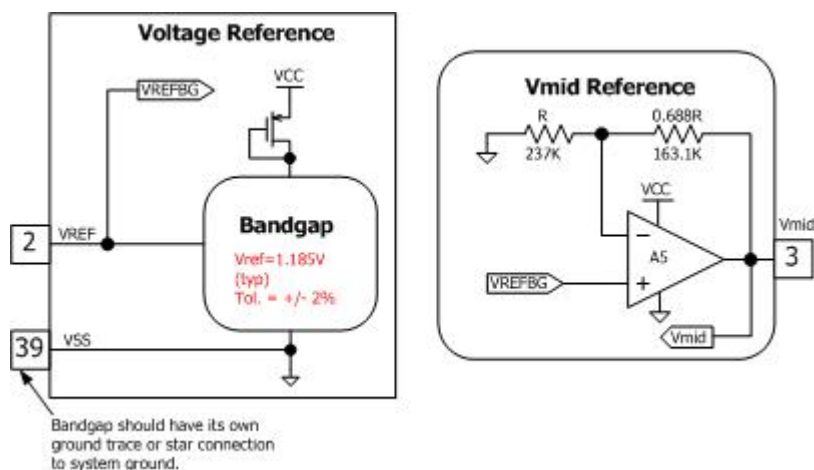


*Figure 7: Bandgap and VMID Voltage Reference*

# AMIS-492x0

## 4.3 Transmit Block

The transmit block contains four sub-blocks:

1. MDS-interface – decodes input signals to generate internal control signals.
2. Tri-level modulator – generates current signals used as inputs to the slew-rate controller.
3. Slew rate controller – converts current to three distinct VDRV voltage levels ($V_S$, $V_H$, $V_L$).
4. Current drive amplifier – op amp designed to drive current drivers for 31.25kbps voltage-mode medium.

### 4.3.1. MDS-interface

The MDS-interface decodes input signals to generate internal control signals. The POL pin is used to select the polarity of TxE (transmit enable). The TxE and TxS (transmit signal) are the MDS-MAU interface signals. These three signals are CMOS logic signals powered by the $V_{DD}$ supply voltage. When POL is connected to GND, TxE is assumed to be active high (positive logic). Likewise, if POL is connected to $V_{DD}$, TxE is assumed to be active low (negative logic). See Table 1 on page 7, Table 11, and Figure 8 to see how MDS_CTRL Pin 26 can be used to control MDS interface operation. Table 11 shows the resulting VDRV output for the various combinations of interface signals.

Table 11: MDS-interface Logic

| POL | TxE | TxS | VDRV |
|-----|-----|-----|------|
| Low | Low | Low | $V_S$ |
| | | High | |
| | High | Low | $V_H$ |
| | | High | $V_L$ |
| High | Low | Low | $V_H$ |
| | | High | $V_L$ |
| | High | Low | $V_S$ |
| | | High | |
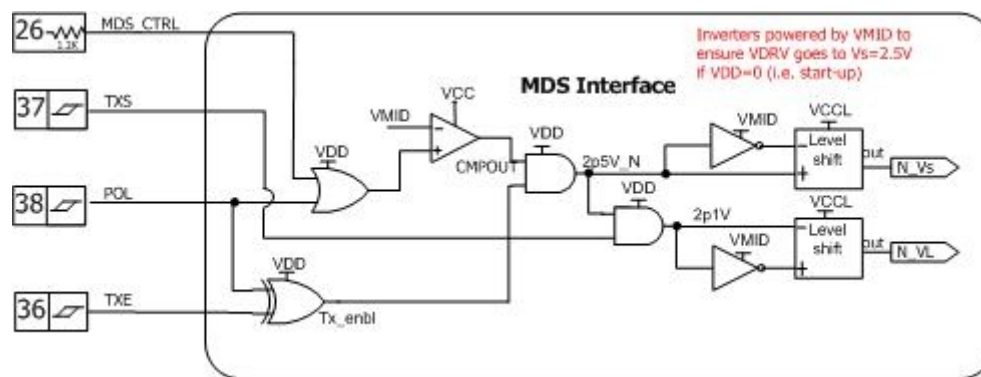


*Figure 8: MDS Interface*

### 4.3.2. Tri-level Modulator

The tri-level modulator switches current signals into a summing node. The slew rate controller converts the current to a voltage signal, VDRV. The DC level of silence ($V_S$) is nominally 2.5V. Transmission high ($V_H$) is nominally 2.9V and transmission low ($V_L$) is nominally 2.1V, yielding an amplitude of 0.8V.

# AMIS-492x0
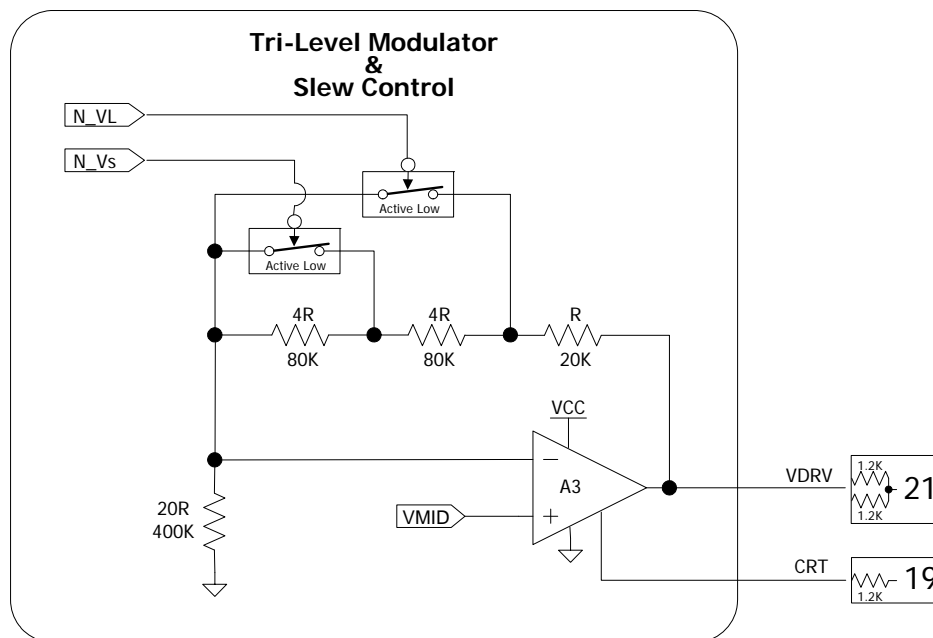


*Figure 9: Tri-level Modulator*

## 4.3.3. Slew Rate Controller

Amplifier (A3), shown in the above figure, controls the slew rate. The amplifier converts the current signals from the tri-level modulator to a voltage signal, VDRV. It controls its slew rate with a capacitor ($C_{RT}$) connected to the CRT pin. The waveform at the VDRV pin is symmetric and the fall/rise times are determined by the following equation:

$$t_F, \ t_R = \ 2.0[\mu s] + 0.12 \ [\mu s/pF] \times C_{RT}$$

The constant part comes from the internal capacitor (not shown). It is recommended to make a guard pattern on your circuit board around the CRT pin and the hot side of $C_{RT}$ to avoid unnecessary interference.

## 4.3.4. Current Drive Amplifier

The drive amplifier is an operational amplifier optimized to drive current drivers for 31.25kbps voltage-mode medium. Its input and output signals are exposed to allow flexible design of the external driver. Note that this amplifier cannot directly sink the necessary current from the medium. In the following drive circuit the current ($I_{BUS}$) through the current-detect resister ($R_F$) is determined by the following equation.

$$I_{bus} = \frac{[\ R_3 \, V_{mid} \, (R_{12} + R_{11})\ ] - [\ V_{drv} \, (R_2 \, R_{11} + R_3 \, R_{11})\ ]}{- [\ R_F \ (\ R_2 \, R_{12} + R_3 \, R_{12})\ ]}$$

A diode and/or a resistor connected to the emitter are necessary to shift the DC level of CCOUT and to suppress the loop gain. The resistance value depends on your design (overall gain and emitter current).

# AMIS-492x0
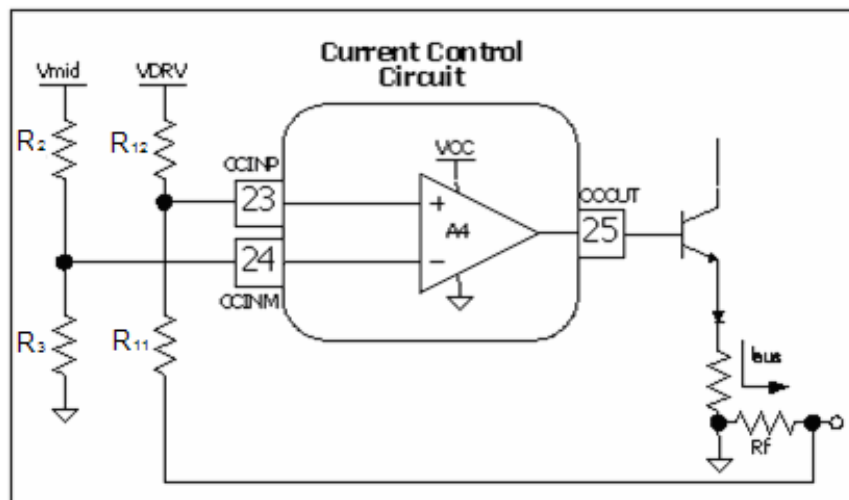


*Figure 10: Current Control Circuit*

## 4.4 Receive Block

The receive block contains three sub-blocks, which are internally connected:

1. A band pass filter – to filter the desired incoming communication signal.
2. Carrier detector – generates the RxA signal by detecting the signal amplitude.
3. Zero-cross detector generates the RxS signal by detecting the high/low transitions of the Manchester code.

### 4.4.1. Band Pass Filter

The band pass filter is a series connection of a high-pass and a low-pass filters each having two poles. Each filter is comprised of a voltage follower and on chip resisters, so only four external capacitors are necessary. The following figure shows an internal circuit and the connection of external capacitors. Cut-off frequency, $f_L$, of the high-pass filter is determined by $C_1$ and $C_2$ while cut-off frequency, $f_H$, of the low-pass filter is determined by $C_3$ and $C_4$.

$$f_L = \frac{1}{2\pi} \sqrt{\frac{1}{R_{F1}*R_{F2}*C_1*C_2}} \qquad\qquad Q_L = \frac{1}{2}\sqrt{\frac{R_{F2}}{R_{F1}}} = 0.95$$

$$f_H = \frac{1}{2\pi} \sqrt{\frac{1}{R_{F3}*R_{F4}*C_3*C_4}} \qquad\qquad Q_L = 0.44*\sqrt{\frac{C_3}{C_4}} = 0.95$$

The possible ranges of $f_L$ and $f_H$ are 1kHz ~ 10kHz and 10kHz ~ 100kHz, respectively. The values in the following figure are recommended to obtain 1kHz and 47.6kHz cut-off frequencies.

# AMIS-492x0



*Figure 11: Band Pass Filter*

### 4.4.2. Receive Signal Detection

The carrier detector generates the receive activity (RxA) signal by detecting the input signal amplitude. Minimum amplitude is 100mVp-p (TYP). A delay, determined by the capacitor connected between the CCD pin and GND, is added to avoid detection of transient noise. The recommended value of $C_{CD}$ is 100pF. The output can drive a CMOS input of $V_{DD}$ supply voltage.

The zero-cross detector generates the receive signal (RxS) with minimum phase error (jitter) by detecting the transition between high and low levels of the incoming Manchester code. Hysteresis of +40mV (TYP) is applied to avoid unnecessary switching by noise. Once the carrier-detect goes active the hysteresis is removed and the switching point threshold is set to Vmid. The output can drive a CMOS input of $V_{DD}$ supply voltage.



*Figure 12: Receive Signal Detectors*

# AMIS-492x0

## 5.0 AMIS-49200 as Replacement for Yokogawa μSAA22Q

The AMIS-49200 is a near pin-for-pin compatible replacement for the Yokogawa μSAA22Q Fieldbus MAU. There are some differences between the two chips both in the internal operation, the required external connections and the value (or existence) of some of the external components. These differences are small and those who used the μSAA22Q would most likely be able to use the AMIS-49200 in designs with only some component value changes.

### 5.1 Functional Differences Between the μSAA22Q and the AMIS-492x0

#### 5.1.1. Jabber Inhibit

The AMIS-492x0 does not implement the Jabber Inhibit function in the μSAA22Q. Typically the AMIS-492x0 will be connected with a link controller chip such as the UFC100-F1 from Aniotek/Softing. This link controller has a Jabber Inhibit function so the absence of this function in the AMIS-492x0 should not be a problem.

As can be seen in Table 12, MDS_CTRL is only connected to ground if POL is connected to VDD.  See Table 1 for a detailed description of the interaction between MDS_CTRL and POL.

In Table 12, the μSAA22Q recommends that the JAB/ signal (Pin 39) be connected to ground if the signal is not used. On AMIS-492x0, Pin 39 must be connected to ground.

#### 5.1.2. Low Power Mode

The low power mode on the μSAA22Q allows the user to have a quiescent current draw of less than 10mA yet still communicate at the proper IEC 61158-2 signal levels. Very few, if any, Fieldbus devices are capable of operating at such a low current level so this capability was not included in the AMIS-492x0.

The pins affected by this are 41, 42 and 43. If the low power mode is not being used on the μSAA22Q, these three pins are grounded. On the AMIS-492x0 it is required that these pins be grounded.

### 5.2 Pin Differences Between the μSAA22Q and the AMIS-492x0

Table 12: Pin Connection Differences Between the μSAA22Q and the AMIS-492x0

| | μSAA22Q | | AMIS-492x0 | |
|---|---|---|---|---|
| Pin No. | Signal Name | Recommended Connection | Signal Name | Required Connection |
| 1 | NC | Ground | VSS | Ground |
| 11 | NC | Ground | VSS | Ground |
| 22 | NC | Ground | VSS | Ground |
| 26 | NC | Ground | MDS_CTRL | Ground* |
| 33 | NC | Ground | VSS | Ground |
| 39 | JAB/ | Ground if not used | VSS | Ground |
| 41 | CJB | 1 μf cap | VSS | Ground |
| 42 | VTX | Ground | VSS | Ground |
| 43 | VSL | Ground | VSS | Ground |

*MDS_CTRL is only connected to ground if POL is connected to VDD. See* Table 1 *for a detailed description of the interaction between MDS_CTRL and POL.*

# AMIS-492x0

## 5.3 External Circuitry

Figure 13 shows the external circuitry required to connect the AMIS-492x0 to an IEC 61158-2 conformant network. This schematic is the circuit that was used to pass the FOUNDATION Fieldbus Physical Layer Conformance test as specified in FOUNDATION Fieldbus specification FF830, Rev 1.5. This circuit is similar but not identical to the circuit recommended by Yokogawa for the µSAA22Q.
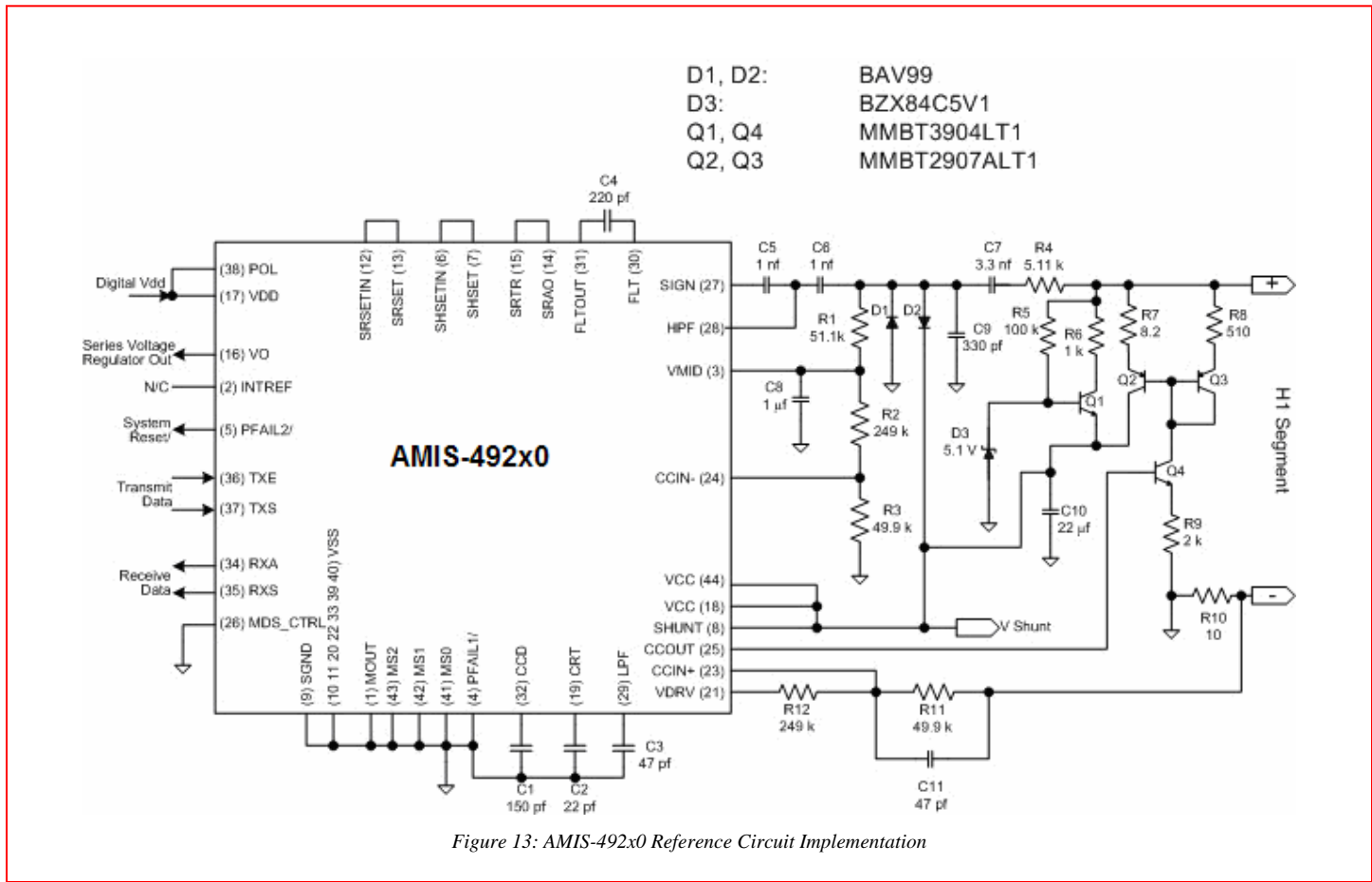


*Figure 13: AMIS-492x0 Reference Circuit Implementation*

Table 13 lists the four external component values that need to be changed with using the AMIS-492x0 in a circuit that previously used the µSAA22Q.

Table 13: Passive External Component Value Differences Between the µSAA22Q and the AMIS-492x0

| Component | µSAA22Q Value | AMIS-492x0 Value |
|---|---|---|
| C1 | 100pf | 150pf |
| C3 | 100pf | 47pf |
| C4 | 470pf | 220pf |
| C8 | 10nf | 1µf |

C1 connects to signal CCD (Pin 32) and controls the carrier detect assert and drop-out timing. Particular implementations may require that the value of C1 be changed to accommodate received signal level changes introduced by the addition of intrinsic safety components added to the external circuitry. C3 and C4 are part of the receive filter and determine the band pass characteristics of the receive filter. It is unlikely that these would need to be changed. C8 is a noise filter for VMID. It is important that VMID have as little noise as possible as it is used as a reference for many sub-circuits in the AMIS-492x0. C8 must be a large capacitor with maximum of 100nf. C8 recommended value is 1µf.

# AMIS-492x0

There is one other minor difference in the recommended external circuitry between the μSAA22Q and the AMIS-492x0. Figure 14 shows the start-up circuits recommended for the μSAA22Q and the AMIS-492x0. The circuit shown for the AMIS-492x0 is different from that shown for the μSAA22Q but either one will work. Both are current sources that turn on when power is applied to the H1 segment terminals so that the AMIS-492x0 can turn on without any turn-on transients on the network.
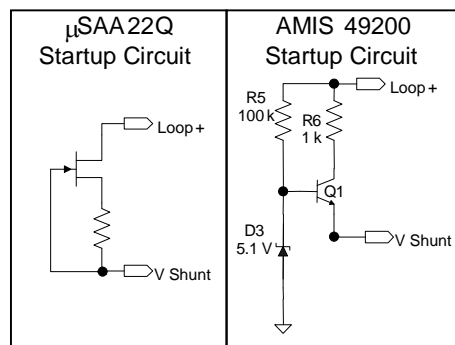


*Figure 14: Recommended Start-up Circuits*

## 5.4 Active Components

Transistors Q1 – Q4 are ordinary small signal transistors. Diodes D1 and D2 are similarly ordinary small signal diodes. Users desiring to replace a μSAA22Q with the AMIS-49200 in an existing design should be able to use whatever transistors and diodes were used with the μSAA22Q. For new designs, the specified transistors can be used or other devices may be chosen.

## 5.5 Alternative Designs

Some users of the Yokogawa μSAA22Q did not use the exact recommended external circuit for the media interface circuit (see Figure 13). Using the AMIS-492x0 without the Yokogawa recommended external circuit may result in some compatibility problems. There are many alternative designs and it is beyond the scope of this document to identify all possible configurations and their associated design implications. Please refer to the AMIS-492x0 Fieldbus MAU Reference Design Application Note for a recommended, FOUNDATION Fieldbus certifiable board design.

## 5.6 Verification

All designs using the AMIS-492x0 should re-run the entire physical layer conformance test as defined in FOUNDATION Fieldbus document FF-830, FOUNDATION™ Specification 31.25 kbit/s Physical Layer Conformance Test. Board layout can alter the behavior of all circuit implementations, even designs that follow the recommended implementation.

# AMIS-492x0

## 6.0 Ordering Information

| Part Number | Package | Shipping Configuration | Temperature Range |
|---|---|---|---|
| AMIS-49200-XTD | 44 LQFP 10x10mm (Green/RoHS Compliant) | Tray | -40°C to 85°C |
| AMIS-49200-XTP | 44 LQFP 10x10mm (Green/RoHS Compliant) | Tape & Reel | -40°C to 85°C |
| AMIS-49250-XTD | 44 NQFP 7x7mm (Green/RoHS Compliant) | Tray | -40°C to 85°C |
| AMIS-49250-XTP | 44 NQFP 7x7mm (Green/RoHS Compliant) | Tape & Reel | -40°C to 85°C |

## 7.0 Appendix (A) – Manchester Encoding

All Fieldbus devices transmit the data onto the media as a Manchester-encoded baseband signal. With Manchester encoding, zeros and ones are represented by transitions that occur in the middle of the bit period (see below). For FOUNDATION Fieldbus H1 and Profibus PA, the nominal bit time is 32$\mu$sec, with the transition occurring at 16$\mu$sec. The Manchester encoding rules have been extended to include two additional symbols, non-data plus (N+) and non-data minus (N-). The symbol encoding rules are shown in Figure 15.
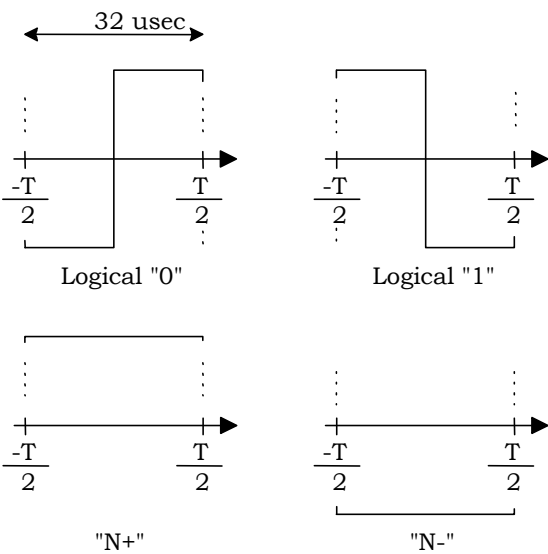


*Figure 15: Manchester Encoding*

# AMIS-492x0

## 8.0 Revision History

| Revision | Date | Modification |
|---|---|---|
| 1 | April 2006 | Initial release |
| 2 | October 2006 | |
| 3 | January 2007 | |
| 4 | February 2008 | Update to new AMIS template |
| 5 | May 2008 | Update to new ON Semiconductor template; update OPN table |
| 6 | June 2008 | Added AMIS-49250 |

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