1. General description

Dual Logic level N-channel MOSFET in an LFPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC-Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- AEC-Q101 compliant
- · Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with V_{GS(th)} rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | | Min | Тур | Max | Unit |
|---------------------|---------------------------------------|--|--|-----|------|------|------|
| Limiting values | Limiting values FET1 and FET2 | | | | | | |
| V _{DS} | drain-source voltage | 25 °C ≤ T _j ≤ 175 °C | | - | - | 80 | V |
| I _D | drain current | V _{GS} = 5 V; T _{mb} = 25 °C; <u>Fig. 2</u> | | - | - | 21 | Α |
| P _{tot} | total power dissipation | T _{mb} = 25 °C; <u>Fig. 1</u> | | - | - | 64 | W |
| Tj | junction temperature | | | -55 | - | 175 | °C |
| Static characte | eristics FET1 and FET2 | | | | • | | |
| R _{DSon} | drain-source on-state resistance | V_{GS} = 5 V; I_D = 10 A; T_j = 175 °C; Fig. 12 | | - | - | 54.5 | mΩ |
| | | $V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 11$ | | - | 15.7 | 21.7 | mΩ |
| Dynamic chara | Dynamic characteristics FET1 and FET2 | | | | | | |
| Q_{GD} | gate-drain charge | I _D = 10 A; V _{DS} = 64 V; V _{GS} = 5 V; | | - | 8.4 | - | nC |
| Q _{G(tot)} | total gate charge | T _j = 25 °C; <u>Fig. 13; Fig. 14</u> | | - | 23.1 | - | nC |



Dual N-channel 80 V, 22 m Ω logic level MOSFET

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|--------------------|----------------|
| 1 | S1 | source1 | 8 7 6 5 | D1 D1 D2 D2 |
| 2 | G1 | gate1 | | |
| 3 | S2 | source2 | | |
| 4 | G2 | gate2 | | |
| 5 | D2 | drain2 | | S1 G1 S2 G2 |
| 6 | D2 | drain2 | | mbk725 |
| 7 | D1 | drain1 | 1 2 3 4 | |
| 8 | D1 | drain1 | LFPAK56D (SOT1205) | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | | | | |
|-------------|----------|---|---------|--|--|--|
| | Name | Description | Version | | | |
| BUK9K22-80E | LFPAK56D | plastic, single ended surface mounted package (LFPAK56D); 8 leads | SOT1205 | | | |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| BUK9K22-80E | 92280E |

Dual N-channel 80 V, 22 m Ω logic level MOSFET

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|----------------------|---|---|---------|-----|-----|------|
| Limiting value | s FET1 and FET2 | | ' | | | |
| V _{DS} | drain-source voltage | 25 °C ≤ T _j ≤ 175 °C | | - | 80 | V |
| V_{DGR} | drain-gate voltage | R_{GS} = 20 k Ω | | - | 80 | V |
| V_{GS} | gate-source voltage | DC; T _j ≤ 175 °C | | -10 | 10 | V |
| | | Pulsed; T _j ≤ 175 °C | [1] [2] | -15 | 15 | V |
| P _{tot} | total power dissipation | T _{mb} = 25 °C; <u>Fig. 1</u> | | - | 64 | W |
| I _D | drain current | V _{GS} = 5 V; T _{mb} = 25 °C; <u>Fig. 2</u> | | - | 21 | Α |
| | | V _{GS} = 5 V; T _{sp} = 100 °C; <u>Fig. 2</u> | | - | 15 | Α |
| I _{DM} | peak drain current | pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; Fig. 3 | | - | 84 | Α |
| T _{stg} | storage temperature | | | -55 | 175 | °C |
| Tj | junction temperature | | | -55 | 175 | °C |
| Source-drain of | liode FET1 and FET2 | | • | • | | |
| I _S | source current | T _{mb} = 25 °C | | - | 21 | Α |
| I _{SM} | peak source current | pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$ | | - | 84 | Α |
| Avalanche rug | gedness FET1 and FET2 | | | | | |
| E _{DS(AL)S} | non-repetitive drain- source avalanche energy | I_D = 21 A; $V_{sup} \le 80$ V; R_{GS} = 50 Ω ; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4 | [3] [4] | - | 116 | mJ |

Accumulated pulse duration up to 50 hours delivers zero defect ppm

^[2]

Significantly longer life times are achieved by lowering T_j and or V_{GS} Single-pulse avalanche rating limited by maximum junction temperature of 175 $^{\circ}$ C

^[3] [4] Refer to application note AN10273 for further information

Dual N-channel 80 V, 22 m Ω logic level MOSFET

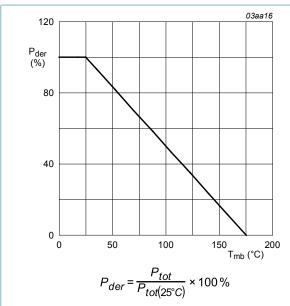


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

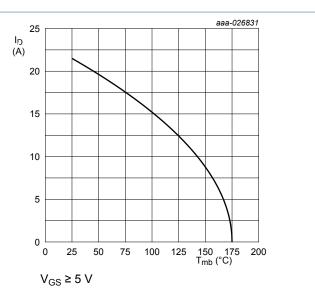


Fig. 2. Continuous drain current as a function of mounting base temperature, FET1 and FET2

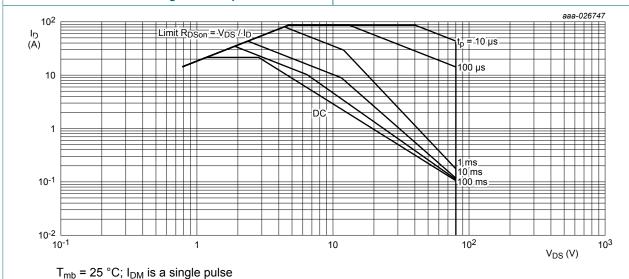
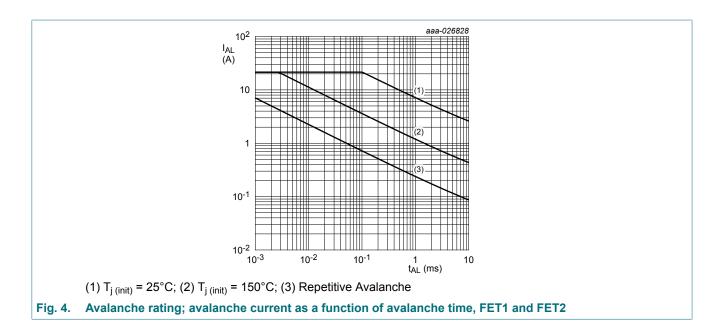


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage, FET1 and

Dual N-channel 80 V, 22 m Ω logic level MOSFET



9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|-----------------------|---|---|-----|-----|------|------|
| R _{th(j-mb)} | thermal resistance from junction to mounting base | Fig. 5 | - | - | 2.36 | K/W |
| R _{th(j-a)} | thermal resistance from junction to ambient | Minimum footprint; mounted on a printed circuit board | - | 95 | - | K/W |

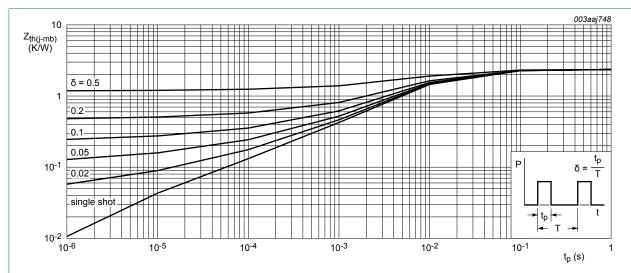


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration, FET1 and FET2

Dual N-channel 80 V, 22 m Ω logic level MOSFET

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|---------------------|-------------------------------|---|----------|------|------|------|
| Static char | acteristics FET1 and FET2 | | | | ' | |
| (D11)D00 | drain-source | I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C | 80 | - | - | V |
| | breakdown voltage | I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C | 72 | - | - | V |
| V _{GS(th)} | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}; Fig. 9;$ Fig. 10 | 1.4 | 1.7 | 2.1 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 10 | - | - | 2.45 | V |
| | | I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C; Fig. 10 | 0.5 | - | - | V |
| I _{DSS} | drain leakage current | V _{DS} = 80 V; V _{GS} = 0 V; T _j = 25 °C | - | 0.01 | 1 | μA |
| | | V _{DS} = 80 V; V _{GS} = 0 V; T _j = 175 °C | - | - | 500 | μA |
| I _{GSS} | gate leakage current | V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C | - | 2 | 100 | nA |
| | | V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C | - | 2 | 100 | nA |
| Doon | drain-source on-state | $V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 11$ | - | 15.7 | 21.7 | mΩ |
| | resistance | V_{GS} = 10 V; I_{D} = 10 A; T_{j} = 25 °C; Fig. 11 | - | 14.4 | 19 | mΩ |
| | | V_{GS} = 5 V; I_D = 10 A; T_j = 175 °C; Fig. 12 | - | - | 54.5 | mΩ |
| Dynamic c | haracteristics FET1 and FE | T2 | <u>'</u> | | | |
| Q _{G(tot)} | total gate charge | I _D = 10 A; V _{DS} = 64 V; V _{GS} = 5 V; | - | 23.1 | - | nC |
| Q _{GS} | gate-source charge | T _j = 25 °C; <u>Fig. 13; Fig. 14</u> | - | 5.4 | - | nC |
| Q _{GD} | gate-drain charge | | - | 8.4 | - | nC |
| C _{iss} | input capacitance | V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; | - | 2342 | 3115 | pF |
| C _{oss} | output capacitance | T _j = 25 °C; <u>Fig. 15</u> | - | 170 | 204 | pF |
| C _{rss} | reverse transfer capacitance | | - | 89 | 122 | pF |
| t _{d(on)} | turn-on delay time | $V_{DS} = 60 \text{ V}; R_L = 5 \Omega; V_{GS} = 5 \text{ V};$ | - | 13.9 | - | ns |
| t _r | rise time | $R_{G(ext)} = 5 \Omega; T_j = 25 ^{\circ}C$ | - | 24.9 | - | ns |
| t _{d(off)} | turn-off delay time | | - | 28.6 | - | ns |
| t _f | fall time | | - | 20.6 | - | ns |
| Source-dra | ain diode FET1 and FET2 | | 1 | | | - |
| V _{SD} | source-drain voltage | $I_S = 10 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 16$ | - | 0.8 | 1.2 | V |
| t _{rr} | reverse recovery time | $I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$ | - | 28.4 | - | ns |
| Q _r | recovered charge | V _{DS} = 25 V; T _i = 25 °C | _ | 33 | | nC |

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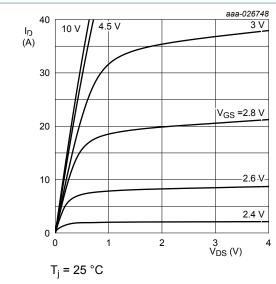


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values, FET1 and FET2

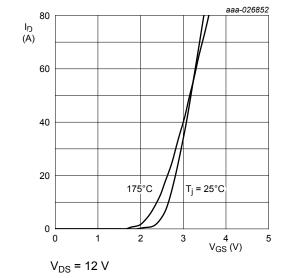


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2

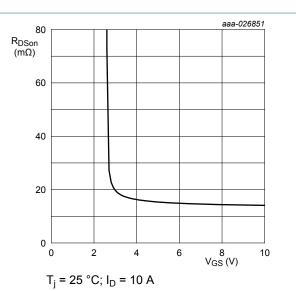
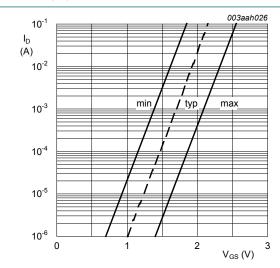


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2



 $T_j = 25 \, ^{\circ}C; \, V_{DS} = 5 \, V$

Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2

Dual N-channel 80 V, 22 mΩ logic level MOSFET

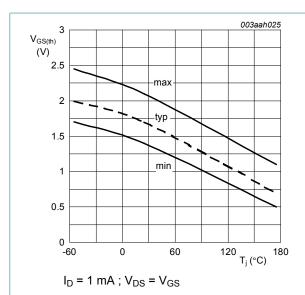


Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2

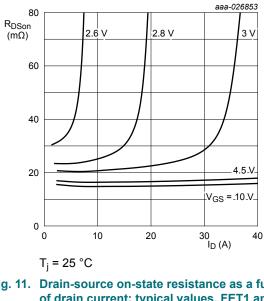


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2

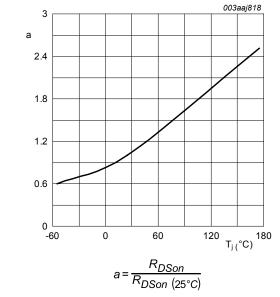


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, **FET1 and FET2**

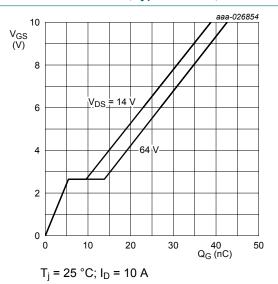


Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2

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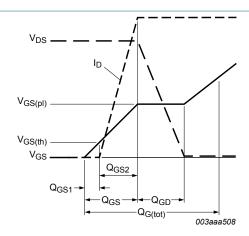
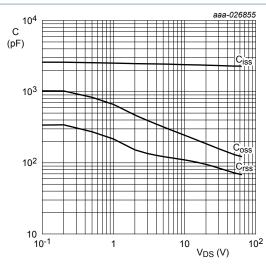
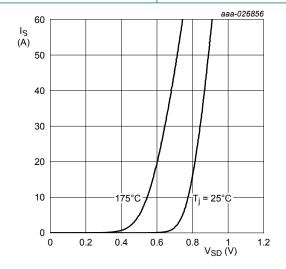


Fig. 14. Gate charge waveform definitions



 $V_{GS} = 0 V$; f = 1 MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2



 $V_{GS} = 0 V$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

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11. Package outline

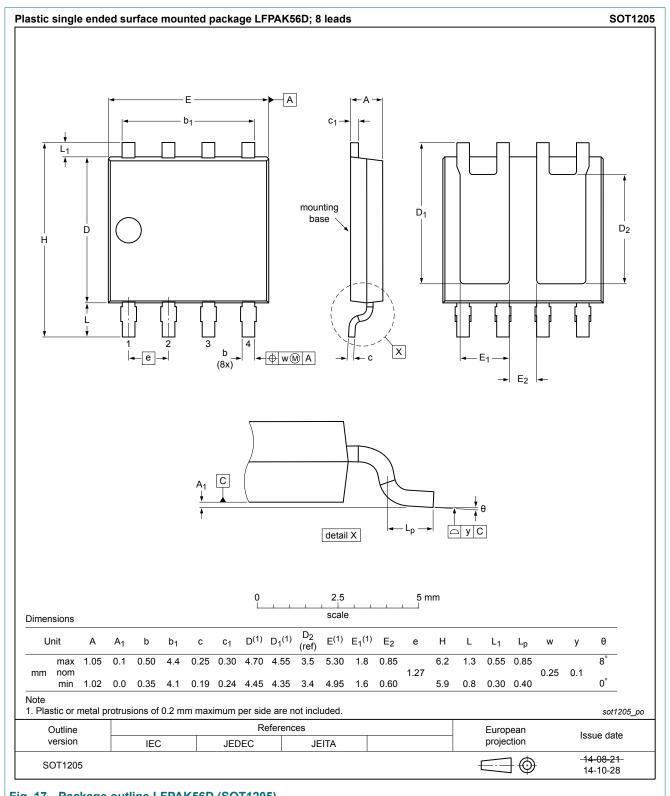


Fig. 17. Package outline LFPAK56D (SOT1205)

Dual N-channel 80 V, 22 mΩ logic level MOSFET

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|--------------------------------|--------------------|---|
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Dual N-channel 80 V, 22 m Ω logic level MOSFET

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