

Data Sheet April 4, 2013 FN6230.3

High-Speed 18V CMOS Comparators

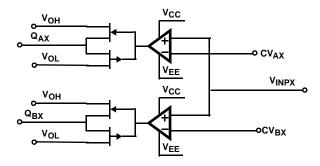
ISL55141, ISL55142, ISL55143 integrated circuits are high-speed, wide input common-mode range comparators. They provide three-state window comparators in a high voltage CMOS process (18V). Each comparator has dual receive thresholds, CV_{A} and CV_{B} , for establishing minimum 1-V $_{\text{IH}}$ and maximum 0-V $_{\text{IL}}$ voltage levels. These devices can accept inputs from a number of logic families, such as TTL, ECL, CMOS, LVCMOS, LVDS and CML. Two bits of output per comparator provide the test controller with qualification of a comparator input into three states. The two output bits work with a separate user supply to establish V_{OH} , V_{OL} levels compatibility with the system's controller logic levels.

Fast propagation delay (9.5ns typical at ±50mV overdrive) makes this family compatible with high-speed digital test systems. The 18V range enables the comparator input to operate over a wide input range. Two references per input enable and three state digitalization of input with voltage swings of up to 13V common mode. The operating frequency of these devices is typically 65MHz.

High voltage CMOS process makes these devices ideal for large voltage swing applications, such as special test voltages levels associated with Flash devices or power supervision applications and may avoid the need for test bus isolation relay(s).

Functional Block Diagram

DUAL LEVEL COMPARATOR - RECEIVERS



Note: x denotes 1, 2 or 4 channels for ISL55141, ISL55142 and ISL55143, respectively

Features

- 18V I/O Range
- · 65MHz Operation
- 9.5ns Typical Propagation Delay
- · Programmable Input Thresholds
- User Defined Comparator OutputLlevels
- · Common-Mode Range Includes Negative Rails
- · Small Footprints in QFN Packages
- Power-Down Current <10µA
- Pb-Free (RoHS compliant)

Applications

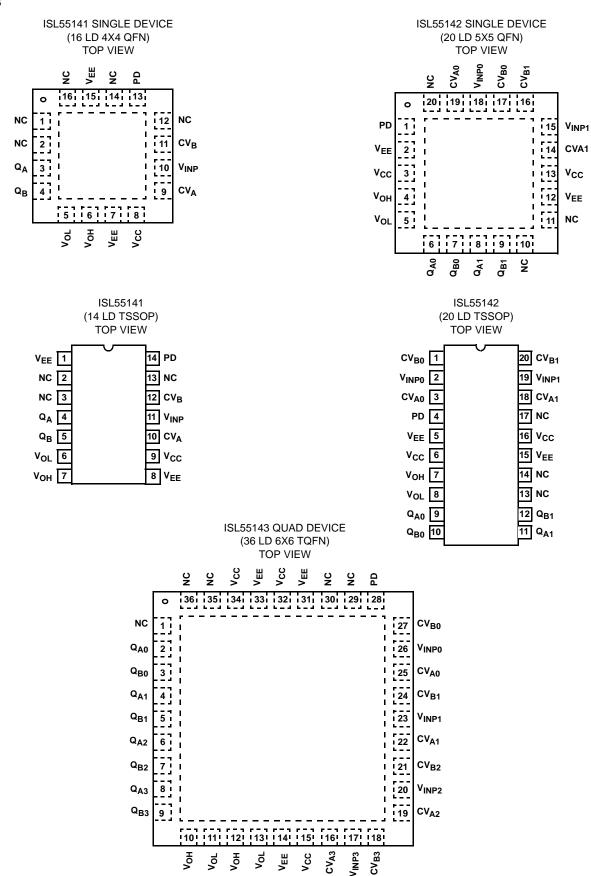
- · Burn in ATE
- Low Cost ATE
- · Fast Supervisory Power Control
- Instrumentation

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG.#
ISL55141IRZ	55 141IRZ	-40 to +85	16 Ld QFN	L16.4X4A
ISL55141IVZ	55141 IVZ	-40 to +85	14 Ld TSSOP	M14.173
ISL55142IRZ	55142 IRZ	-40 to +85	20 Ld QFN	L20.5x5
ISL55142IVZ	55142 IVZ	-40 to +85	20 Ld TSSOP	M20.173
ISL55143IRZ	55143 IRZ	-40 to +85	36 Ld TQFN	L36.6X6

- Add "-T*" suffix for tape and reel. Please refer to <u>TB347</u> for details on reel specifications.
- 2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- For Moisture Sensitivity Level (MSL), please see device information page for <u>ISL55141</u>, <u>ISL55142</u>, <u>ISL55143</u>. For more information on MSL please see techbrief TB363.

Pinouts



Pin Descriptions

PIN	FUNCTION
V _{EE}	Negative supply input
Q_{AX}	Channel A, CV _{AX} reference driven. Comparator output.
Q _{BX}	Channel B, CV _{BX} reference driven. Comparator output.
V _{OL}	Comparator output logic low supply. Unbuffered analog input that sets all Q _{AX} , Q _{BX} "low" voltage level.
V _{OH}	Comparator output logic high supply. Unbuffered analog input that sets all Q _{AX} , Q _{BX} "high" voltage level.
VCC	Positive supply input.
CV _{AX}	Channel A comparator reference analog input.
V _{INPX}	Window comparator input. Common to both Channel Ax and Channel Bx.
CV _{BX}	Channel B comparator reference analog input.
PD	Power-down logic input (connect to V _{EE} if not used for power-down).
NC	No internal connection.

TABLE 1. $\text{CV}_{A}\text{-}\text{Q}_{A}$ AND $\text{CV}_{B}\text{-}\text{Q}_{B}$ BASIC COMPARATOR TRUTH TABLE

INF	PUT	OUTPUTS*			
VIN	V _{INPX}		Q _{BX}		
<cv<sub>AX</cv<sub>	<cv<sub>BX</cv<sub>	0	0		
<cv<sub>AX</cv<sub>	>CV _{BX}	0	1		
>CV _{AX}	<cv<sub>BX</cv<sub>	1	0		
>CV _{AX}	>CV _{BX}	1	1		
* When $Q_{AX}/Q_{BX} = 1$, Output is connect to V_{OH}					
* Whe	n $Q_{AX}/Q_{BX} = 0$, C	Output is connect	to V _{OL}		

3 intersil FN6230.3 April 4, 2013

Absolute Maximum Ratings

V _{CC} to V _{EE}	0.5V to 19V
Input Voltages	
PD, CV _{AX} , CV _{BX} , V _{INPX} , V _{OH} , V _{OL}	
	$(V_{EE} - 0.5V)$ to $(V_{CC} + 0.5V)$
Output Voltage	
Q _A y, Q _B y	$(V_{OL} - 0.5V)$ to $(V_{OH} + 0.5V)$

Thermal Information

Thermal Resistance (Typical, Note 8)	θ _{JA} (°C/W)	θ _{JC} (°C/W)
16 Ld QFN Package (Notes 6, 7)	40	3
14 Ld TSSOP Package (Notes 4, 5)	100	31
20 Ld QFN Package (Notes 6, 7)	31	1.4
20 Ld TSSOP Package (Notes 4, 5)	76	25
36 Ld TQFN Package (Notes 6, 7)	29	0.75
Maximum Junction Temperature (Plastic F	Plackage)	150°
Maximum Storage Temperature Range	6	5°C to 150°C
Pb-Free Reflow Profile		ee link below
http://www.intersil.com/pbfree/Pb-FreeF	Reflow.asp	

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- 4. θJA is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- 5. For θ_{JC} , the "case temp" location is taken at the package top center.
- 6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- 7. For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.
- 8. Device temperature is closely tied to data-rates, driver loads and overall pin activity. Review "Power Dissipation Considerations" on page 6 for more information.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Device Power	V _{CC} -V _{EE}	10	15	18	V
Comparator Output High Rail	V _{OH}	V _{EE} +1		V _{CC} -0.5	V
Comparator Output Low Rail	V _{OL}	V _{EE} +0.5		V _{EE} +6	V
Common Mode Input Voltage Range	V _{CM}	V _{EE}		V _{CC} -5	V
Ambient Temperature	T _A	-40	27	+85	°C
Junction Temperature	TJ			+125	°C

Electrical Specifications

Test Conditions: V_{CC} = 12V, V_{EE} = -3V, V_{OH} = 5V, V_{OL} = 0V, PD = V_{EE} , C_{LOAD} = 15pF, T_A = 25°C, unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNITS
DC CHARACTERISTICS		1				
Input Offset Voltage	Vos	$CV_{AX} = CV_{BX} = 1.5V$	-50		50	mV
Input Bias Current	I _{BIAS}	V_{INPX} - $CV_{(A/B)X}$ = ±5V		10	25	nA
Power-down Current	I _{PD}	PD = V _{CC}		8	25	μA
Power-down Time (Note 11)	t _{PD}			10		μs
Power-up Time (Note 11)	t _{PU}			15		μs
TIMING CHARACTERISTICS					1	
Propagation Delay	t _{pd}		4.0	9.5	15	ns
Rise Time (Note 11)	t _r			1.4		ns
Fall Time (Note 11)	t _f			1.5		ns
Propagation Delay Mismatch	Δt_{pd}			0.5	2	ns
Maximum Operating Frequency	F _{MAXR}	Symmetry 50%		65		MHz
Min Pulse Width	twidr			7.7		ns
COMPARATOR INPUT	<u> </u>		, ,		1	
Input Current	I _{IN}	$V_{INPX} = V_{CC}$ or V_{EE}	-100	0	100	nA

4 intersil FN6230.3 April 4, 2013

Electrical Specifications

Test Conditions: $V_{CC} = 12V$, $V_{EE} = -3V$, $V_{OH} = 5V$, $V_{OL} = 0V$, $PD = V_{EE}$, $C_{LOAD} = 15pF$, $T_A = 25^{\circ}C$, unless otherwise specified. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNITS
Input Capacitance (Note 11)	C _{IN}			2.5		pF
DIGITAL OUTPUTS Q _{AX} , Q _{BX}						
Output Resistance	RoutR		18	27	37	Ω
Output Logic High Voltage	V _{OH}	V _{OH} = 5V, I _{SOURCE} = 1mA	4.9	4.95	5.0	V
Output Logic Low Voltage	V _{OL}	V _{OL} = 0V, I _{SINK} = 1mA	0.00	0.05	0.1	V
POWER SUPPLIES, STATIC CONDITION	NS					
Positive Supply DC Current/Comparator	Icc	No input data		+8.25	12.5	mA
Negative Supply Current/Comparator	I _{EE}	No input data	-12.5	-8.25		mA
Total Power Dissipation/Comparator	P (Note 12)	Input data at 40MHz		670		mW

NOTES:

- 9. Lab characterization, room temperature, timing parameters matched stimulus/loads, channel-to-channel skew < 500ps, 1ns maximum by design
- 10. Note about I_{CC} measurement input can approach 140mA (single comparator) at maximum pattern rates
- 11. Limits should be considered typical and are not production tested.
- 12. Total Power dissipation per comparator can be approximately calculated from the following:

 P = (V_{CC}-V_{EE})*8.25mW + 90pF*(V_{CC}-V_{EE})^2*f + C_L*(V_{CC}-V_{EE})^2*f, where f is the operating frequency and C_L is the load capacitance.

 Because the ISL55142 has two comparators, the power dissipation would be twice of P calculated from this equation. The ISL55143 would be four times P
- 13. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Test Circuits and Waveforms

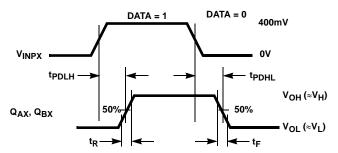
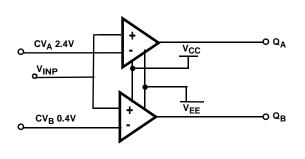


FIGURE 1. COMPARATOR PROPAGATION DELAY AND TRANSITION TIME MEASUREMENT POINTS



Although there is no electrical difference between the CV_A and CV_B Inputs, if one defines CV_A as being the high threshold and CV_B being the low threshold, it becomes easier to understand the utilization of a dual threshold comparator. Essentially this enables the qualification of an incoming signal into three states. In Figure 2, the three states are Valid Low <0.4V, No-man's-land (between 0.4 and 2.4V), Valid High >2.4V. Table 2 shows how the Q_A/Q_B truth table would be utilized in the real world.

TABLE 2. Q_A/Q_B TRUTH TABLE

V _{INP}	Q_{A}	Q _B	COMMENT
<0.4V	0	0	Valid 0
>0.4 and <2.4V	0	1	Invalid
>2.4V	1	1	Valid 1

FIGURE 2. THREE-STATE WINDOW COMPARATOR FUNDAMENTALS

intersil FN6230.3 April 4, 2013

 $CV_A = CV_B = 1.5V$

Test Circuits and Waveforms (Continued)

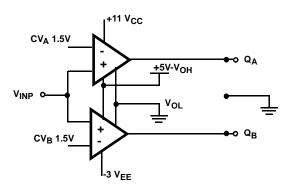


FIGURE 3. tpD RECEIVER SWITCHING TEST CIRCUIT

Application Information

The ISL55141, ISL55142, ISL55143 provide 1, 2 and 4 dual threshold, three-state window comparator(s) in TSSOP or QFN footprints. They offer a combination of speed (10ns Tpd and wide voltage range (18V). This product directly addresses the need for unique common-mode characteristics while supplying a power-down feature.

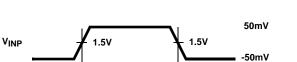
Figures 3 and 4 show the stimulus setup and measurement points for an example propagation delay measurement. Typical room temperature results are displayed in Figure 11.

Figure 4 shows a V_{INP} range of 50mV. In Figure 11 the offset is increased in the horizontal axis from 50mV above and below the reference (1.5V) up to 2.5V above and below the 1.5V reference.

Two lines are displayed in Figure 11. One represents the rising-to-rising delay (tpDLH) and the other the falling-to-falling delay (tPDHL).

Comparator Features

These three-state window comparators feature high output current capability, and user defined high and low output levels to interface with a wide variety of logic families. Each receiver comprises two comparators and each comparator has an independent threshold level input, making it easy to implement (Minimum1- V_{IH})/(Maximum 0- V_{IL}) logic level comparator functions. The CV_{AX} and CV_{BX} pins set the threshold levels of the A and B comparators respectively. VOH and V_{OL} set all the comparator output levels, and V_{OH} must be more positive than V_{OL}. These two inputs are unbuffered supply pins, so the sources driving these pins must provide adequate current for the expected load. VOH and VOL typically connect to the power supplies of the logic device driven by the comparator outputs.



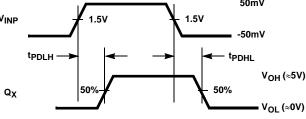


FIGURE 4. tpD RECEIVER PROPAGATION DELAY **MEASUREMENT POINTS**

The truth table for the receivers is given in Table 1. Receiver outputs are not tri-statable, and do not incorporate any on-chip short circuit current protection. Momentary short circuits to GND, or any supply voltage, will not cause permanent damage, but care must be taken to avoid longer duration short circuits. If tolerable to the application, current limiting resistors can be inserted in series with the QAX and QBX outputs to protect the receiver outputs from damage due to overcurrent conditions.

Power-down Features

The ISL55141, ISL55142, ISL55143 PD pin provides a means of reducing current consumption when the device is not in use. Supply currents fall from ~7mA to less than 10µA in the power-down mode. The device requires approximately 10μs to power-down and 15μs to power-up.

Power Supply Bypassing and Printed Circuit **Board Layout**

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible, and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the VFF pin is connected to ground, one 0.1µF ceramic capacitor should be placed from the V_{CC} pin to ground. A 4.7µF tantalum capacitor should then be connected from the V_{CC} pin to ground. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

Power Dissipation Considerations

Specifying continuous data rates, driver loads and driver level amplitudes are key in determining power supply requirements as well as dissipation/cooling necessities. Driver output patterns also impact these needs. The faster the pin activity, the greater the need to supply current and remove heat.

intersil FN6230.3 April 4, 2013 The maximum power dissipation allowed in a package is determined according to Equation 1.

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$
 (EQ. 1)

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

Approximate Power Dissipation

(Typ) $P = N^*[(V_{CC}-V_{EE})^*8.25mW + 90pF^*(V_{CC}-V_{EE})^*2^*f + CL^*(V_{OH}-V_{OL})^*2^*f]$

where:

N is the number of comparators in the chip (1 for ISL55141, 2 for ISL55142 and 4 for ISL55143). (f) is the operating frequency. CL is the load capacitor.

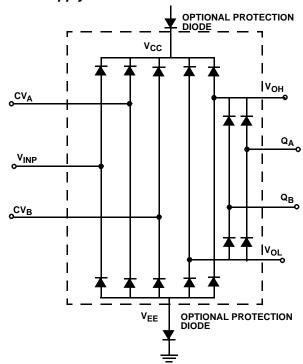
The power dissipation calculated from the above formula may have an error of ±20 to 25%.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads. Power also depends on the number of channels changing state and frequency of operation. The extent of continuous active pattern generation/reception will greatly affect dissipation requirements.

The user should evaluate various heat sink/cooling options in order to control the ambient temperature part of the equation. This is especially true if the user's applications require continuous, high-speed operation.

Note: The reader is cautioned against assuming the same level of thermal performance in actual applications. A careful inspection of conditions in your application should be conducted.

Power Supply Information



Circuit design must always take into account the internal EOS/ESD protection structure of the device.

Important Note: The QFN package metal plane is used for heat sinking of the device. It is electrically connected to the negative supply potential (VEE). If VEE is tied to ground, the thermal pad can be connected to ground. Otherwise, the thermal pad (VEE) must be isolated from other power planes.

Power Supply Sequencing

The ISL55141, ISL55142, ISL55143 reference every supply with respect to V_{EE} . Therefore, apply V_{EE} , V_{OL} then V_{CC} followed by the CV_A and CV_B supplies. The comparator V_{INP} pin should not exceed V_{FE} or V_{CC} during power-up.

In cases where inputs may exceed voltage rails during power-up, series resistance should be employed to safeguard EOS to the ESD protection diodes.

Typical Performance Curves Device installed on Intersil ISL55141, ISL55142, ISL55143 Evaluation Boards.

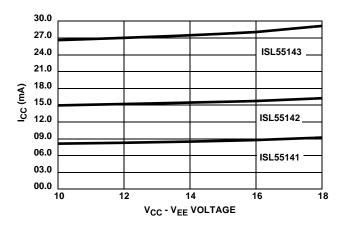


FIGURE 5. ISL55141, ISL55142, ISL55143 QUIESCENT **CURRENT**

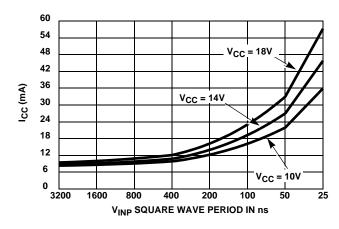


FIGURE 6. ISL55141 I_{CC} vs FREQUENCY @ 10V, 14V, AND

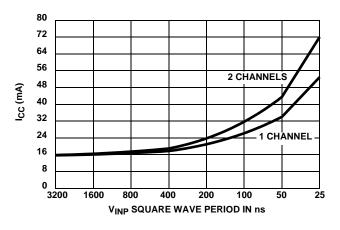


FIGURE 7. ISL55142 I_{CC} 1 AND 2 CHANNELS ACTIVE

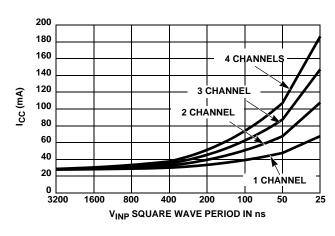


FIGURE 8. ISL55143 I_{CC} 1, 2, 3, 4 CHANNELS ACTIVE

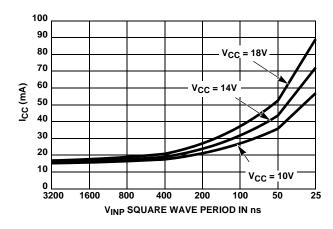


FIGURE 9. ISL55142 2-CHANNEL I_{CC} @ 10V, 14V, AND 18V

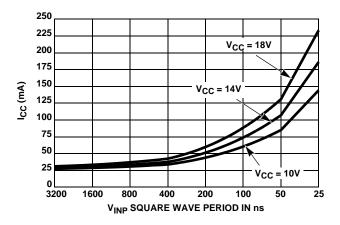


FIGURE 10. ISL55143 4-CHANNEL I_{CC} @ 10V, 14V, AND 18V

FN6230.3 April 4, 2013

intersil

Typical Performance Curves Device installed on Intersil ISL55141, ISL55142, ISL55143 Evaluation Boards. (Continued)

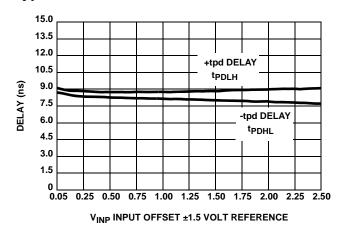


FIGURE 11. PROPAGATION DELAY @ 14V V_{CC}-V_{EE}

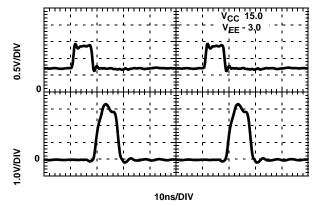


FIGURE 12. MINIMUM PULSE WIDTH RESPONSE

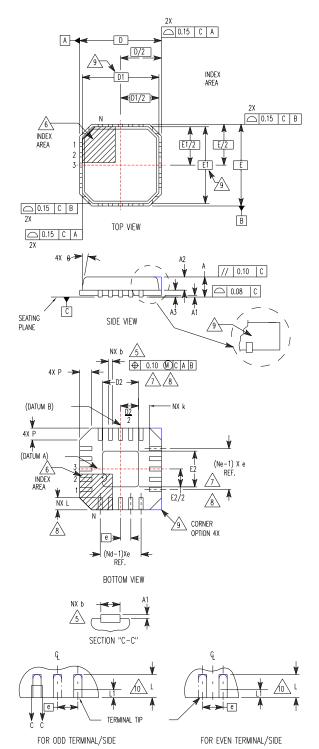
All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

intersil

Quad Flat No-Lead Plastic Package (QFN) Micro Lead Frame Plastic Package (MLFP)



L16.4x4A

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
(COMPLIANT TO JEDEC MO-220-VGGD-10)

	MILLIMETERS				
SYMBOL	MIN	NOMINAL	MAX	NOTES	
А	0.80	0.90	1.00	-	
A1	-	-	0.05	-	
A2	-	-	1.00	9	
A3		0.20 REF		9	
b	0.18	0.25	0.30	5, 8	
D		4.00 BSC		-	
D1		3.75 BSC		9	
D2	2.30	2.40	2.55	7, 8	
E		4.00 BSC			
E1		3.75 BSC		9	
E2	2.30	2.40	2.55	7, 8	
е		0.50 BSC		-	
k	0.25	-	-	-	
L	0.30	0.40	0.50	8	
L1	-	-	0.15	10	
N	16			2	
Nd		3			
Ne	4			3	
Р	-	0.60		9	
θ	-	-	12	9	

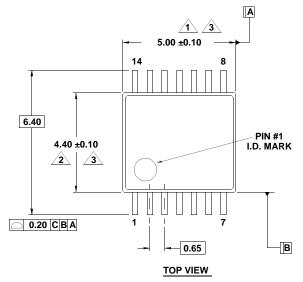
Rev. 2 3/06

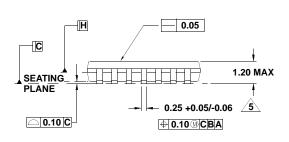
- 1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
- 2. N is the number of terminals.
- 3. Nd and Ne refer to the number of terminals on each D and E.
- 4. All dimensions are in millimeters. Angles are in degrees.
- 5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
- 6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
- Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
- 8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
- 9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
- Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present.
 L minus L1 to be equal to or greater than 0.3mm.

Package Outline Drawing

M14.173

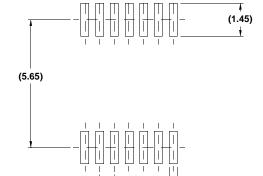
14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP) Rev 3, 10/09



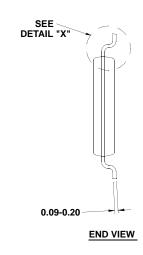


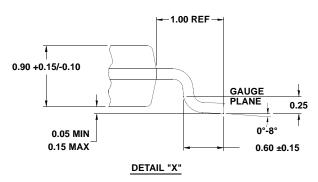
SIDE VIEW

1 1 1



TYPICAL RECOMMENDED LAND PATTERN





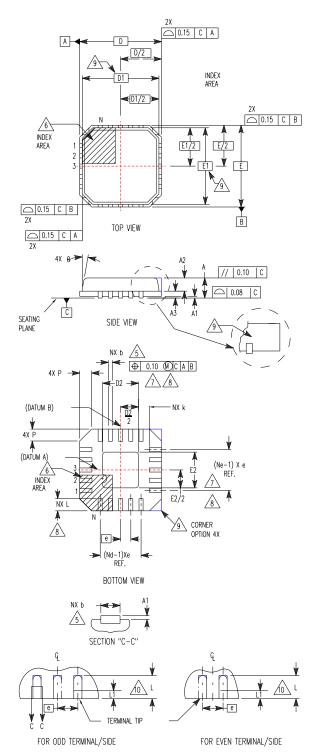
NOTES:

(0.35 TYP)

- Dimension does not include mold flash, protrusions or gate burrs.
 Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
- Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
- 3. Dimensions are measured at datum plane H.
- 4. Dimensioning and tolerancing per ASME Y14.5M-1994.
- Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
- 6. Dimension in () are for reference only.
- 7. Conforms to JEDEC MO-153, variation AB-1.

(0.65 TYP)

Quad Flat No-Lead Plastic Package (QFN) Micro Lead Frame Plastic Package (MLFP)



L20.5x5
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MIN	NOMINAL	MAX	NOTES		
А	0.80	0.90	1.00	-		
A1	-	0.02	0.05	-		
A2	-	0.65	1.00	9		
A3		0.20 REF		9		
b	0.23	0.30	0.38	5, 8		
D		5.00 BSC		-		
D1		4.75 BSC				
D2	2.95	3.10	3.25	7, 8		
E		5.00 BSC				
E1		4.75 BSC		9		
E2	2.95	3.10	3.25	7, 8		
е		0.65 BSC		-		
k	0.20	-	-	-		
L	0.35	0.60	0.75	8		
N		2				
Nd		5				
Ne		5				
Р	-	0.60				
θ	-	-	12	9		

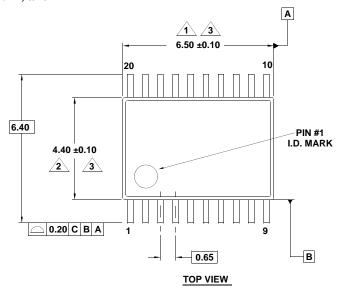
Rev. 4 11/04

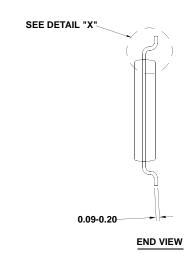
- 1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
- 2. N is the number of terminals.
- 3. Nd and Ne refer to the number of terminals on each D and E.
- 4. All dimensions are in millimeters. Angles are in degrees.
- 5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
- The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
- 7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
- 8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
- Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
- Compliant to JEDEC MO-220VHHC Issue I except for the "b" dimension.

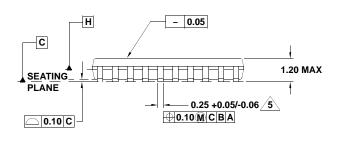
Package Outline Drawing

M20.173

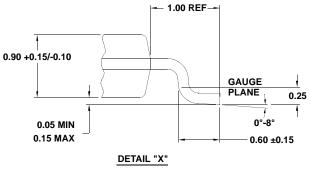
20 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP) Rev 2, 5/10

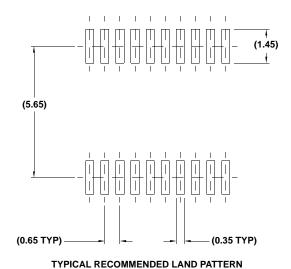






SIDE VIEW



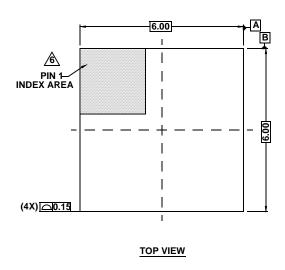


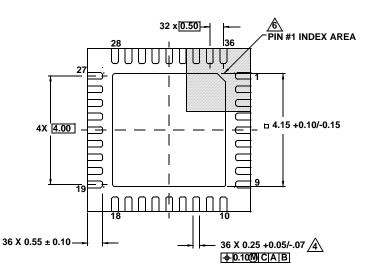
- 1. Dimension does not include mold flash, protrusions or gate burrs.

 Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
- <u>2.</u> Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
- 3. Dimensions are measured at datum plane H.
- 4. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
- 6. Dimension in () are for reference only.
- 7. Conforms to JEDEC MO-153.

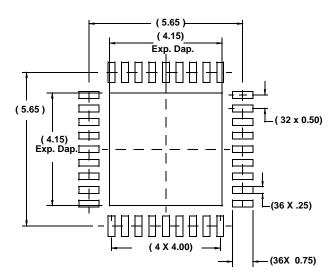
Package Outline Drawing

L36.6x6 36 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE Rev 5, 08/08

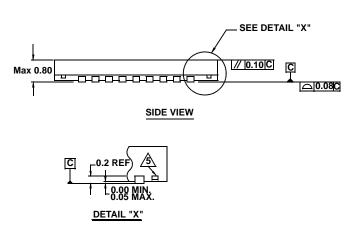




BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



- 1. Dimensions are in millimeters.
- 2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
- 3. Unless otherwise specified, tolerance : Decimal ± 0.05
- 4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
- 5. Tiebar shown (if present) is a non-functional feature.
- The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

intersil* FN6230.3 April 4, 2013

ПОСТАВКА ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru_6 moschip.ru_4 moschip.ru_9