

EOS and ESD Transil™ protection for charger and battery port

Features

- Breakdown voltage: 12 V, 18 V
- Unidirectional device
- High peak power dissipation: 450 W (8/20 μ s waveform)
- ESD protection level better than IEC 61000-4-2 level 4: 30 kV contact discharge.
- Low leakage current < 0.5 μ A at 5 V
- PCB area: 1.3 mm²

Benefits

- High EOS and ESD protection level
- High integration
- Suitable for high density board
- Small package

Complies with the following standards

- IEC 61000-4-2 level 4
 - 15 kV (air discharge)
 - 8 kV (contact discharge)
- MIL STD 883G - Method 3015-7 Class 3B
 - HBM (Human Body Model): \geq 8 kV

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

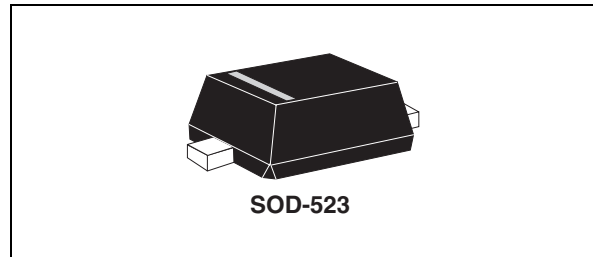
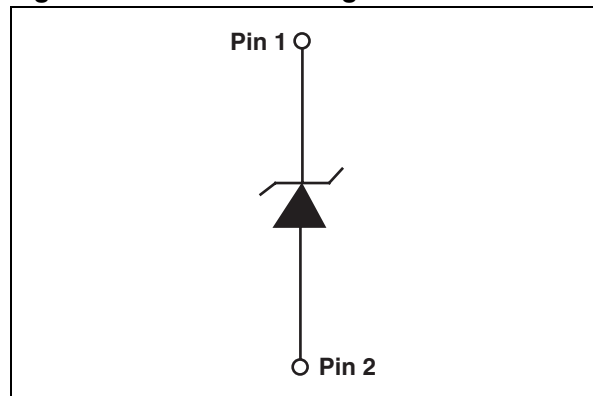


Figure 1. Functional diagram



Description

The ESDA-1K is a single line Transil diode designed specifically for the protection of integrated circuits in portable equipment and miniaturized electronics devices subject to ESD and EOS transient overvoltages.

TM: Transil is a trademark of STMicroelectronics.

1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 air discharge	30	kV
		IEC 61000-4-2 contact discharge	30	
T_j	Operating Junction temperature rage		-40 to +150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		-65 to +150	$^{\circ}\text{C}$
T_L	Maximum lead temperature for soldering during 10 s		260	$^{\circ}\text{C}$

Table 2. Absolute maximum ratings ($t_{amb} = 25\text{ }^{\circ}\text{C}$) - product specific parameters

Order code	I_{PP} (A) peak pulse current (8/20 μs)	P_{PP} (W) peak pulse power (8/20 μs)
ESDA12-1K	16	450
ESDA18-1K	12	400

Figure 2. Electrical characteristics (definitions)

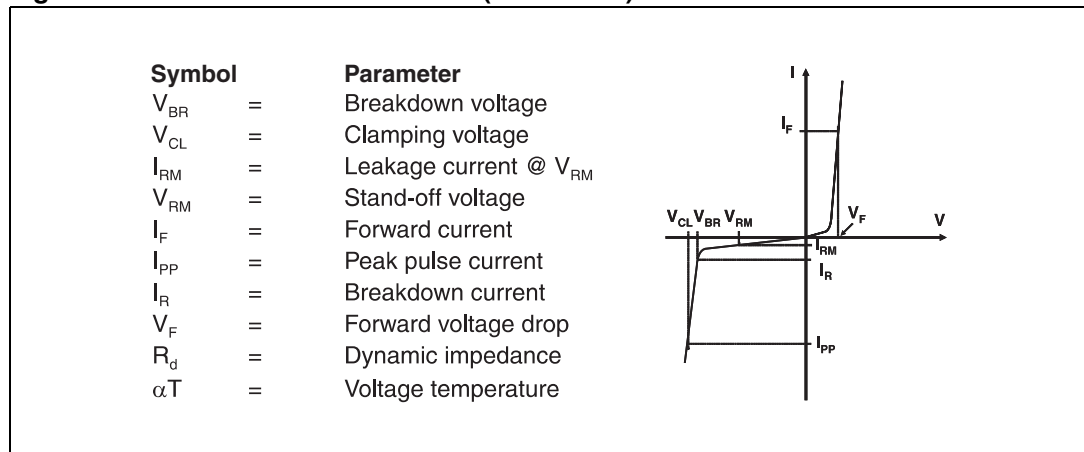


Table 3. Electrical characteristics (values, $T_{amb} = 25\text{ }^{\circ}\text{C}$)

Order code	$V_{BR} @ I_R$			$I_{RM} @ V_{RM}$		$V_{CL} @ I_{PP} (8/20\text{ }\mu\text{s})$				$C_{line}^{(1)}$
	Min.	Typ.		Max.		Max.		Max.		Max.
	V	V	mA	μA	V	V	A	V	A	pF
ESDA12-1K	12	13	1	0.5	10	16.5	1	28	16	150
ESDA18-1K	18	19	1	0.5	15	24	1	34	12	105

1. $V_R = 0\text{ V}$, $F_{osc} = 1\text{ MHz}$, $V_{osc} = 30\text{ mV}$

Figure 3. Peak pulse power dissipation versus exponential pulse duration (typical values)

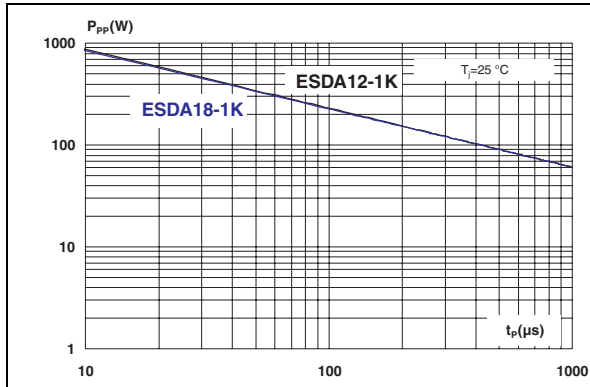


Figure 4. Peak pulse power dissipation versus initial junction temperature (typical values)

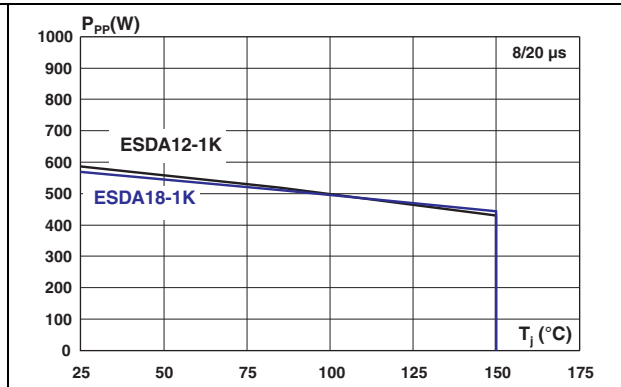


Figure 5. Clamping voltage versus peak pulse current (typical values)

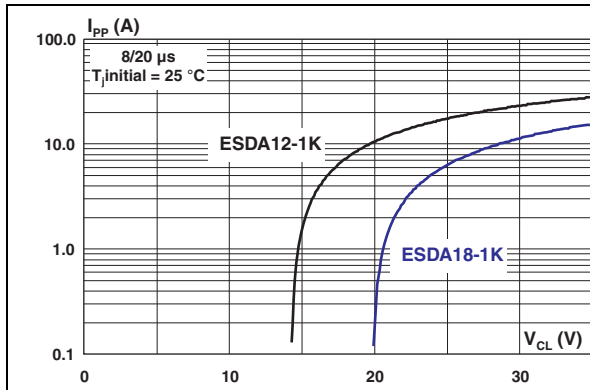


Figure 6. Leakage current versus junction temperature (typical values)

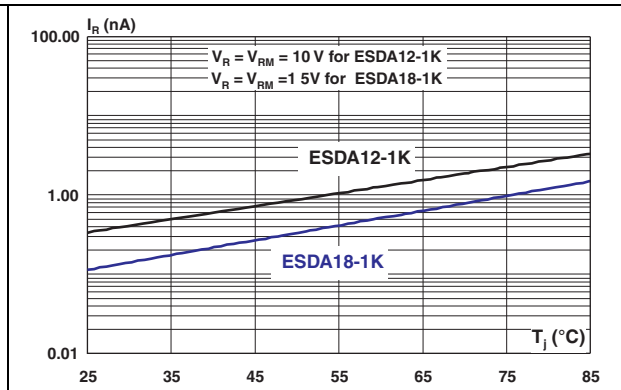


Figure 7. ESD response to IEC 61000-4-2 (+15 kV air discharge) ESDA12-1K

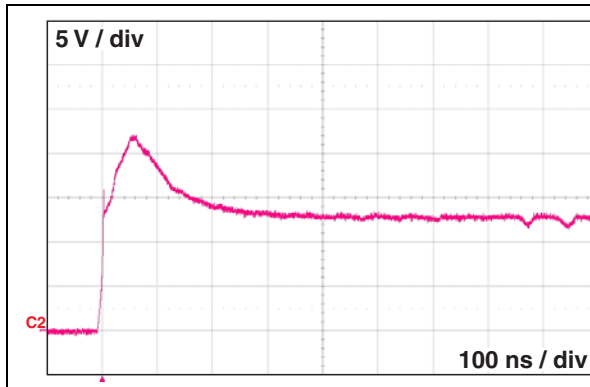
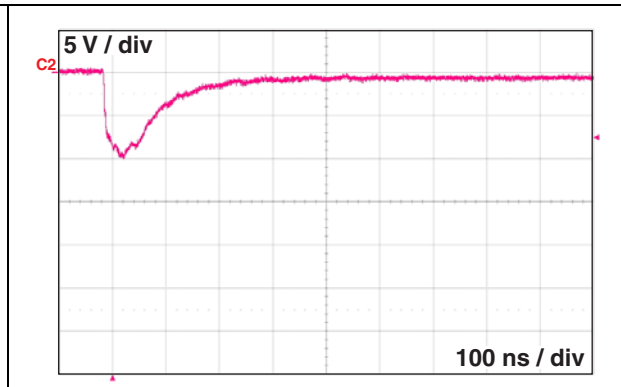
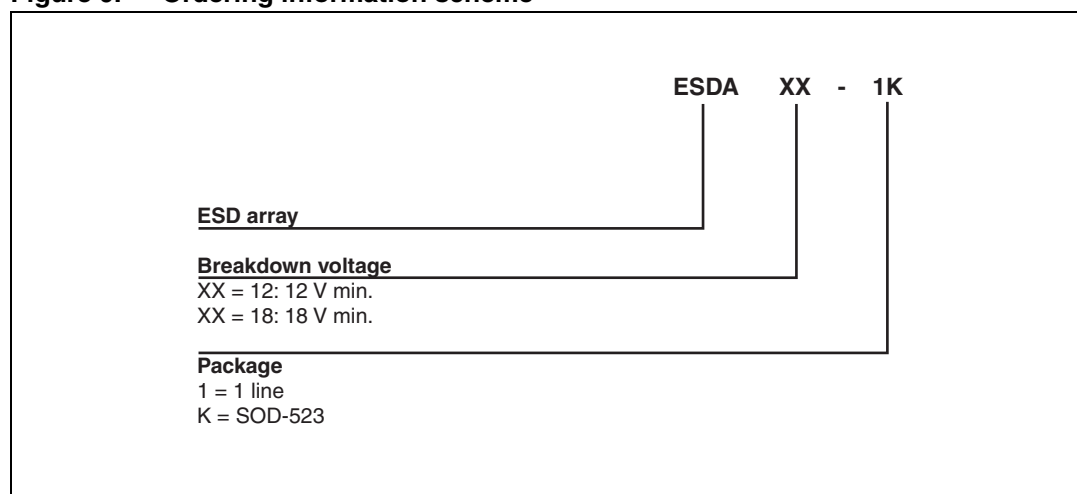


Figure 8. ESD response to IEC 61000-4-2 (-15 kV air discharge) ESDA12-1K



2 Ordering information scheme

Figure 9. Ordering information scheme



3 Package information

- Epoxy meets UL94,V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 4. SOD-523 dimensions

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.60	0.70	0.020	0.024	0.028
E	1.50	1.60	1.70	0.059	0.063	0.067
E1	1.10	1.20	1.30	0.043	0.047	0.051
D	0.70	0.80	0.90	0.028	0.031	0.035
b	0.25		0.35	0.010		0.014
c	0.07		0.20	0.003		0.008
L	0.15	0.20	0.25	0.006	0.008	0.010
L1	0.05		0.20	0.002		0.008

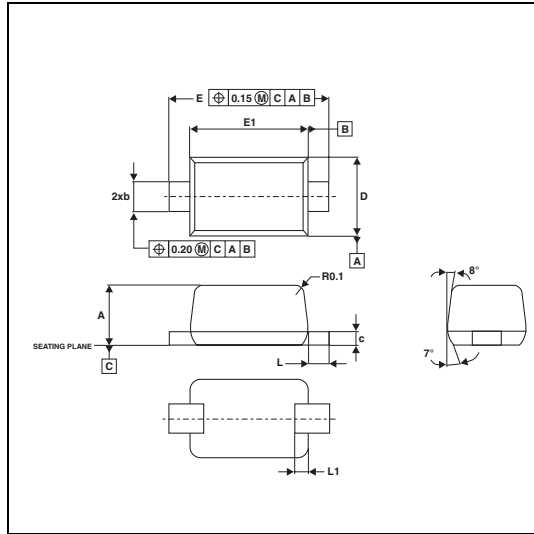


Figure 10. Footprint (dimensions in mm)

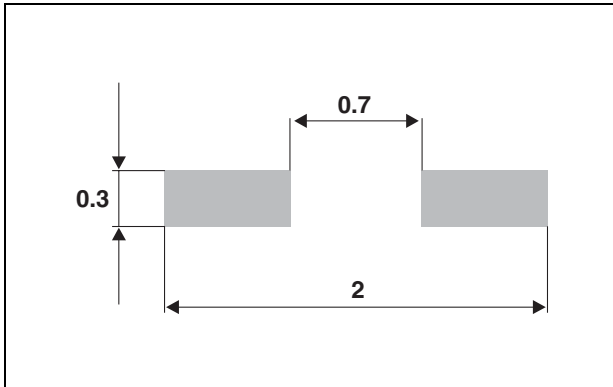
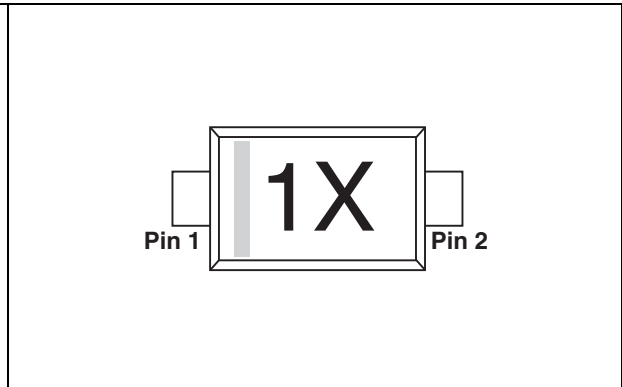
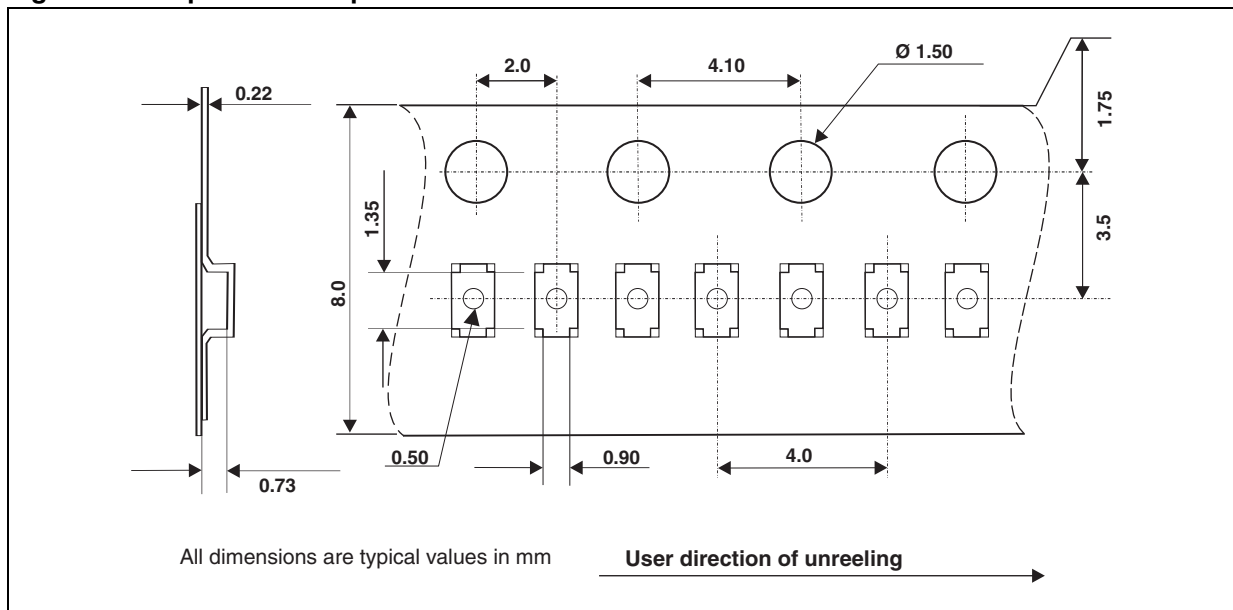


Figure 11. Marking



Note: Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 12. Tape and reel specification



4 Recommendation on PCB assembly

4.1 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 μm .

4.2 Placement

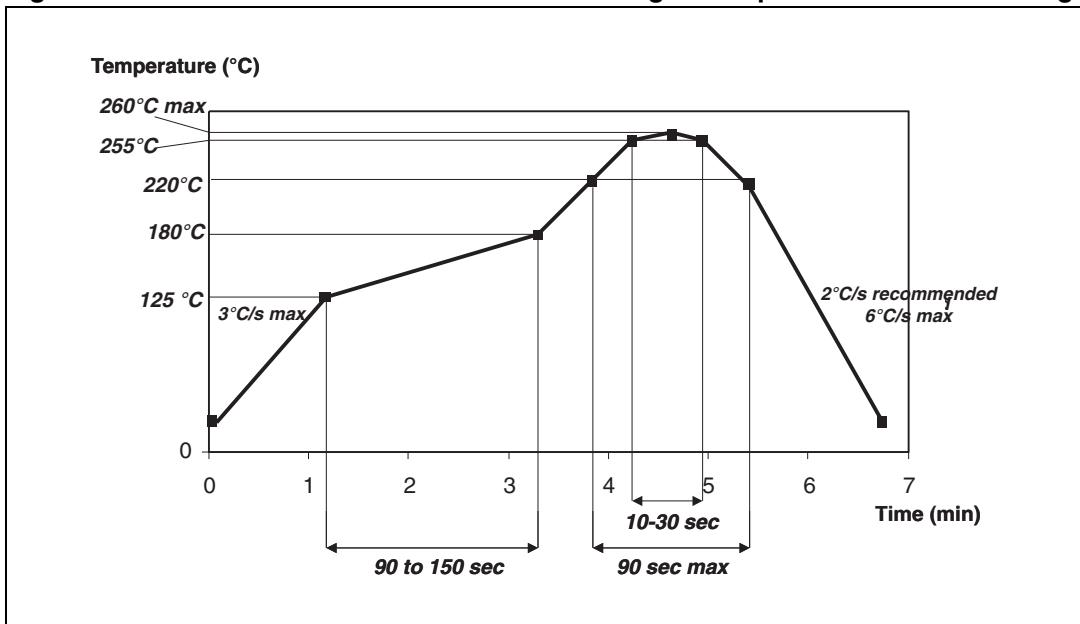
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.3 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.4 Reflow profile

Figure 13. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDA12-1K	12	SOD-523	1.46	3000	Tape and reel
ESDA18-1K	18				

Note: The marking can be rotated by multiples of 90° to differentiate assembly location.

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
02-Sep-2010	1	First issue.

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