



# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

## General Description

The MAX16060/MAX16061/MAX16062 are 1% accurate, quad-/hex-/octal-voltage µP supervisors in a small thin QFN package. These devices provide supervisory functions for complex multivoltage systems. The MAX16060 monitors four voltages, the MAX16061 monitors six voltages, and the MAX16062 monitors eight voltages.

These devices offer independent outputs for each monitored voltage along with a reset output that asserts whenever any of the monitored voltages fall below their respective thresholds (down to 0.4V) or the manual reset input is asserted. The reset output remains asserted for the reset timeout after all voltages are above their respective thresholds and the manual reset input is deasserted. The minimum reset timeout is internally set to 140ms or can be adjusted with an external capacitor.

All open-drain outputs have internal 30µA pullups that eliminate the need for external pullup resistors. However, each output can be driven with an external voltage up to 5.5V. Other features offered include a manual reset input, a tolerance pin for selecting 5% or 10% input thresholds, and a margin enable function for deasserting the outputs during margin testing.

An additional feature is a watchdog timer that asserts RESET when the watchdog timeout period (1.6s typ) is exceeded. The watchdog timer can be disabled by leaving WDI unconnected.

These devices are offered in 16-, 20-, and 24-pin thin QFN packages (4mm x 4mm) and are fully specified from -40°C to +125°C.

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16060_TE+	-40°C to +125°C	16 TQFN-EP*
MAX16061_TP+	-40°C to +125°C	20 TQFN-EP*
MAX16062_TG+	-40°C to +125°C	24 TQFN-EP*

**Note:** The “\_” is a placeholder for the input voltage threshold. See Table 1. The MAX16060/MAX16061/MAX16062 are available in factory-preset thresholds/configuration combinations. Choose the desired combination and complete part number from Table 1.

\*Denotes a lead-free package.

For tape-and-reel, add a “T” after the “.” Tape-and-reel are offered in 2.5k increments.

\*EP = Exposed pad.

## Features

- ◆ Fixed Thresholds for 3.3V, 2.5V, and 1.8V Systems
- ◆ Adjustable Thresholds Monitor Low Voltages (Down to 0.4V)
- ◆ 1% Accurate over Temperature
- ◆ Open-Drain Outputs with Internal Pullups Reduce the Number of External Components
- ◆ Fixed 140ms (min) or Capacitor-Adjustable Reset Timeout
- ◆ Manual Reset, Margin Enable, and Tolerance Select Inputs
- ◆ Watchdog Timer
  - 1.6s (typ) Timeout Period
  - 54s Startup Delay After Reset
- ◆ Monitors Four (MAX16060), Six (MAX16061), or Eight (MAX16062) Voltages
- ◆ RESET Output Indicates All Voltages Present
- ◆ Independent Voltage Monitors
- ◆ Guaranteed to Remain Asserted Down to V<sub>CC</sub> = 1V
- ◆ Small (4mm x 4mm) Thin QFN Package

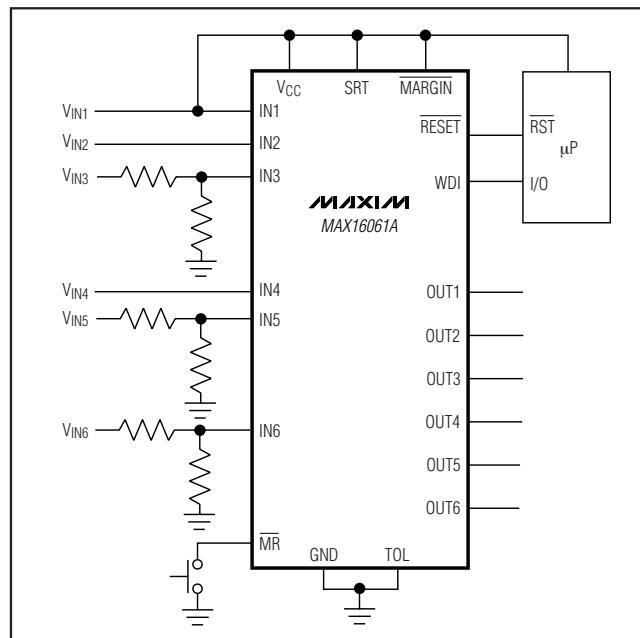
## Applications

Storage Equipment Multivoltage ASICs

Servers Automotive

Networking/Telecommunication Equipment

## Typical Operating Circuit



**MAX16060/MAX16061/MAX16062**

# 1% Accurate, Quad-/Hex-/Octal-Voltage μP Supervisors

## ABSOLUTE MAXIMUM RATINGS

V<sub>CC</sub>, OUT<sub>1</sub>, IN<sub>1</sub>, RESET to GND ..... -0.3V to +6V  
 TOL, MARGIN, MR, SRT, WDI to GND ..... -0.3V to V<sub>CC</sub> + 0.3  
 Input/Output Current (RESET, MARGIN,  
 SRT, MR, TOL, OUT<sub>1</sub>, WDI) ..... ±20mA  
 Continuous Power Dissipation (T<sub>A</sub> = +70°C)  
 16-Pin TQFN (derate 16.9mW/°C above +70°C) ..... 1349mW  
 20-Pin TQFN (derate 16.9mW/°C above +70°C) ..... 1355mW  
 24-Pin TQFN (derate 16.9mW/°C above +70°C) ..... 1666mW

Operating Temperature Range ..... -40°C to +125°C  
 Junction Temperature ..... +150°C  
 Storage Temperature Range ..... -65°C to +150°C  
 Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 2.0V to 5.5V, T<sub>A</sub> = -40°C to +125°C, unless otherwise specified. Typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V <sub>CC</sub>	(Note 2)	1.0	5.5		V
Supply Current (Note 3)	I <sub>CC</sub>	V <sub>CC</sub> = 3.3V, OUT <sub>1</sub> , RESET not asserted		45	65	μA
		V <sub>CC</sub> = 5V, OUT <sub>1</sub> , RESET not asserted		50	70	
UVLO (Undervoltage Lockout)	V <sub>UVLO</sub>	V <sub>CC</sub> rising	1.62	1.80	1.98	V
UVLO Hysteresis	V <sub>UVLO_HYS</sub>			65		mV
<b>IN_ (See Table 1)</b>						
Threshold Voltages (IN_ Falling)	V <sub>TH</sub>	3.3V threshold, TOL = GND	3.069	3.102	3.135	V
		3.3V threshold, TOL = V <sub>CC</sub>	2.904	2.937	2.970	
		2.5V threshold, TOL = GND	2.325	2.350	2.375	
		2.5V threshold, TOL = V <sub>CC</sub>	2.200	2.225	2.250	
		1.8V threshold, TOL = GND	1.674	1.692	1.710	
		1.8V threshold, TOL = V <sub>CC</sub>	1.584	1.602	1.620	
Adjustable Threshold (IN_ Falling)	V <sub>TH</sub>	TOL = GND	0.390	0.394	0.398	V
		TOL = V <sub>CC</sub>	0.369	0.373	0.377	
IN_ Hysteresis	V <sub>TH_HYS</sub>	IN_ rising		0.5		% V <sub>TH</sub>
IN_ Input Current		Fixed thresholds		3	16	μA
		Adjustable thresholds	-100		+100	nA

# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC}$  = 2.0V to 5.5V,  $T_A$  = -40°C to +125°C, unless otherwise specified. Typical values are at  $V_{CC}$  = 3.3V,  $T_A$  = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>RESET</b>						
Reset Timeout	tRP	SRT = $V_{CC}$	140	200	280	ms
		CSRT = 1500pF (Note 4)	2.43	3.09	3.92	
		CSRT = 100pF		0.206		
		CSRT = open		50		µs
SRT Ramp Current	ISRT	$V_{SRT}$ = 0V	460	600	740	nA
SRT Threshold			1.173	1.235	1.293	V
SRT Hysteresis				100		mV
IN_ to Reset Delay	trD	IN_ falling		20		µs
RESET Output-Voltage Low	VOL	$V_{CC}$ = 3.3V, $I_{SINK}$ = 10mA, RESET asserted		0.3		V
		$V_{CC}$ = 2.5V, $I_{SINK}$ = 6mA, RESET asserted		0.3		
		$V_{CC}$ = 1.2V, $I_{SINK}$ = 50µA, RESET asserted		0.3		
RESET Output-Voltage High	VOH	$V_{CC} \geq 2.0V$ , $I_{SOURCE}$ = 6µA, RESET deasserted	0.8 x $V_{CC}$			V
MR Input-Voltage Low	VI <sub>L</sub>			0.3 x $V_{CC}$		V
MR Input-Voltage High	VI <sub>H</sub>		0.7 x $V_{CC}$			V
MR Minimum Pulse Width			1			µs
MR Glitch Rejection				100		ns
MR to Reset Delay				200		ns
MR Pullup Resistance		Pulled up to $V_{CC}$	12	20	28	kΩ
<b>OUTPUTS (OUT_)</b>						
OUT_ Output-Voltage Low	VOL	$V_{CC}$ = 3.3V, $I_{SINK}$ = 2mA		0.3		V
		$V_{CC}$ = 2.5V, $I_{SINK}$ = 1.2mA		0.3		
OUT_ Output-Voltage High	VOH	$V_{CC} \geq 2.0V$ , $I_{SOURCE}$ = 6µA	0.8 x $V_{CC}$			V
IN_ to OUT_ Propagation Delay	tD	( $V_{TH}$ + 100mV) to ( $V_{TH}$ - 100mV)		20		µs

**MAX16060/MAX16061/MAX16062**

# 1% Accurate, Quad-/Hex-/Octal-Voltage μP Supervisors

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC}$  = 2.0V to 5.5V,  $T_A$  = -40°C to +125°C, unless otherwise specified. Typical values are at  $V_{CC}$  = 3.3V,  $T_A$  = +25°C). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>WATCHDOG TIMER</b>						
WDI Input-Voltage Low	$V_{IL}$			0.3 x $V_{CC}$		V
WDI Input-Voltage High	$V_{IH}$		0.7 x $V_{CC}$			V
WDI Pulse Width		(Note 5)	50			ns
Watchdog Timeout Period	$t_{WDI}$		1.12	1.60	2.40	s
Watchdog Startup Period			35	54	72	s
Watchdog Input Current		$V_{WDI}$ = 0 to $V_{CC}$ (Note 5)	-1		+1	μA
<b>DIGITAL LOGIC</b>						
TOL Input-Voltage Low	$V_{IL}$			0.3 x $V_{CC}$		V
TOL Input-Voltage High	$V_{IH}$		0.7 x $V_{CC}$			V
TOL Input Current		$TOL = V_{CC}$		100		nA
MARGIN Input-Voltage Low	$V_{IL}$			0.3 x $V_{CC}$		V
MARGIN Input-Voltage High	$V_{IH}$		0.7 x $V_{CC}$			V
MARGIN Pullup Resistance		Pulled up to $V_{CC}$	12	20	28	kΩ
MARGIN Delay Time	$t_{MD}$	Rising or falling (Note 6)		50		μs

**Note 1:** Devices are tested at  $T_A$  = +25°C and guaranteed by design for  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ .

**Note 2:** The outputs are guaranteed to remain asserted down to  $V_{CC}$  = 1V.

**Note 3:** Measured with WDI, MARGIN, and  $\overline{MR}$  unconnected.

**Note 4:** The minimum and maximum specifications for this parameter are guaranteed by using the worst case of the SRT ramp current and SRT threshold specifications.

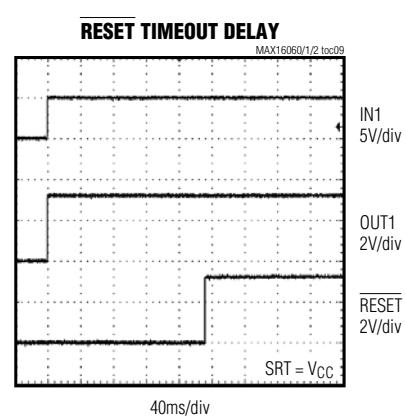
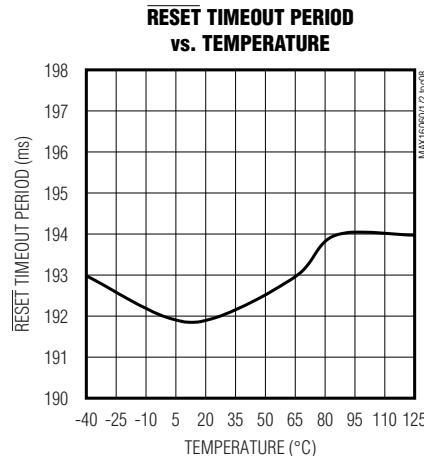
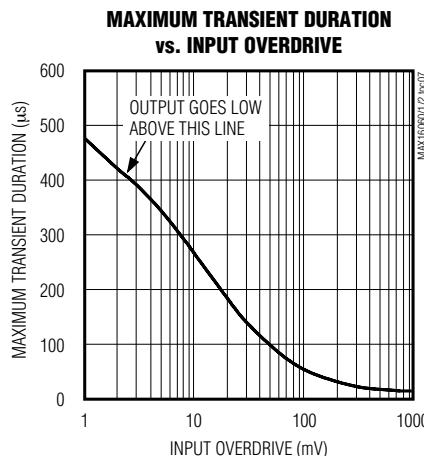
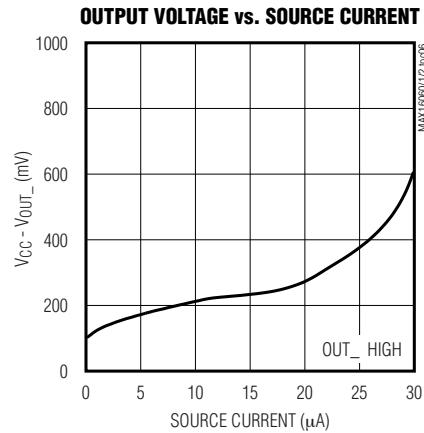
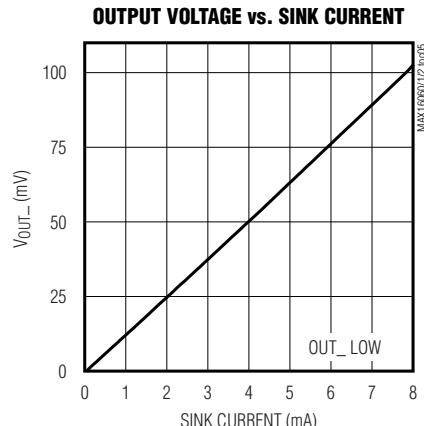
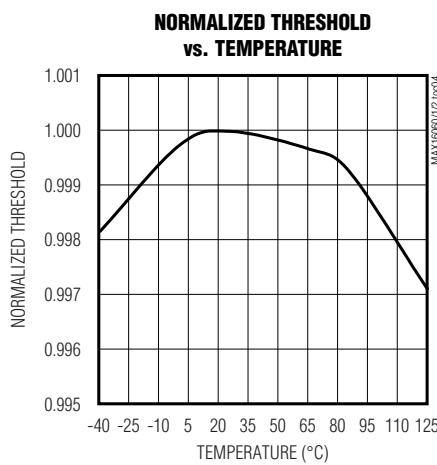
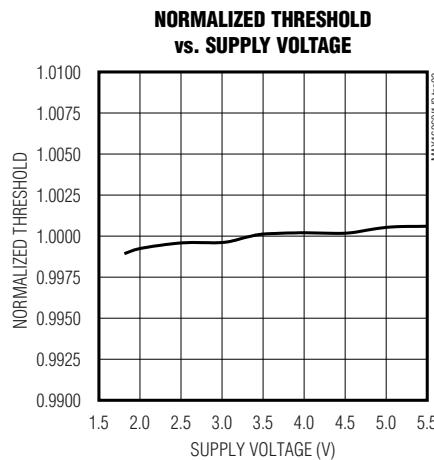
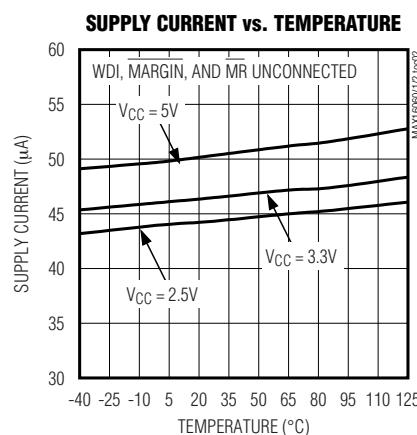
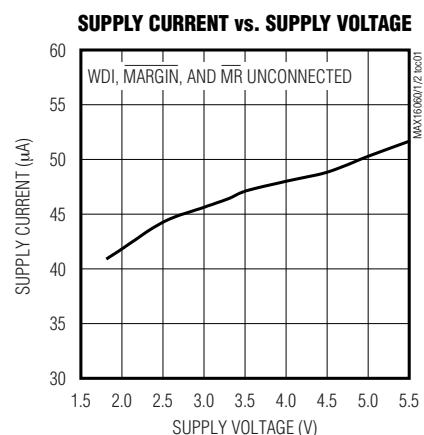
**Note 5:** Guaranteed by design and not production tested.

**Note 6:** Amount of time required for logic to lock/unlock outputs from margin testing.

# 1% Accurate, Quad-/Hex-/Octal-Voltage $\mu$ P Supervisors

## Typical Operating Characteristics

( $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

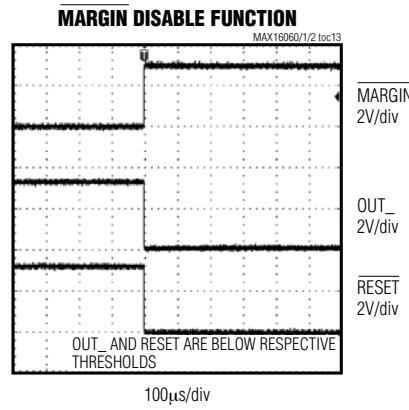
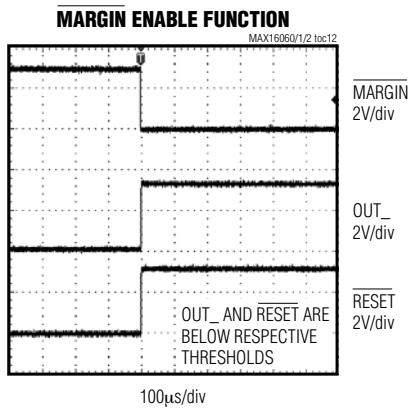
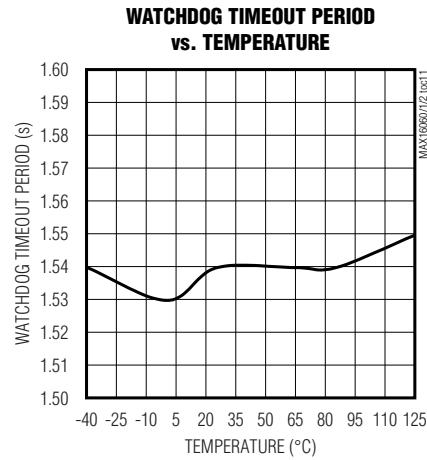
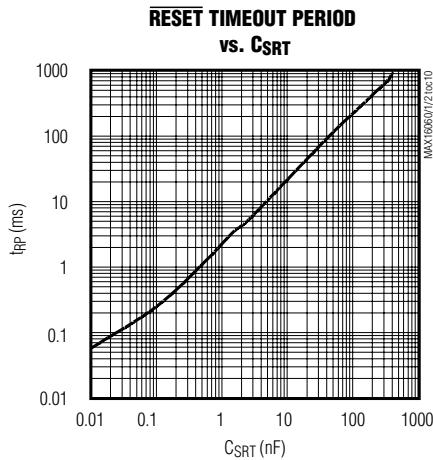


**MAX16060/MAX16061/MAX16062**

# 1% Accurate, Quad-/Hex-/Octal-Voltage μP Supervisors

## Typical Operating Characteristics (continued)

( $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

## Pin Description (MAX16060)

PIN	NAME	FUNCTION
1	IN3	Monitored Input Voltage 3. See Table 1 for the input voltage threshold.
2	IN4	Monitored Input Voltage 4. See Table 1 for the input voltage threshold.
3	WDI	Watchdog Timer Input. If WDI remains low or high for longer than the watchdog timeout period, <u>RESET</u> is asserted. The timer clears whenever a reset is asserted or a rising or falling edge on WDI is detected. The watchdog timer enters a startup period that allows 54s for the first transition to occur before a reset. Leave WDI unconnected to disable the watchdog timer. The WDI unconnected-state detector uses a small 400nA current. Therefore, do not connect WDI to anything that will source or sink more than 200nA. Note that the leakage current specification for most three-state drivers exceeds 200nA.
4	GND	Ground
5	Vcc	Unmonitored Power-Supply Input
6	OUT3	Output 3. When the voltage at IN3 falls below its threshold, OUT3 goes low and stays low until the voltage at IN3 exceeds its threshold. The open-drain output has a 30µA internal pullup to Vcc.
7	OUT4	Output 4. When the voltage at IN4 falls below its threshold, OUT4 goes low and stays low until the voltage at IN4 exceeds its threshold. The open-drain output has a 30µA internal pullup to Vcc.
8	<u>MR</u>	Active-Low Manual Reset Input. Pull <u>MR</u> low to assert <u>RESET</u> low. <u>RESET</u> remains low for the reset timeout period after <u>MR</u> is deasserted. <u>MR</u> is pulled up to Vcc through a 20kΩ resistor.
9	SRT	Set Reset Timeout Input. Connect a capacitor from SRT to GND to set the reset timeout period. The reset timeout period can be calculated as follows: Reset Timeout (s) = $2.06 \times 10^6 (\Omega) \times C_{SRT} (F)$ . For the internal timeout period of 140ms (min), connect SRT to Vcc.
10	<u>MARGIN</u>	Active-Low Manual Deassert Input. Pull <u>MARGIN</u> low to deassert all outputs (go into high state), regardless of the voltage at any monitored input.
11	OUT2	Output 2. When the voltage at IN2 falls below its threshold, OUT2 goes low and stays low until the voltage at IN2 exceeds its threshold. The open-drain output has a 30µA internal pullup to Vcc.
12	OUT1	Output 1. When the voltage at IN1 falls below its threshold, OUT1 goes low and stays low until the voltage at IN1 exceeds its threshold. The open-drain output has a 30µA internal pullup to Vcc.
13	<u>RESET</u>	Active-Low Reset Output. <u>RESET</u> asserts low when any of the monitored voltages falls below its respective threshold or <u>MR</u> is asserted. <u>RESET</u> remains asserted for the reset timeout period after all monitored voltages exceed their respective thresholds and <u>MR</u> is deasserted. This open-drain output has a 30µA internal pullup.
14	IN1	Monitored Input Voltage 1. See Table 1 for the input voltage threshold.
15	IN2	Monitored Input Voltage 2. See Table 1 for the input voltage threshold.
16	TOL	Threshold Tolerance Input. Connect TOL to GND to select 5% threshold tolerance. Connect TOL to Vcc to select 10% threshold tolerance.
—	EP	Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal resistance path from the IC junction to the PCB. Do not use as the electrical connection to GND.

**MAX16060/MAX16061/MAX16062**

# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

## Pin Description (MAX16061)

PIN	NAME	FUNCTION
1	IN4	Monitored Input Voltage 4. See Table 1 for the input voltage threshold.
2	IN5	Monitored Input Voltage 5. See Table 1 for the input voltage threshold.
3	IN6	Monitored Input Voltage 6. See Table 1 for the input voltage threshold.
4	WDI	Watchdog Timer Input. If WDI remains low or high for longer than the watchdog timeout period, <u>RESET</u> is asserted and the timer is cleared. The timer also clears whenever a reset is asserted or a rising or falling edge on WDI is detected. The watchdog timer enters a startup period that allows 54s for the first transition to occur before a reset. Leave WDI unconnected to disable the watchdog timer. The WDI unconnected-state detector uses a small 400nA current. Therefore, do not connect WDI to anything that will source or sink more than 200nA. Note that the leakage current specification for most three-state drivers exceeds 200nA.
5	GND	Ground
6	V <sub>CC</sub>	Unmonitored Power-Supply Input
7	OUT4	Output 4. When the voltage at IN4 falls below its threshold, OUT4 goes low and stays low until the voltage at IN4 exceeds its threshold. The open-drain output has a 30µA internal pullup to V <sub>CC</sub> .
8	OUT5	Output 5. When the voltage at IN5 falls below its threshold, OUT5 goes low and stays low until the voltage at IN5 exceeds its threshold. The open-drain output has a 30µA internal pullup to V <sub>CC</sub> .
9	OUT6	Output 6. When the voltage at IN6 falls below its threshold, OUT6 goes low and stays low until the voltage at IN6 exceeds its threshold. The open-drain output has a 30µA internal pullup to V <sub>CC</sub> .
10	<u>MR</u>	Active-Low Manual Reset Input. Pull <u>MR</u> low to assert <u>RESET</u> low. <u>RESET</u> remains low for the reset timeout period after <u>MR</u> is deasserted. <u>MR</u> is pulled up to V <sub>CC</sub> through a 20kΩ resistor.
11	SRT	Set Reset Timeout Input. Connect a capacitor from SRT to GND to set the reset timeout period. The reset timeout period can be calculated as follows: Reset Timeout (s) = $2.06 \times 10^6 (\Omega) \times C_{SRT} (F)$ . For the internal timeout period of 140ms (min), connect SRT to V <sub>CC</sub> .
12	MARGIN	Manual Deassert Input. Pull <u>MARGIN</u> low to deassert all outputs (go into high state), regardless of the voltage at any monitored input.
13	OUT3	Output 3. When the voltage at IN3 falls below its threshold, OUT3 goes low and stays low until the voltage at IN3 exceeds its threshold. The open-drain output has a 30µA internal pullup to V <sub>CC</sub> .
14	OUT2	Output 2. When the voltage at IN2 falls below its threshold, OUT2 goes low and stays low until the voltage at IN2 exceeds its threshold. The open-drain output has a 30µA internal pullup to V <sub>CC</sub> .
15	OUT1	Output 1. When the voltage at IN1 falls below its threshold, OUT1 goes low and stays low until the voltage at IN1 exceeds its threshold. The open-drain output has a 30µA internal pullup to V <sub>CC</sub> .
16	<u>RESET</u>	Active-Low Reset Output. <u>RESET</u> asserts low when any of the monitored voltages falls below its respective threshold or <u>MR</u> is asserted. <u>RESET</u> remains asserted for the reset timeout period after all monitored voltages exceed their respective thresholds and <u>MR</u> is deasserted. This open-drain output has a 30µA internal pullup.
17	IN1	Monitored Input Voltage 1. See Table 1 for the input voltage threshold.
18	IN2	Monitored Input Voltage 2. See Table 1 for the input voltage threshold.
19	IN3	Monitored Input Voltage 3. See Table 1 for the input voltage threshold.
20	TOL	Threshold Tolerance Input. Connect TOL to GND to select 5% threshold tolerance. Connect TOL to V <sub>CC</sub> to select 10% threshold tolerance.
—	EP	Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal resistance path from the IC junction to the PCB. Do not use as the electrical connection to GND.

# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

## Pin Description (MAX16062)

PIN	NAME	FUNCTION
1	IN5	Monitored Input Voltage 5. See Table 1 for the input voltage threshold.
2	IN6	Monitored Input Voltage 6. See Table 1 for the input voltage threshold.
3	IN7	Monitored Input Voltage 7. See Table 1 for the input voltage threshold.
4	IN8	Monitored Input Voltage 8. See Table 1 for the input voltage threshold.
5	WDI	Watchdog Timer Input. If WDI remains low or high for longer than the watchdog timeout period, <u>RESET</u> is asserted and the timer is cleared. The timer also clears whenever a reset is asserted or a rising or falling edge on WDI is detected. The watchdog timer enters a startup period that allows 54s for the first transition to occur before a reset. Leave WDI unconnected to disable the watchdog timer. The WDI unconnected state detector uses a small 400nA current. Therefore, do not connect WDI to anything that will source or sink more than 200nA. Note that the leakage current specification for most three-state drivers exceeds 200nA.
6	GND	Ground
7	VCC	Unmonitored Power-Supply Input
8	OUT5	Output 5. When the voltage at IN5 falls below its threshold, OUT5 goes low and stays low until the voltage at IN5 exceeds its threshold. The open-drain output has a 30µA internal pullup to VCC.
9	OUT6	Output 6. When the voltage at IN6 falls below its threshold, OUT6 goes low and stays low until the voltage at IN6 exceeds its threshold. The open-drain output has a 30µA internal pullup to VCC.
10	OUT7	Output 7. When the voltage at IN7 falls below its threshold, OUT7 goes low and stays low until the voltage at IN7 exceeds its threshold. The open-drain output has a 30µA internal pullup to VCC.
11	OUT8	Output 8. When the voltage at IN8 falls below its threshold, OUT8 goes low and stays low until the voltage at IN8 exceeds its threshold. The open-drain output has a 30µA internal pullup to VCC.
12	MR	Active-Low Manual Reset Input. Pull <u>MR</u> low to assert <u>RESET</u> low. <u>RESET</u> remains low for the reset timeout period after <u>MR</u> is deasserted. <u>MR</u> is pulled up to VCC through a 20kΩ resistor.
13	SRT	Set Reset Timeout Input. Connect a capacitor from SRT to GND to set the reset timeout period. The reset timeout period can be calculated as follows: Reset Timeout (s) = $2.06 \times 10^6 (\Omega) \times C_{SRT} (F)$ . For the internal timeout period of 140ms (min), connect SRT to VCC.
14	MARGIN	Margin Disable Input. Pull <u>MARGIN</u> low to deassert all outputs (go into high state), regardless of the voltage at any monitored input.
15	OUT4	Output 4. When the voltage at IN4 falls below its threshold, OUT4 goes low and stays low until the voltage at IN4 exceeds its threshold. The open-drain output has a 30µA internal pullup to VCC.
16	OUT3	Output 3. When the voltage at IN3 falls below its threshold, OUT3 goes low and stays low until the voltage at IN3 exceeds its threshold. The open-drain output has a 30µA internal pullup to VCC.
17	OUT2	Output 2. When the voltage at IN2 falls below its threshold, OUT2 goes low and stays low until the voltage at IN2 exceeds its threshold. The open-drain output has a 30µA internal pullup to VCC.
18	OUT1	Output 1. When the voltage at IN1 falls below its threshold, OUT1 goes low and stays low until the voltage at IN1 exceeds its threshold. The open-drain output has a 30µA internal pullup to VCC.
19	RESET	Active-Low Reset Output. <u>RESET</u> asserts low when any of the monitored voltages falls below its respective threshold or <u>MR</u> is asserted. <u>RESET</u> remains asserted for the reset timeout period after all monitored voltages exceed their respective thresholds and <u>MR</u> is deasserted. This open-drain output has a 30µA internal pullup.
20	IN1	Monitored Input Voltage 1. See Table 1 for the input voltage threshold.
21	IN2	Monitored Input Voltage 2. See Table 1 for the input voltage threshold.
22	IN3	Monitored Input Voltage 3. See Table 1 for the input voltage threshold.
23	IN4	Monitored Input Voltage 4. See Table 1 for the input voltage threshold.
24	TOL	Threshold Tolerance Input. Connect TOL to GND to select 5% threshold tolerance. Connect TOL to VCC to select 10% threshold tolerance.
—	EP	Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal resistance path from the IC junction to the PCB. Do not use as the electrical connection to GND.

**MAX16060/MAX16061/MAX16062**

# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

**Table 1. Input-Voltage-Threshold Selector**

PART	IN1	IN2	IN3	IN4	IN5	IN6	IN7	IN8
MAX16060A	3.3	2.5	ADJ	1.8	—	—	—	—
MAX16060B	3.3	ADJ	ADJ	1.8	—	—	—	—
MAX16060C	ADJ	2.5	ADJ	1.8	—	—	—	—
MAX16060D	3.3	2.5	ADJ	ADJ	—	—	—	—
MAX16060E	ADJ	ADJ	ADJ	ADJ	—	—	—	—
MAX16061A	3.3	2.5	ADJ	1.8	ADJ	ADJ	—	—
MAX16061B	3.3	ADJ	ADJ	1.8	ADJ	ADJ	—	—
MAX16061C	3.3	2.5	ADJ	ADJ	ADJ	ADJ	—	—
MAX16061D	ADJ	2.5	ADJ	1.8	ADJ	ADJ	—	—
MAX16061E	ADJ	ADJ	ADJ	ADJ	ADJ	ADJ	—	—
MAX16062A	3.3	2.5	ADJ	1.8	ADJ	ADJ	ADJ	ADJ
MAX16062B	3.3	ADJ	ADJ	1.8	ADJ	ADJ	ADJ	ADJ
MAX16062C	3.3	2.5	ADJ	ADJ	ADJ	ADJ	ADJ	ADJ
MAX16062D	ADJ	2.5	ADJ	1.8	ADJ	ADJ	ADJ	ADJ
MAX16062E	ADJ							

**Note:** Other fixed thresholds may be available. Contact factory for availability.

# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

## Functional Diagrams

**MAX16060/MAX16061/MAX16062**

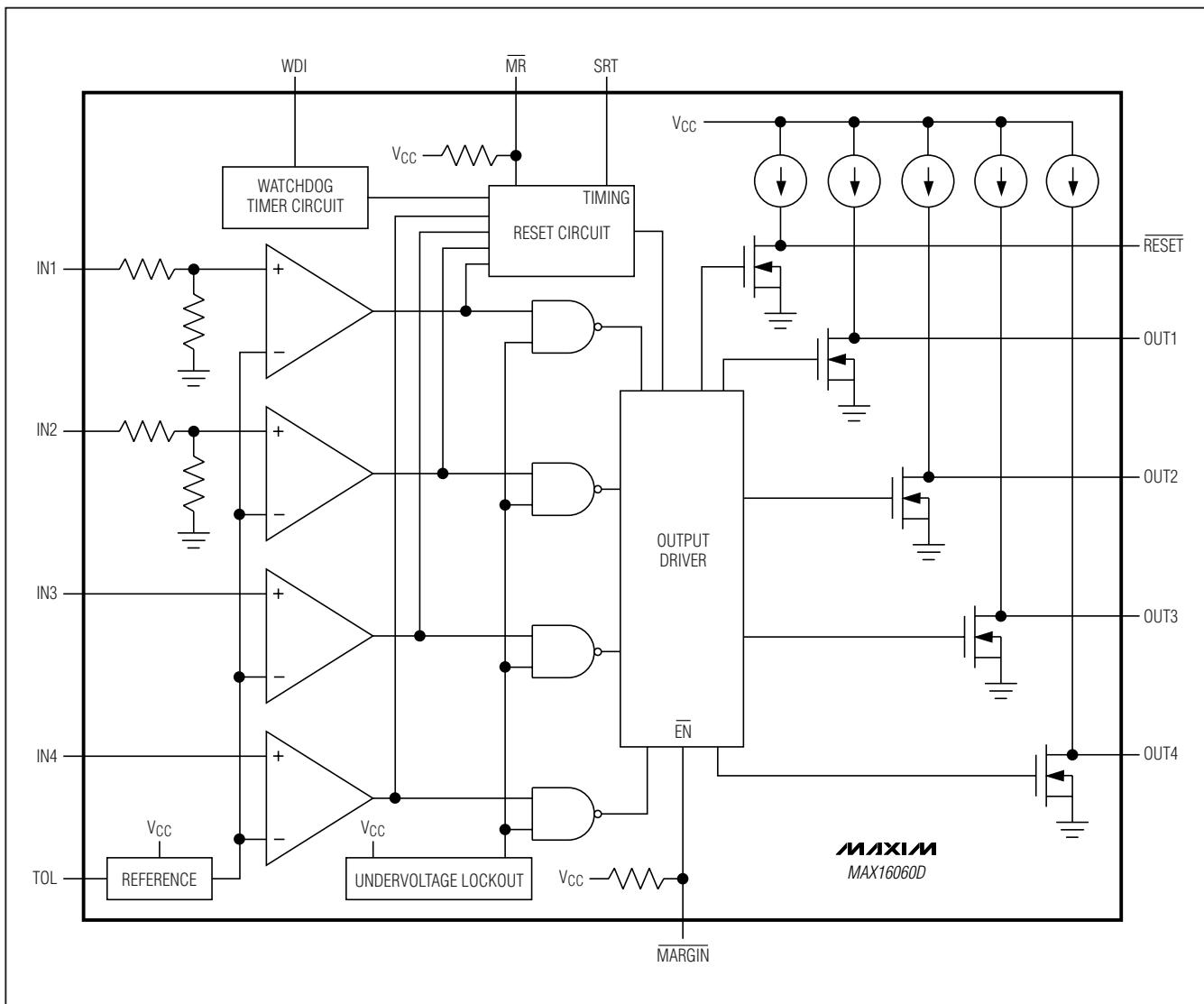


Figure 1. MAX16060D Functional Diagram

# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

## Functional Diagrams (continued)

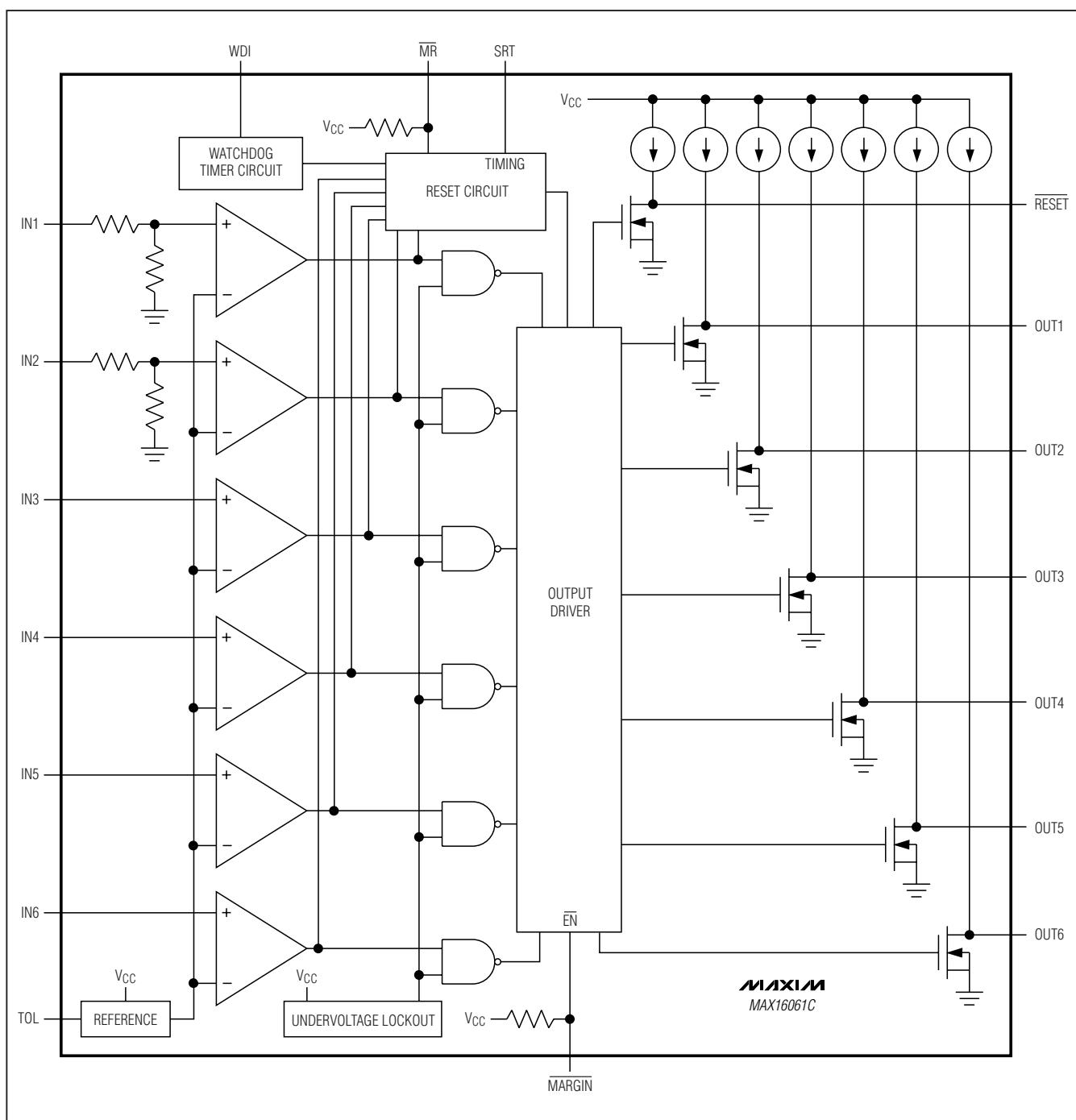


Figure 2. MAX16061C Functional Diagram

# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

## Functional Diagrams (continued)

**MAX16060/MAX16061/MAX16062**

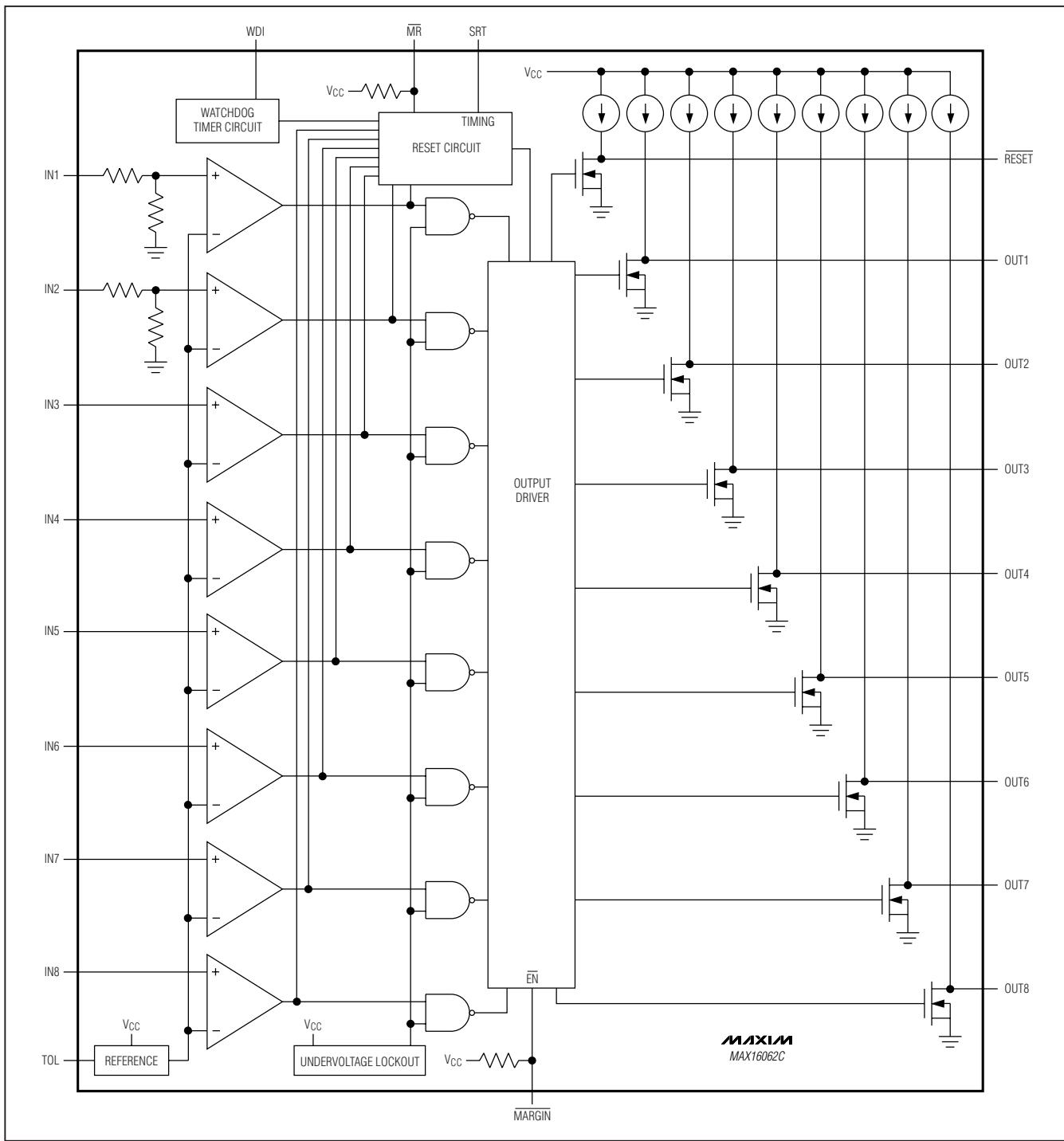


Figure 3. MAX16062C Functional Diagram

# 1% Accurate, Quad-/Hex-/Octal-Voltage μP Supervisors

## Detailed Description

The MAX16060/MAX16061/MAX16062 are 1% accurate low-voltage, quad-/hex-/octal-voltage μP supervisors in a small thin QFN package. These devices provide supervisory functions for complex multivoltage systems. The MAX16060 monitors four voltages; the MAX16061 monitors six voltages; and the MAX16062 monitors eight voltages.

These supervisors offer independent outputs for each monitored voltage along with a reset output that asserts whenever any of the monitored voltages fall below their respective thresholds or the manual reset input is asserted. The reset output remains asserted for the reset timeout after all voltages are above their respective thresholds and the manual reset input is deasserted. The minimum reset timeout is internally set to 140ms or can be adjusted with an external capacitor.

All open-drain outputs have internal 30μA pullups that eliminate the need for external pullup resistors. However, each output can be driven with an external voltage up to 5.5V. Other features offered include a manual reset input, a tolerance pin for selecting 5% or 10% input thresholds, and a margin enable function for deasserting the outputs during margin testing.

An additional feature is a watchdog timer that asserts RESET when the watchdog timeout period (1.6s typ) is exceeded. The watchdog timer can be disabled by leaving WDI unconnected.

## Applications Information

### Undervoltage-Detection Circuit

The open-drain outputs of the MAX16060/MAX16061/MAX16062 can be configured to detect an undervoltage condition. Figure 4 shows a configuration where an LED turns on when the comparator output is low, indicating an undervoltage condition. These devices can also be used in applications such as system supervisory monitoring, multivoltage level detection, and V<sub>CC</sub> bar-graph monitoring (Figure 5).

### Tolerance (TOL)

The MAX16060/MAX16061/MAX16062 feature a pin-selectable threshold tolerance. Connect TOL to GND to select 5% threshold tolerance. Connect TOL to V<sub>CC</sub> to select 10% threshold tolerance.

## Window Detection

A window detector circuit uses two inputs in the configuration shown in Figure 6. External resistors set the two threshold voltages of the window detector circuit. External logic gates create the OUT signal. The window detection width is the difference between the threshold voltages (Figure 7).

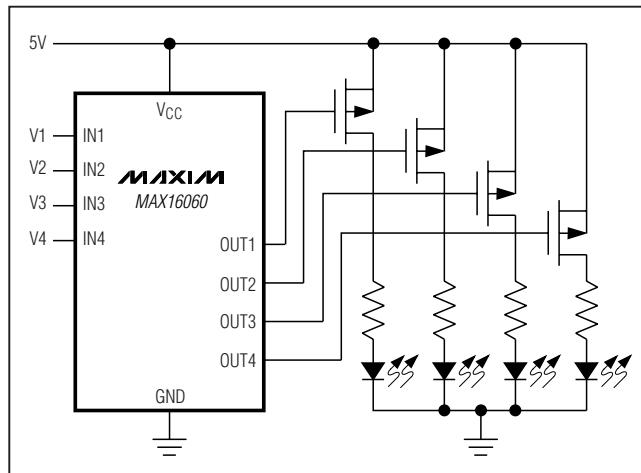


Figure 4. Quad Undervoltage Detector with LED Indicators

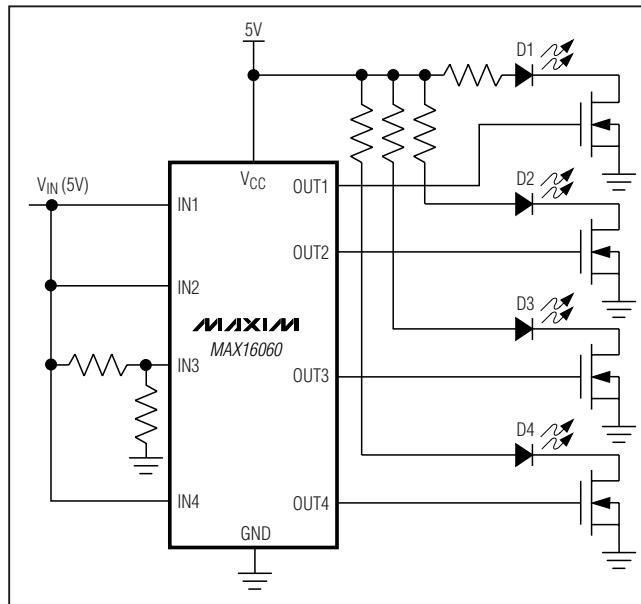


Figure 5. V<sub>CC</sub> Bar-Graph Monitoring

# **1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors**

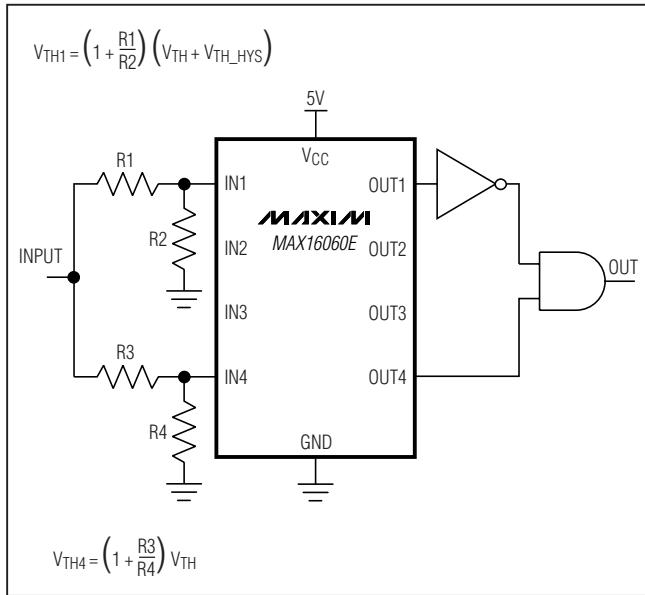


Figure 6. Window Detection

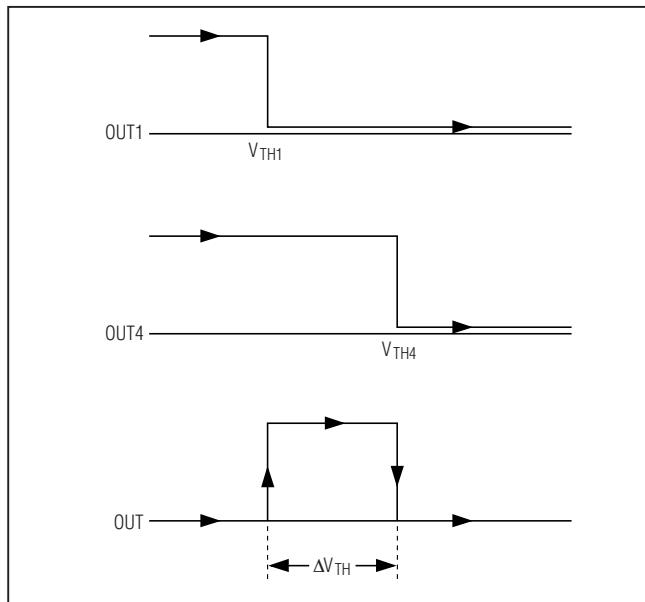
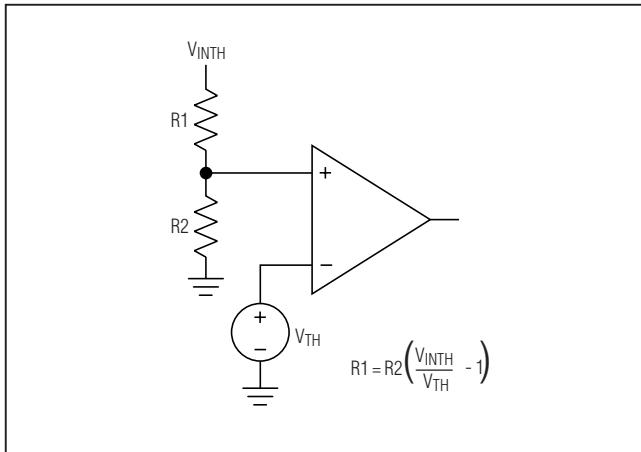


Figure 7. Output Response of Window Detector Circuit



*Figure 8. Setting the Adjustable Input*

## ***Adjustable Input***

These devices offer several monitor options with adjustable input thresholds (see Table 1). The threshold voltage at each adjustable IN\_ input is typically 0.394V (TOL = GND) or 0.373V (TOL = Vcc). To monitor a voltage  $V_{INTH}$ , connect a resistive-divider network to the circuit as shown in Figure 8.

$$V_{INTH} = V_{TH} \left( \frac{R1}{R2} + 1 \right)$$

Large resistors can be used to minimize current through the external resistors. For greater accuracy, use lower-value resistors.

## ***Unused Inputs***

Connect any unused IN\_ inputs to a voltage above its threshold.

## **OUT\_ Outputs**

The OUT<sub>\_</sub> outputs go low when their respective IN<sub>\_</sub> inputs drop below their specified thresholds. The output is open drain with a 30 $\mu$ A internal pullup to V<sub>CC</sub>. For many applications, no external pullup resistor is required to interface with other logic devices. An external pullup resistor to any voltage from 0 to 5.5V overrides the internal pullup if interfacing to different logic supply voltages. Internal circuitry prevents reverse current flow from the external pullup voltage to V<sub>CC</sub> (Figure 9).

# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

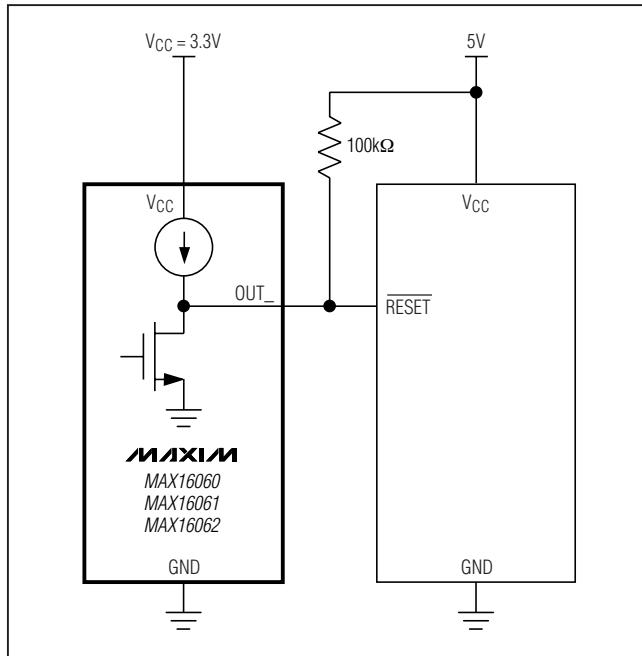


Figure 9. Interfacing to a Different Logic Supply Voltage

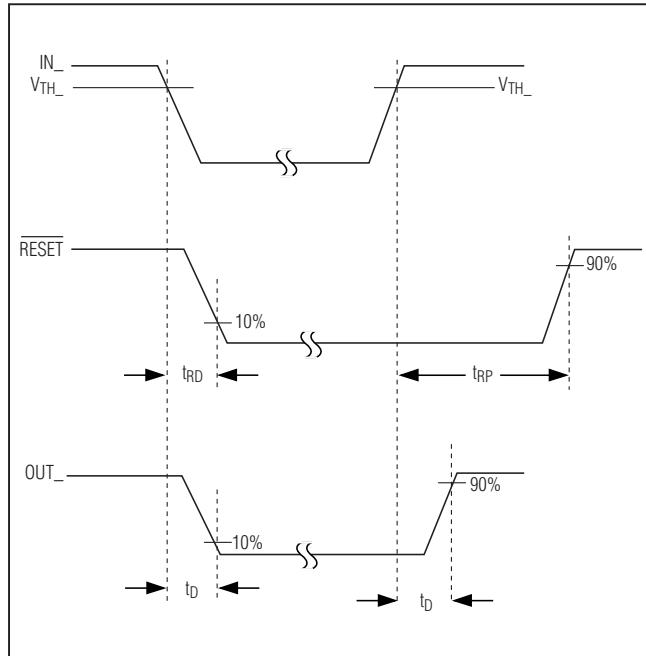


Figure 10. Output Timing Diagram

## RESET Output

RESET asserts low when any of the monitored voltages fall below their respective thresholds or  $\overline{MR}$  is asserted. RESET remains asserted for the reset timeout period after all monitored voltages exceed their respective thresholds and  $\overline{MR}$  is deasserted (see Figure 10). This open-drain output has a 30µA internal pullup. An external pullup resistor to any voltage from 0 to 5.5V overrides the internal pullup if interfacing to different logic supply voltages. Internal circuitry prevents reverse current flow from the external pullup voltage to VCC (Figure 9).

## Reset Timeout Capacitor

The reset timeout period can be adjusted to accommodate a variety of µP applications. Adjust the reset timeout period ( $t_{RP}$ ) by connecting a capacitor ( $C_{SRT}$ ) between SRT and GND. Calculate the reset timeout capacitor as follows:

$$C_{SRT}(F) = \frac{t_{RP}(s) \times I_{SRT}}{V_{TH\_SRT}}$$

Connect SRT to VCC for a factory-programmed reset timeout of 140ms (min).

## Manual Reset Input (MR)

Many µP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic-low on  $\overline{MR}$  asserts  $\overline{RESET}$  low.  $\overline{RESET}$  remains asserted while  $\overline{MR}$  is low, and during the reset timeout period (140ms min) after  $\overline{MR}$  returns high. The  $\overline{MR}$  input has an internal 20kΩ pullup resistor to VCC, so it can be left unconnected if not used.  $\overline{MR}$  can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from  $\overline{MR}$  to GND to create a manual reset function. External debounce circuitry is not required. If  $\overline{MR}$  is driven from long cables or if the device is used in a noisy environment, connecting a 0.1µF capacitor from  $\overline{MR}$  to GND provides additional noise immunity.

# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

## **Margin Output Disable (MARGIN)**

MARGIN allows system-level testing while power supplies are adjusted from their nominal voltages. Drive MARGIN low to force RESET and OUT\_ high, regardless of the voltage at any monitored input. The state of each output does not change while MARGIN = GND. The watchdog timer continues to run when MARGIN is low, and if a timeout occurs, RESET will assert tMD after MARGIN is deasserted.

The MARGIN input is internally pulled up to Vcc. Leave MARGIN unconnected or connect to Vcc if unused.

## **Undervoltage Lockout (UVLO)**

The MAX16060/MAX16061/MAX16062 feature a Vcc undervoltage lockout (UVLO) that preserves a reset status even if Vcc falls as low as 1V. The undervoltage lockout circuitry monitors the voltage at Vcc. If Vcc falls below the UVLO falling threshold (typically

1.735V), RESET is asserted and all OUT\_ are asserted low. This eliminates an incorrect RESET or OUT\_ output state as Vcc drops below the normal Vcc operational voltage range of 1.98V to 5.5V.

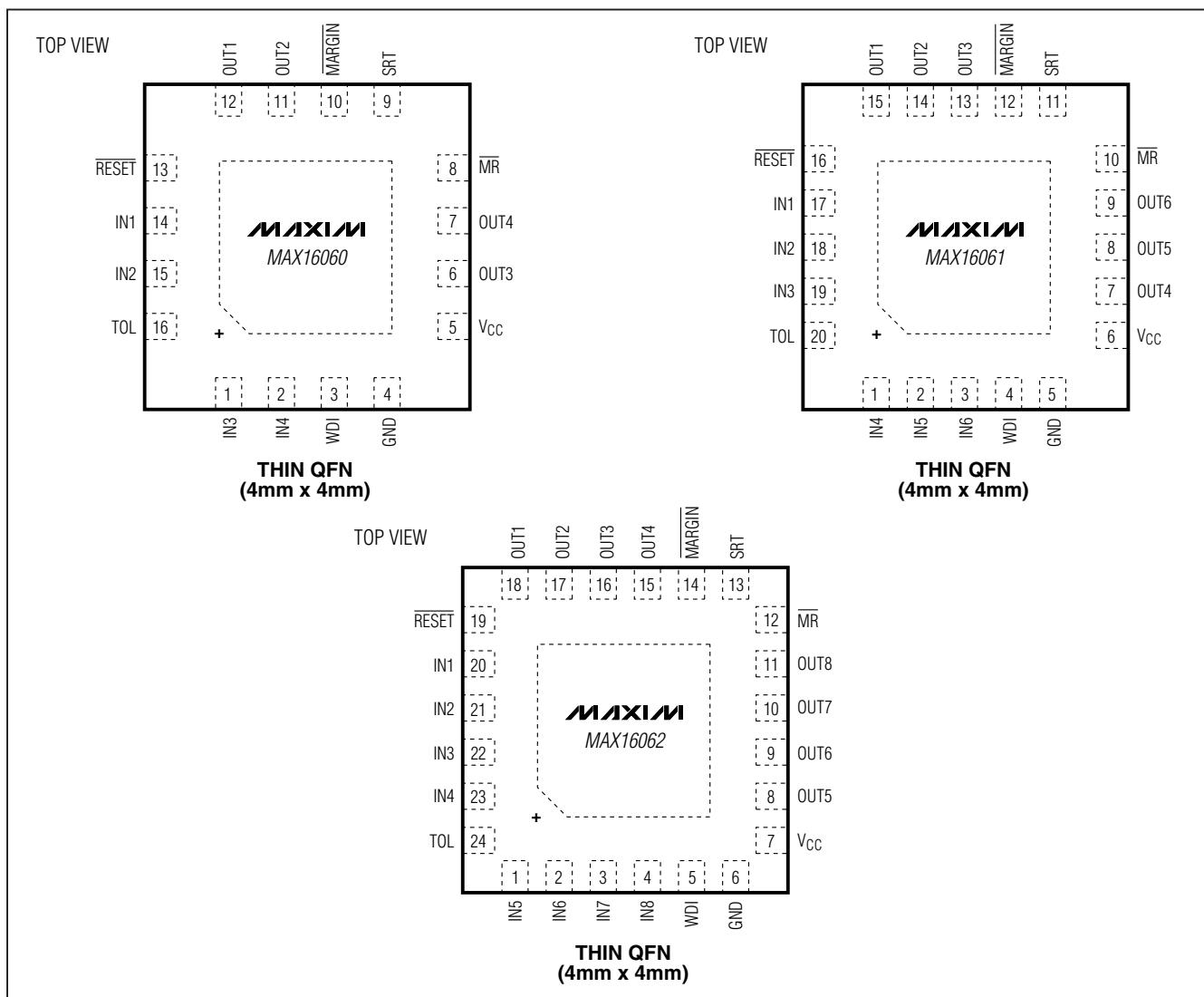
During power-up as Vcc rises above 1V, RESET is asserted and all OUT\_ are asserted low until Vcc exceeds the UVLO threshold. As Vcc exceeds the UVLO threshold, all inputs are monitored and the correct output state appears at all the outputs. This also ensures that RESET and all OUT\_ are in the correct state once Vcc reaches the normal Vcc operational range.

## **Power-Supply Bypassing**

In noisy applications, bypass Vcc to ground with a 0.1µF capacitor as close to the device as possible. The additional capacitor improves transient immunity. For fast-rising Vcc transients, additional capacitance may be required.

# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

## Pin Configurations



## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information, go to  
[www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 TQFN	T1644-4	<a href="#">21-0139</a>
20 TQFN	T2044-3	<a href="#">21-0139</a>
24 TQFN	T2444-4	<a href="#">21-0139</a>

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

18 **Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600**

© 2008 Maxim Integrated Products

**MAXIM** is a registered trademark of Maxim Integrated Products, Inc.

**Данный компонент на территории Российской Федерации****Вы можете приобрести в компании MosChip.**

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибуторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ Р В 0015-002 и ЭС РД 009

**Офис по работе с юридическими лицами:**

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru  
moschip.ru\_4

moschip.ru\_6  
moschip.ru\_9