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January 1997 Revised August 2004

NC7ST08

TinyLogic® HST 2-Input AND Gate

General Description

The NC7ST08 is a single 2-Input high performance CMOS AND Gate, with TTL-compatible inputs. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation. ESD protection diodes inherently guard both inputs and output with respect to the $V_{\rm CC}$ and GND rails. High gain circuitry offers high noise immunity and reduced sensitivity to input edge rate. The TTL-compatible inputs facilitate TTL to NM OS/CMOS interfacing. Device performance is similar to MM74HCT but with 1/2 the output current drive of HC/HCT.

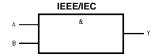
Features

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak™ leadless package
- High Speed: t_{PD} 6 ns (typ), V_{CC} = 5V, C_L = 15 pF, T_A = 25°C
- \blacksquare Low Quiescent Power, $I_{CC} < 1~\mu\text{A},~V_{CC} = 5.5 V$
- \blacksquare Balanced Output Drive; 2 mA I_OL, -2 mA I_OH
- TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7ST08M5X	MA05B	8808	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7ST08P5X	MAA05A	T08	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel
NC7ST08L6X	MAC06A	NN	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

Logic Symbol



Pin Descriptions

Pin Names	Description
A, B	Inputs
Y	Output
NC	No Connect

Function Table

Y = AB

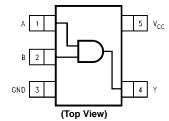
Inp	Output	
Α	В	Y
L	L	L
L	Н	L
Н	L	L
Н	Н	Н

H = HIGH Logic Level

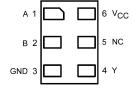
c Level L = LOW Logic Level

Connection Diagrams

Pin Assignments for SC70 and SOT23



Pad Assignment for MicroPak



(Top Thru View)

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Absolute Maximum Ratings(Note 1)

-0.5V to +7.0V Supply Voltage (V_{CC}) DC Input Diode Current (I_{IK})

 $@V_{IN} < -0.5V$ -20 mA $@V_{IN} \ge V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_{IN}) -0.5V to $V_{CC} + 0.5V$

DC Output Diode Current (I_{OK})

 $V_{OUT} < -0.5V$ -20 mA $V_{OUT} > V_{CC} + 0.5V$ +20 mA

Output Voltage (V_{OUT}) -0.5V to $V_{CC} + 0.5V$

DC Output Source or Sink Current

 (I_{OUT}) ±12.5 mA

DC V_{CC} or Ground Current per

Supply Pin (I $_{\rm CC}$ or I $_{\rm GND}$) ±25 mA -65°C to +150°C Storage Temperature (T_{STG}) 150°C

Junction Temperature (T_J)

Lead Temperature (T_L);

(Soldering, 10 seconds) 260°C

Power Dissipation (P_D) @+85°C

SOT23-5 200 mW SC70-5 150 mW

Recommended Operating Conditions (Note 2)

Supply Voltage 4.5V to 5.5V Input Voltage (V_{IN}) 0.0V to $V_{\rm CC}$ Output Voltage (V_{OUT}) 0V to V_{CC} Operating Temperature (T_A) -40°C to +85°C

Input Rise and Fall Time (t_r, t_f)

0 ns to 500 ns $V_{CC} = 5.0V$

Thermal Resistance (θ_{JA})

300°C/W SOT23-5

SC70-5 425°C/W

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of circuits outside the databook specifica-

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

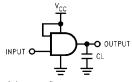
Symbol	Parameter	v _{cc}	$T_A = +25^{\circ}C$		$T_A = 40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	
Cymbol		(V)	Min	Тур	Max	Min	Max	Onnes	Conditions
V _{IH}	HIGH Level Input Voltage	4.5–5.5	2.0			2.0		V	
V _{IL}	LOW Level Input Voltage	4.5–5.5			8.0		0.8	V	
V _{OH}	HIGH Level Output Voltage	4.5	4.4	4.5		4.4			$I_{OH} = -20 \mu A$
		4.5	4.18	4.35		4.13		V	$I_{OH} = -2 \text{ mA}$
									$V_{IN} = V_{IH}$
V _{OL}	LOW Level Output Voltage	4.5		0	0.1		0.1		$I_{OL} = 20 \mu A$
		4.5		0.10	0.26		0.33	V	$I_{OL} = 2 \text{ mA}$
									$V_{IN} = V_{IL}$
I _{IN}	Input Leakage Current	5.5			±0.1		±1.0	μΑ	$0 \le V_{IN} \le 5.5V$
I _{CC}	Quiescent Supply Current	5.5			1.0		10.0	μΑ	$V_{IN} = V_{CC}$ or GND
I _{CCT}	I _{CC} per Input	5.5			2.0		2.9	mA	One Input $V_{IN} = 0.5V$ or 2.4V,
									Other Input V _{CC} or GND

AC Electrical Characteristics

Symbol	Parameter	Vcc	T _A = +25°C		$T_A = 40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	Figure	
		(V)	Min	Тур	Max	Min	Max	Units		Number
t _{PLH} ,	Propagation Delay	5.0		4	12				C 45 mF	
t_{PHL}				6	17			ns	C _L = 15 pF	
		4.5		6	16		20			Figures
				12	27		31	ns	C _I = 50 pF	1, 3
		5.5		5	14		18	115	CL = 50 pr	
				11	26		30			
t _{TLH} ,	Output Transition Time	5.0		4	10			ns	C _L = 15 pF	
t_{THL}		4.5		11	25		31	ns	C ₁ = 50 pF	Figures 1, 3
		5.5		10	21		26	115	OL = 30 pi	1, -
C _{IN}	Input Capacitance	Open			10			pF		
C _{PD}	Power Dissipation Capacitance	5.0		6				pF	(Note 3)	Figure 2

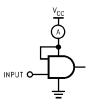
Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{|N}) + (I_{CC}static)$.

AC Loading and Waveforms



 C_L includes load and stray capacitance Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit



 $Input = AC \ Waveform; \ PRR = variable; \ Duty \ Cycle = 50\%$

FIGURE 2. $I_{\rm CCD}$ Test Circuit

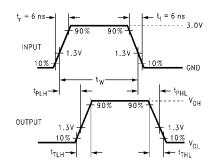
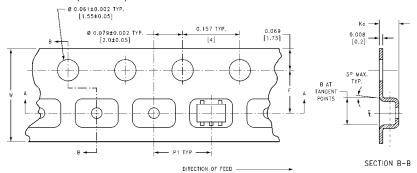


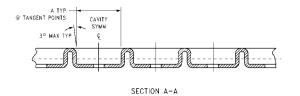
FIGURE 3. AC Waveforms

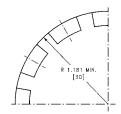
Tape and Reel Specification TAPE FORMAT for SC70 and SOT23

Package	Tape	Number	Cavity	Cover Tape	
Designator	Section	Cavities	Status	Status	
	Leader (Start End)	125 (typ)	Empty	Sealed	
M5X, P5X	Carrier	3000	Filled	Sealed	
	Trailer (Hub End)	75 (typ)	Empty	Sealed	

TAPE DIMENSIONS inches (millimeters)

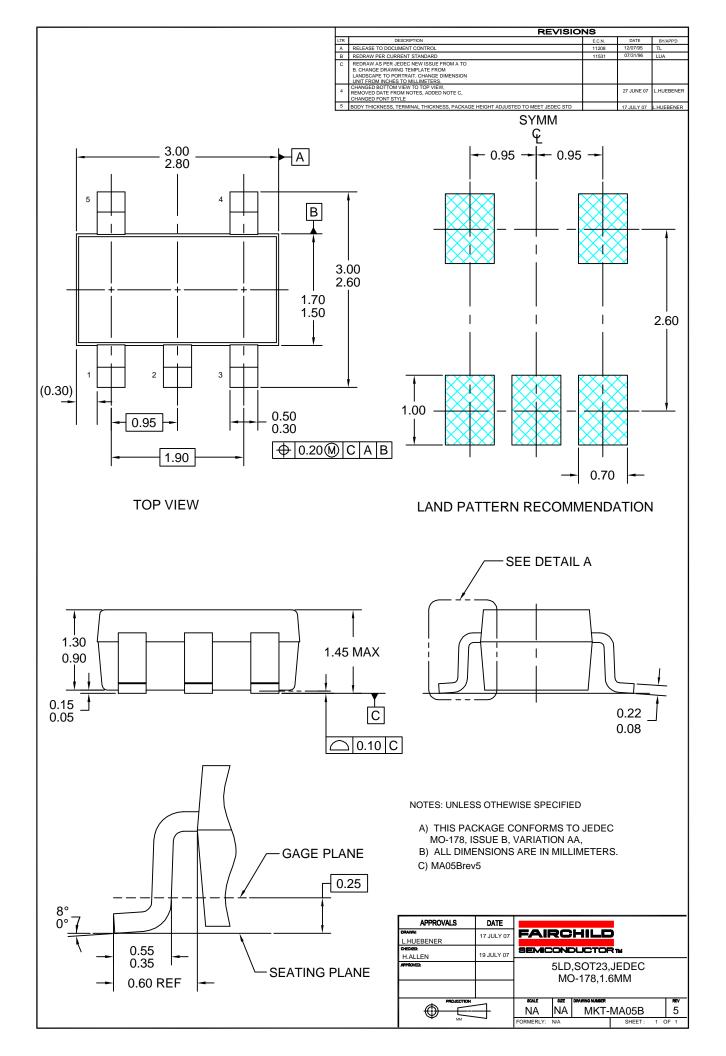


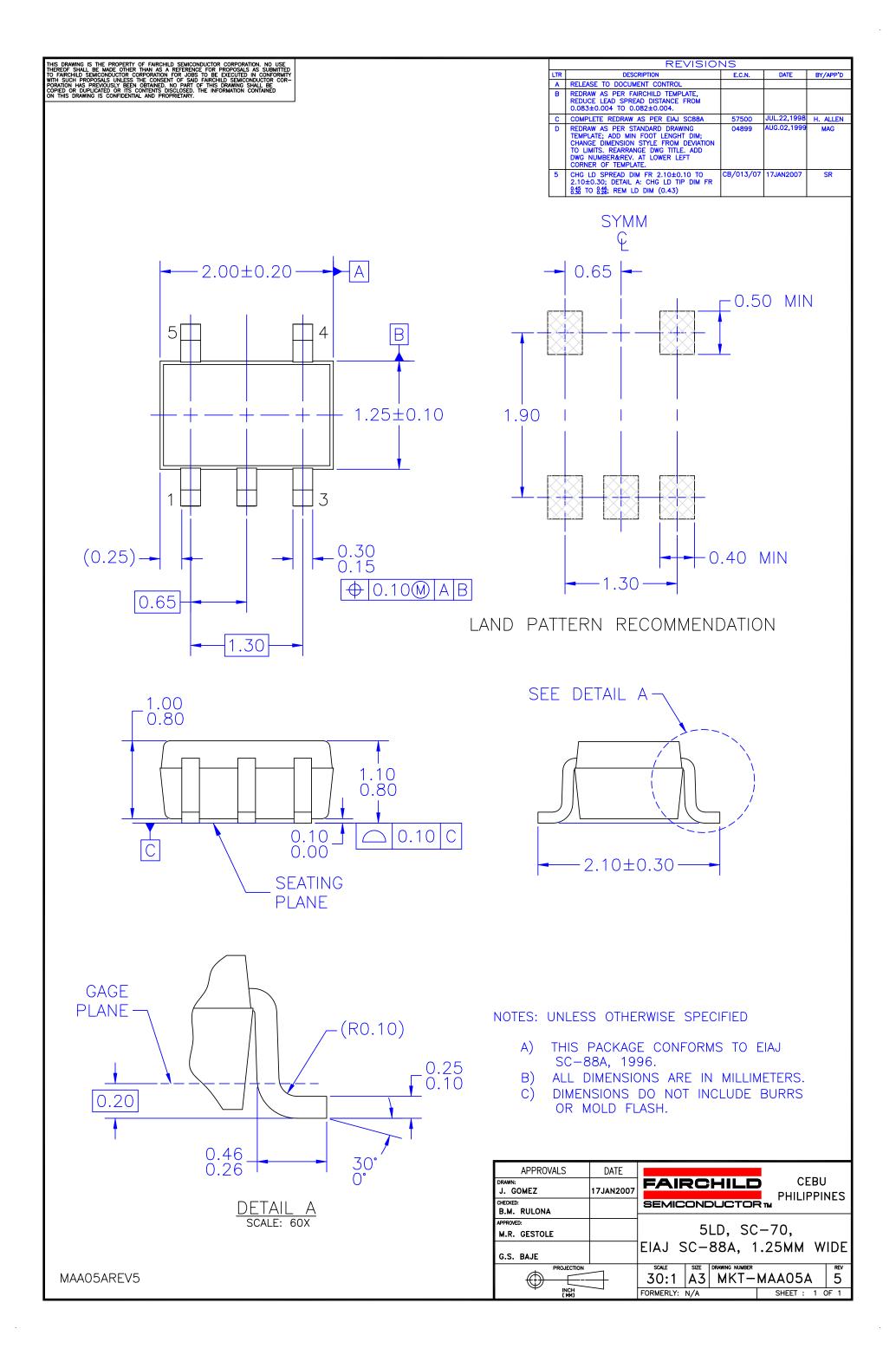


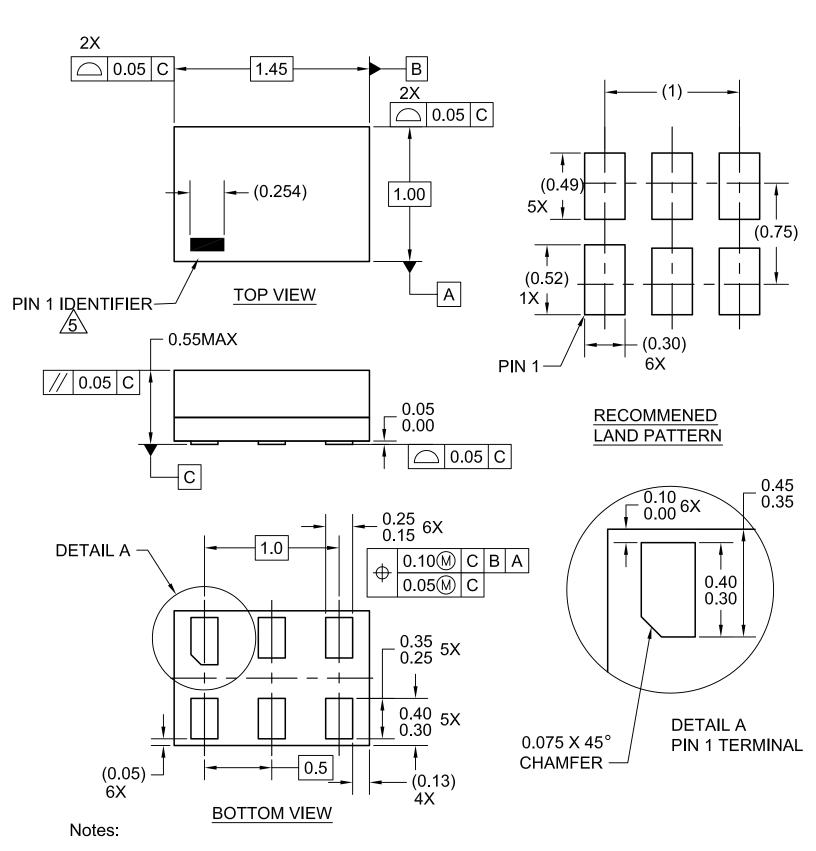


					BEND R	ADIUS NOT TO SO	CALE
Package	Tape Size	DIM A	DIM B	DIM F	DIM K _o	DIM P1	DIM W
SC70-5 8 I	0 mm	0.093	0.096	0.138 ± 0.004	0.053 ± 0.004	0.157	0.315 ± 0.004
	8 mm	(2.35)	(2.45)	(3.5 ± 0.10)	(1.35 ± 0.10)	(4)	(8 ± 0.1)
0.0700.5	0	0.130	0.130	0.138 ± 0.002	0.055 ± 0.004	0.157	0.315 ± 0.012
SOT23-5	8 mm	(3.3)	(3.3)	(3.5 ± 0.05)	(1.4 + 0.11)	(4)	(8 + 0.3)

Tape and Reel Specification (Continued) TAPE FORMAT for MircoPak Package Tape Number Cavity Cover Tape Designator Section Cavities Status Status Leader (Start End) 125 (typ) Empty Sealed L6X Carrier 5000 Filled Sealed Trailer (Hub End) 75 (typ) **Empty** Sealed 2.00-1.75±0.10 В 8.00 ^{+0.30} -0.10 3.50±0.05 1.15±0.05 **-** → В◄ -ø 0.50 ±0.05 SECTION B-B DIRECTION OF FEED SCALE:10X 0.254±0.020 Г 0.70±0.05 SECTION A-A SCALE:10X **REEL DIMENSIONS** inches (millimeters) TAPE SLOT DETAIL X DETAIL X SCALE: 3X W1 W2 W3 Tape В С D Ν Α Size W1 + 0.078/-0.039 0.331 + 0.059/-0.000 7.0 0.567 0.059 0.512 0.795 2.165 8 mm (177.8)(1.50)(13.00)(20.20)(55.00) (8.40 + 1.50 / -0.00)(W1 + 2.00/-1.00)(14.40)







- 1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994
- 4. FILENAME AND REVISION: MAC06AREV4
- 5 PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.





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