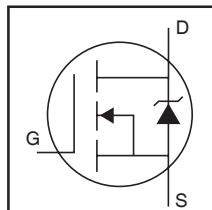


IRF1018EPbF IRF1018ESPbF IRF1018ESLPbF

HEXFET® Power MOSFET

Applications

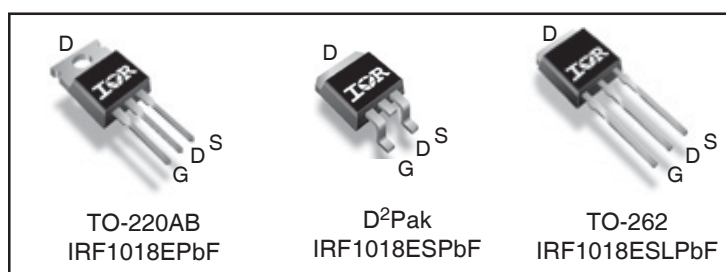
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



V_{DS}		60V
$R_{DS(on)}$	typ.	7.1mΩ
	max.	8.4mΩ
I_D		79A

Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	79	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	56	
I_{DM}	Pulsed Drain Current ①	315	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	110	W
	Linear Derating Factor	0.76	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ③	21	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw ⑨	10lb·in (1.1N·m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	88	mJ
I_{AR}	Avalanche Current ①	47	A
E_{AR}	Repetitive Avalanche Energy ④	11	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	1.32	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface, TO-220	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, TO-220 ⑧	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount), D²Pak ⑦⑧	—	40	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.073	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 5mA$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	7.1	8.4	m Ω	$V_{GS} = 10V, I_D = 47A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 60V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 48V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	110	—	—	S	$V_{DS} = 50V, I_D = 47A$
Q_g	Total Gate Charge	—	46	69	nC	$I_D = 47A$
Q_{gs}	Gate-to-Source Charge	—	10	—		$V_{DS} = 30V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	12	—		$V_{GS} = 10V$ ④
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	34	—		$I_D = 47A, V_{DS} = 0V, V_{GS} = 10V$
$R_{G(int)}$	Internal Gate Resistance	—	0.73	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = 39V$
t_r	Rise Time	—	35	—		$I_D = 47A$
$t_{d(off)}$	Turn-Off Delay Time	—	55	—		$R_G = 10\Omega$
t_f	Fall Time	—	46	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	2290	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	270	—		$V_{DS} = 50V$
C_{rss}	Reverse Transfer Capacitance	—	130	—		$f = 1.0MHz$
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)⑥	—	390	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 60V$ ⑥
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)⑤	—	630	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 60V$ ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	79	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	315		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 47A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	26	39	ns	$T_J = 25^\circ\text{C}$
		—	31	47		$T_J = 125^\circ\text{C}$
Q_{rr}	Reverse Recovery Charge	—	24	36	nC	$T_J = 25^\circ\text{C}$
		—	35	53		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	1.8	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
 ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.08mH$
 $R_G = 25\Omega$, $I_{AS} = 47A$, $V_{GS} = 10V$. Part not recommended for use above this value.
 ③ $I_{SD} \leq 47A$, $di/dt \leq 1668A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
 ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

- ⑤ $C_{oss \text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
 ⑥ $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
 ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
 ⑧ R_θ is measured at T_J approximately 90°C .
 ⑨ This is only applied to TO-220

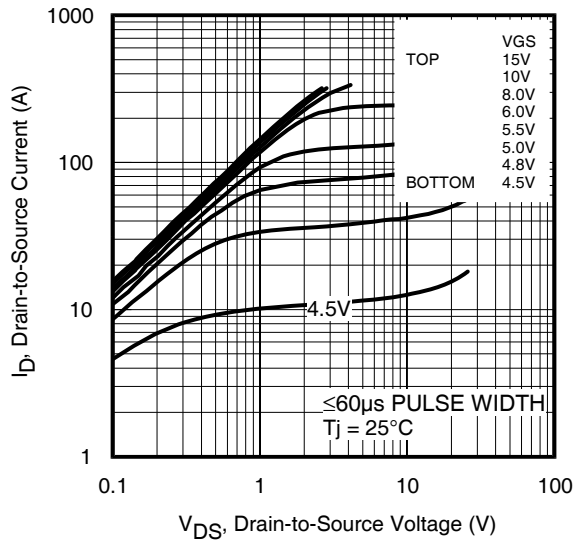


Fig 1. Typical Output Characteristics

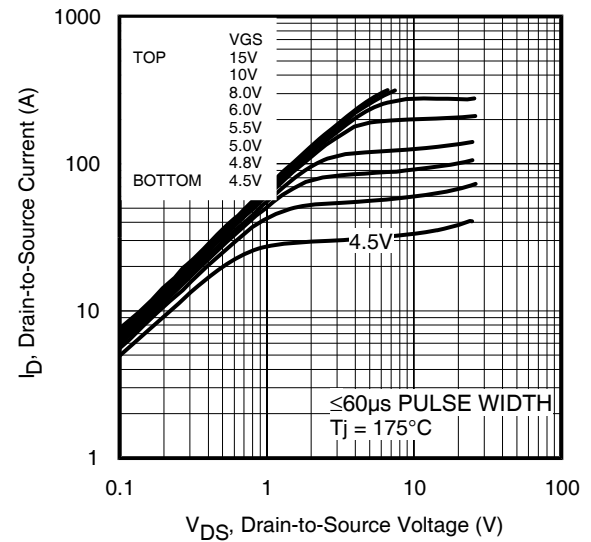


Fig 2. Typical Output Characteristics

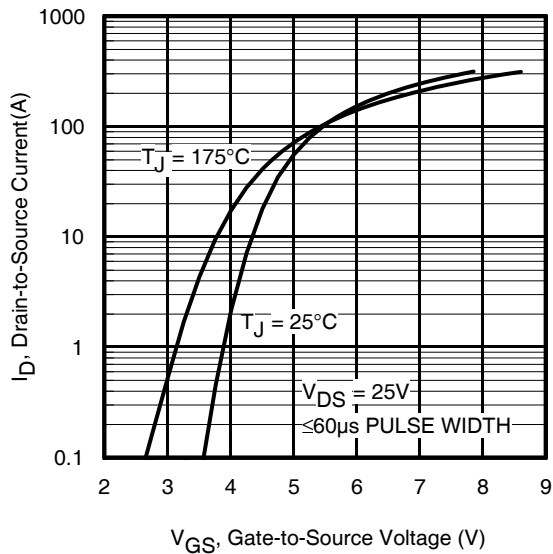


Fig 3. Typical Transfer Characteristics

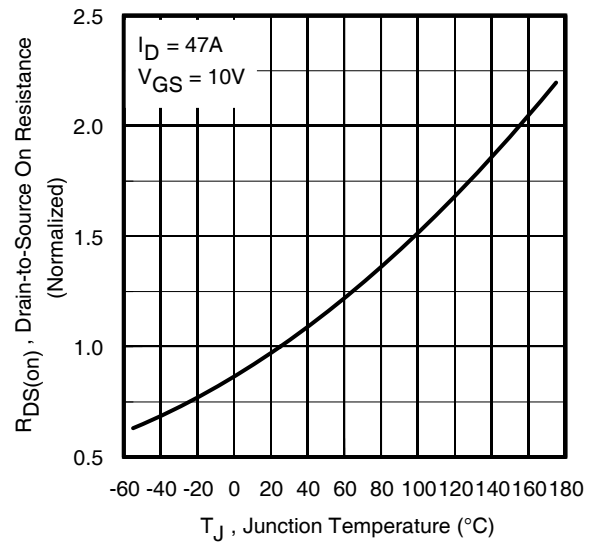


Fig 4. Normalized On-Resistance vs. Temperature

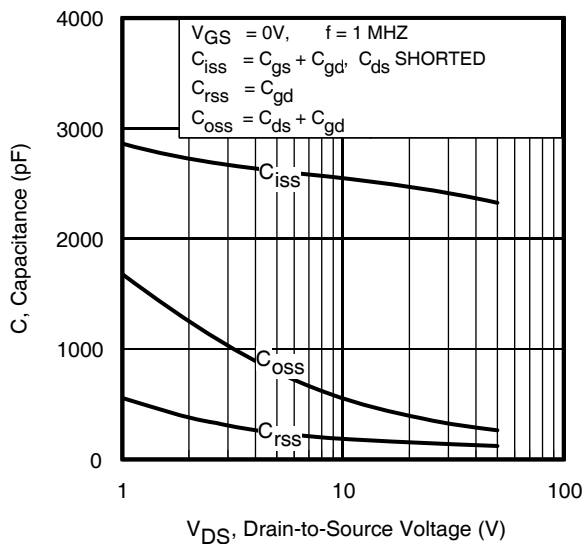


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

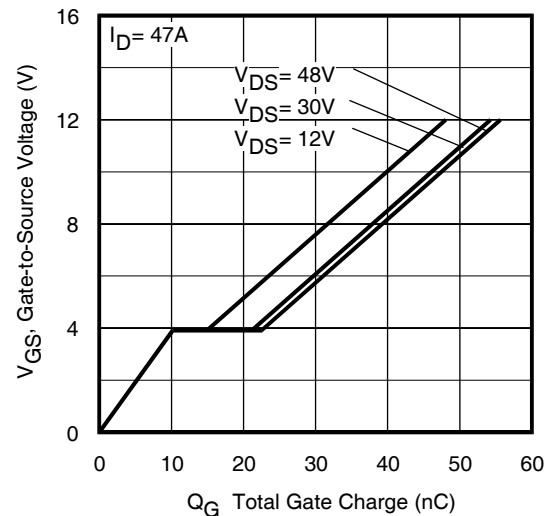


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

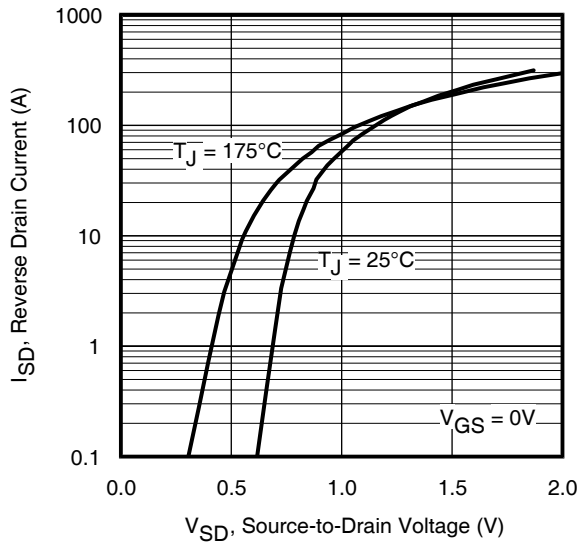


Fig 7. Typical Source-Drain Diode Forward Voltage

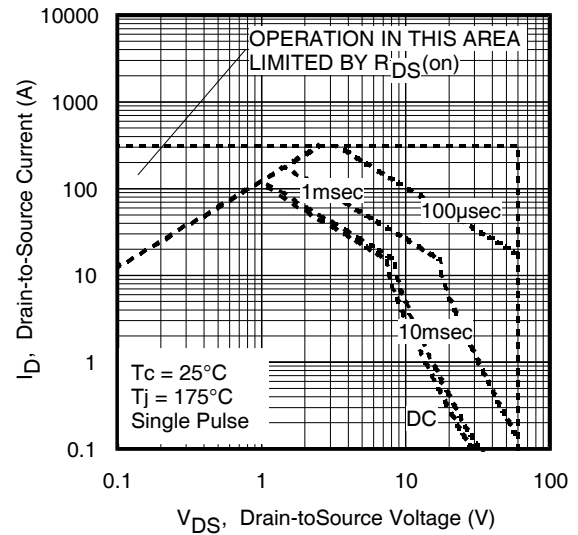


Fig 8. Maximum Safe Operating Area

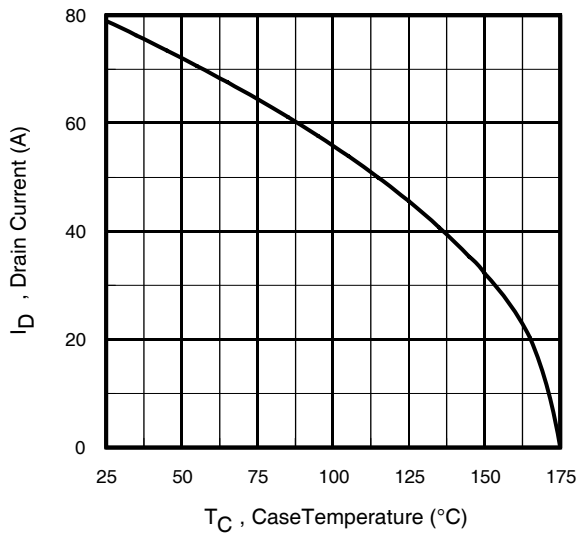


Fig 9. Maximum Drain Current vs. Case Temperature

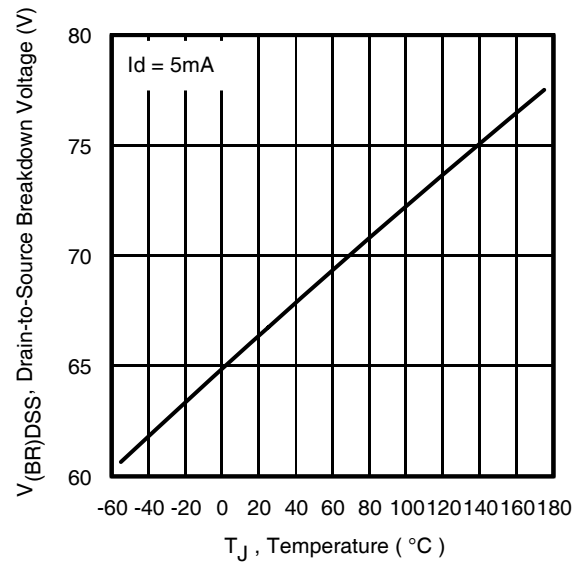


Fig 10. Drain-to-Source Breakdown Voltage

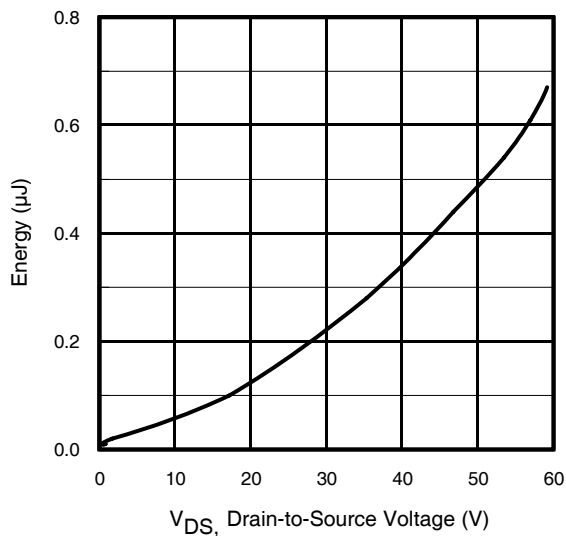


Fig 11. Typical C_{OSS} Stored Energy

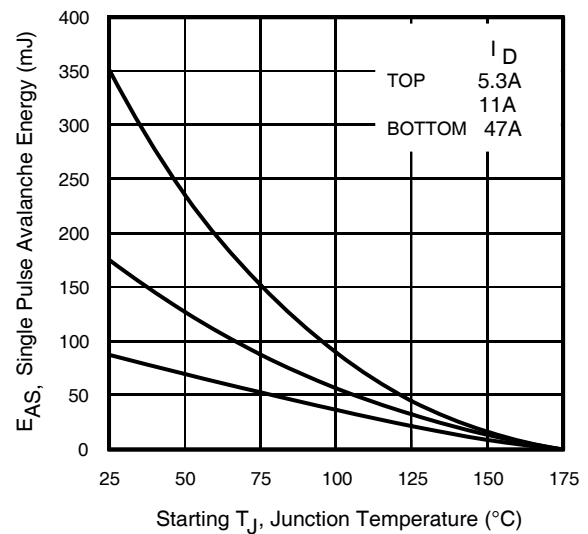


Fig 12. Maximum Avalanche Energy vs. Drain Current
www.irf.com

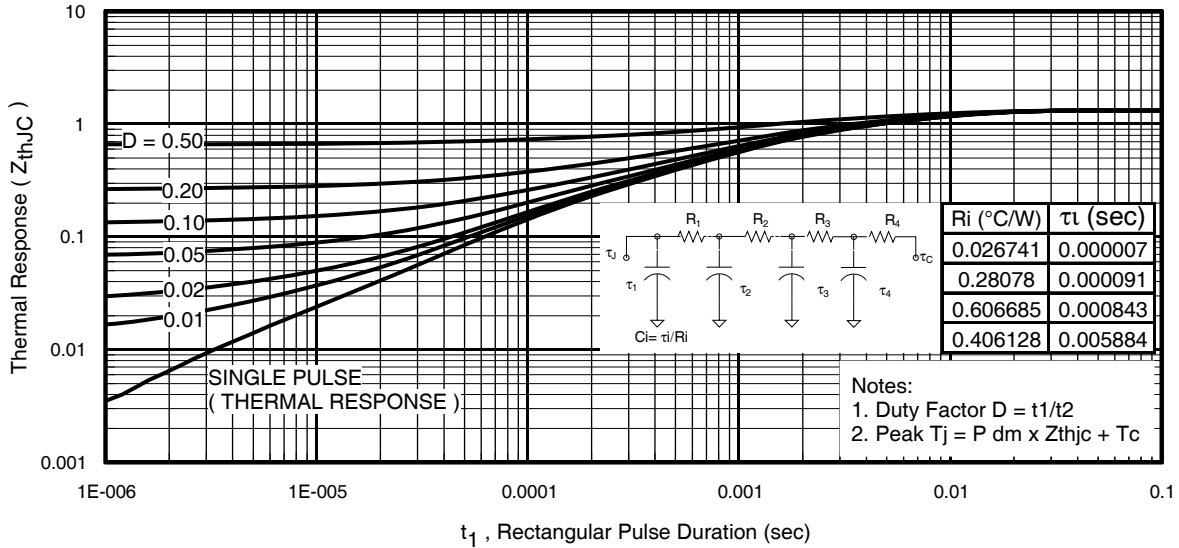


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

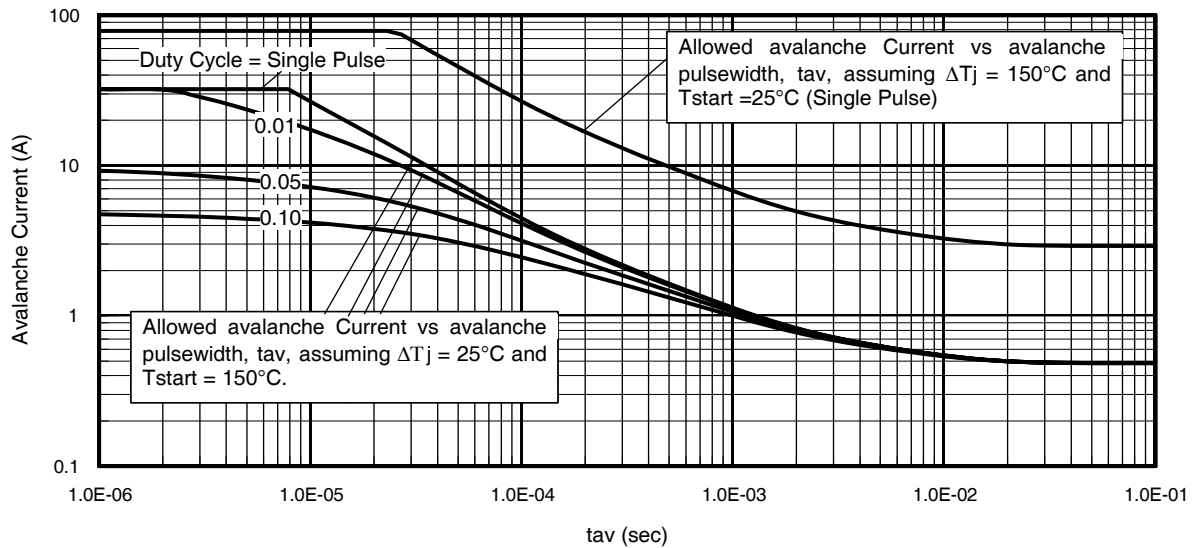


Fig 14. Typical Avalanche Current vs. Pulsewidth

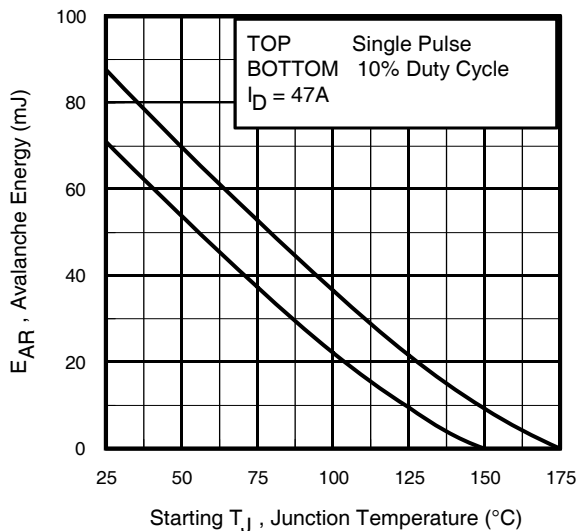


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

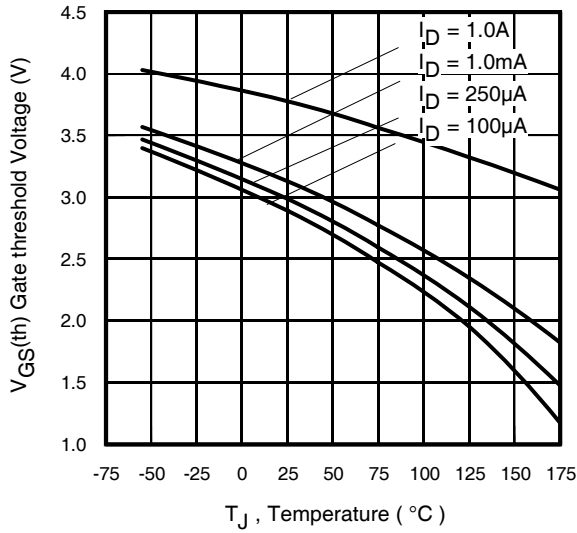


Fig. 16. Threshold Voltage vs. Temperature

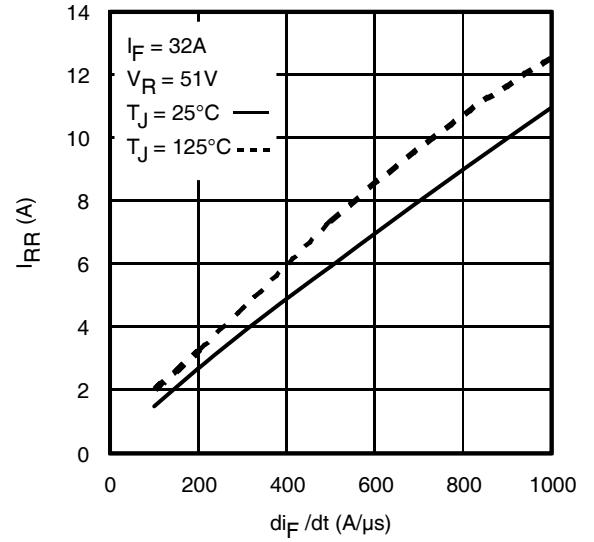


Fig. 17 - Typical Recovery Current vs. di_F/dt

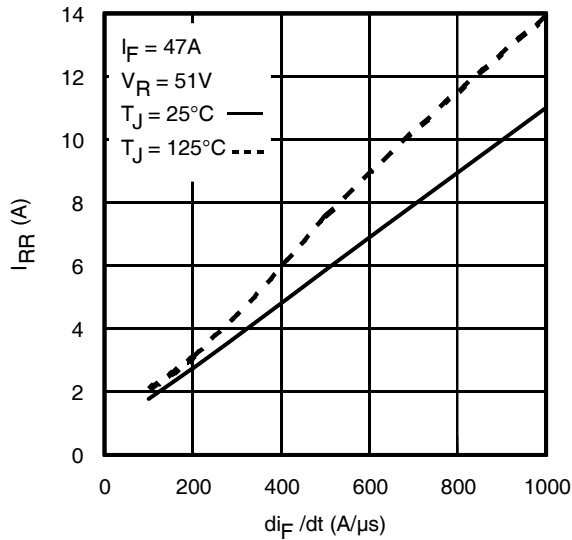


Fig. 18 - Typical Recovery Current vs. di_F/dt

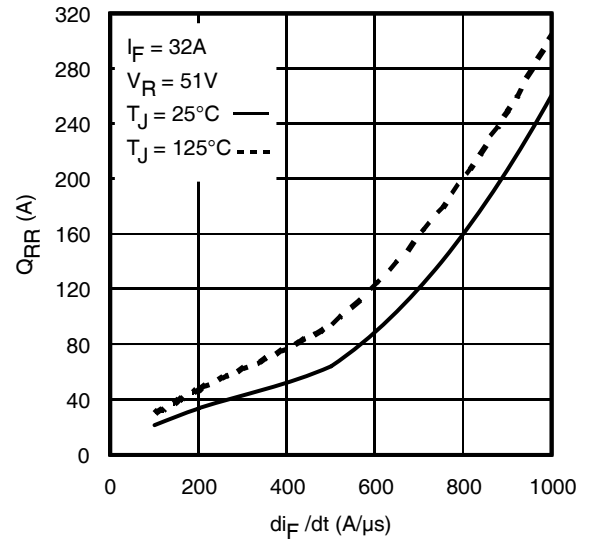


Fig. 19 - Typical Stored Charge vs. di_F/dt

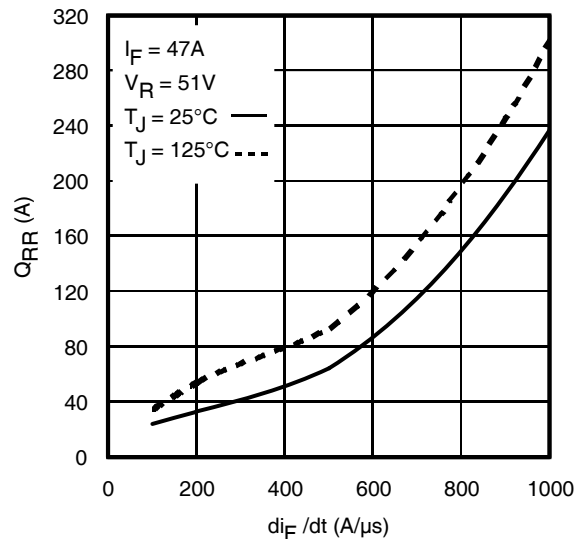


Fig. 20 - Typical Stored Charge vs. di_F/dt

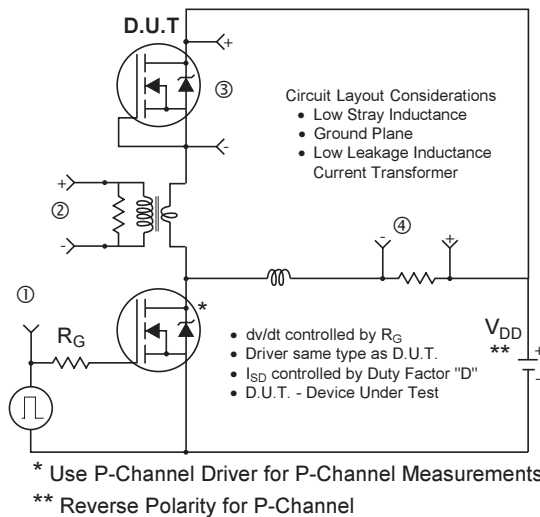


Fig 21. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs

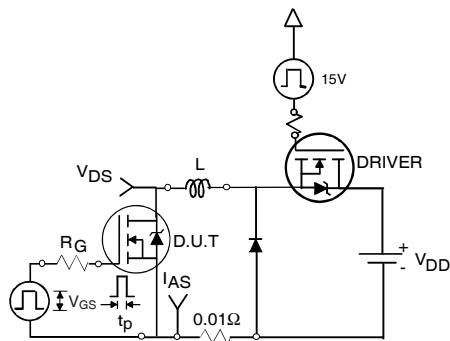
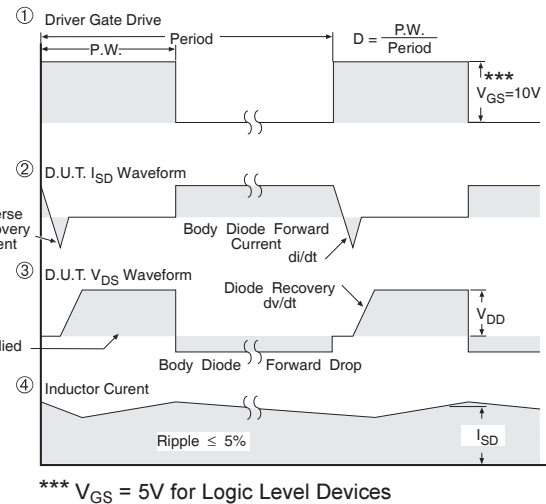


Fig 22a. Unclamped Inductive Test Circuit

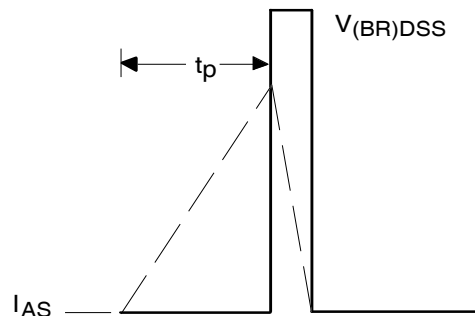


Fig 22b. Unclamped Inductive Waveforms

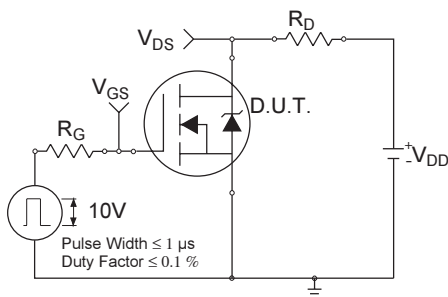


Fig 23a. Switching Time Test Circuit

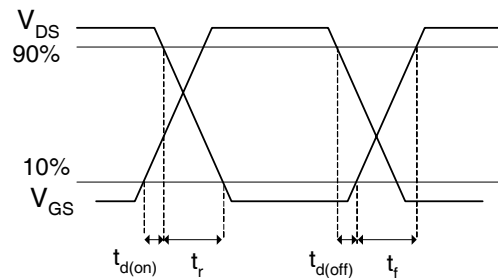


Fig 23b. Switching Time Waveforms

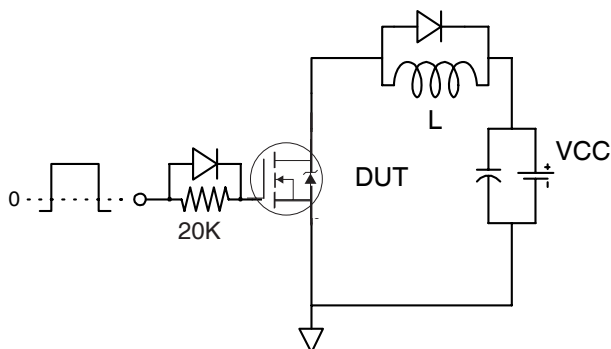


Fig 24a. Gate Charge Test Circuit

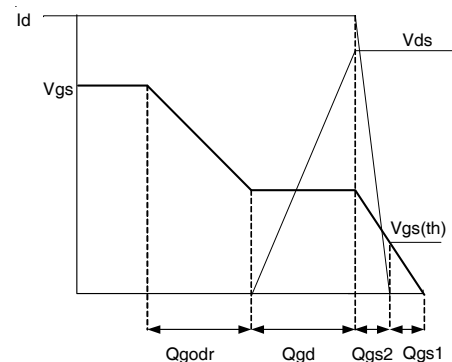


Fig 24b. Gate Charge Waveform

Dimensions are shown in millimeters (inches)



- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONFINED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC 20-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	—	0.76	—	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

HEXFET

1.- GATI

3.- SOU

CDT- C-D

IGBTs, CoPACK

1.- GAT

3.- EMI

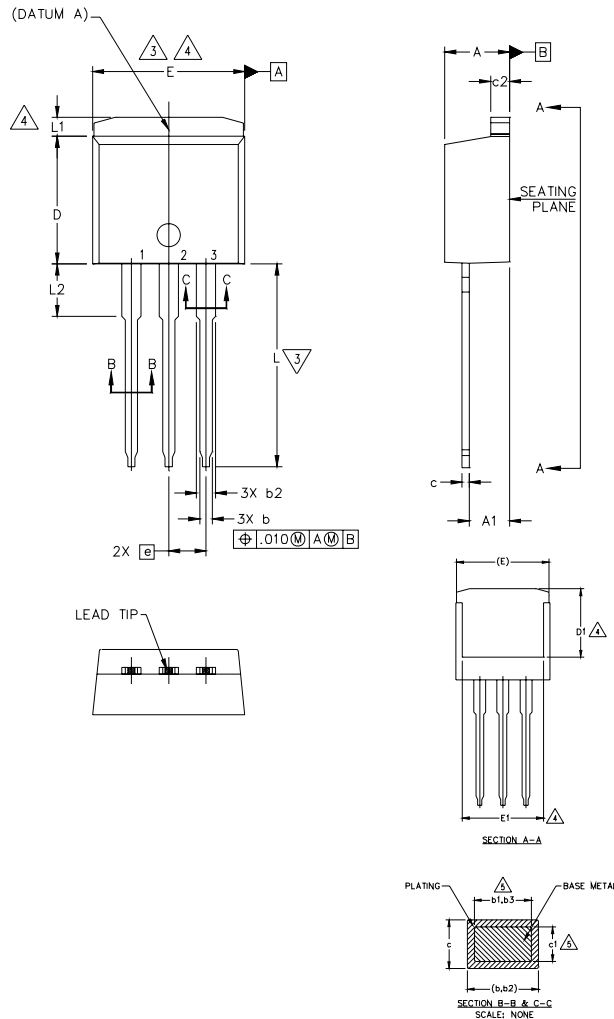
DIODES

1.- AND

3.- ANO

www.irf.com

TO-262 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	—	1.65	—	.065	4
L2	3.56	3.71	.140	.146	

LEAD ASSIGNMENTS

HEXFET

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

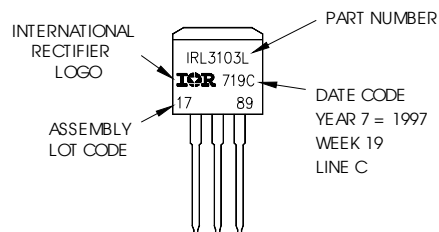
IGBTs, CoPACK

1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

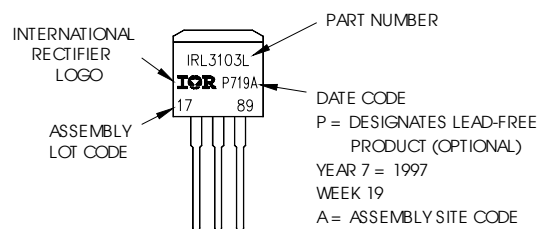
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



OR



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Figure 1 illustrates the dimensioning and tolerancing of a mechanical part. The drawing includes three views: a front view, a side view, and a detail view.

Front View: Shows the main body of the part. Key dimensions include:

- L1**: Distance from the top surface to the center of the central hole.
- L2**: Distance from the bottom surface to the center of the central hole.
- D**: Total height of the part.
- E**: Width of the top flange.
- H**: Height of the central hole.
- 1, 2, 3, 4**: Diameters of various holes and features.
- 2x b2**: Width of the central hole.
- 2x b**: Width of the side holes.
- 2x e**: Width of the bottom flange.

Side View: Shows the profile of the part. Key dimensions include:

- A**: Distance from the top surface to the center of the central hole.
- c2**: Distance from the top surface to the center of the side hole.
- SEATING PLANE**: The surface where the part is seated.

Detail View: Shows a close-up of the seating plane. Key dimensions include:

- c**: Distance from the top surface to the center of the side hole.
- A**: Distance from the top surface to the center of the central hole.

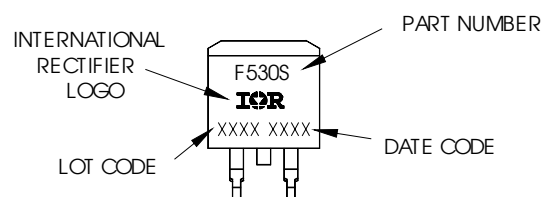
Tolerancing:

- Positional Tolerance:** A feature control frame for the central hole specifies a positional tolerance of ± 0.10 relative to datum A.
- Surface Texture Tolerance:** A feature control frame for the seating plane specifies a surface texture tolerance of ± 0.04 .

Lead Tip: A label pointing to the bottom flange of the part.

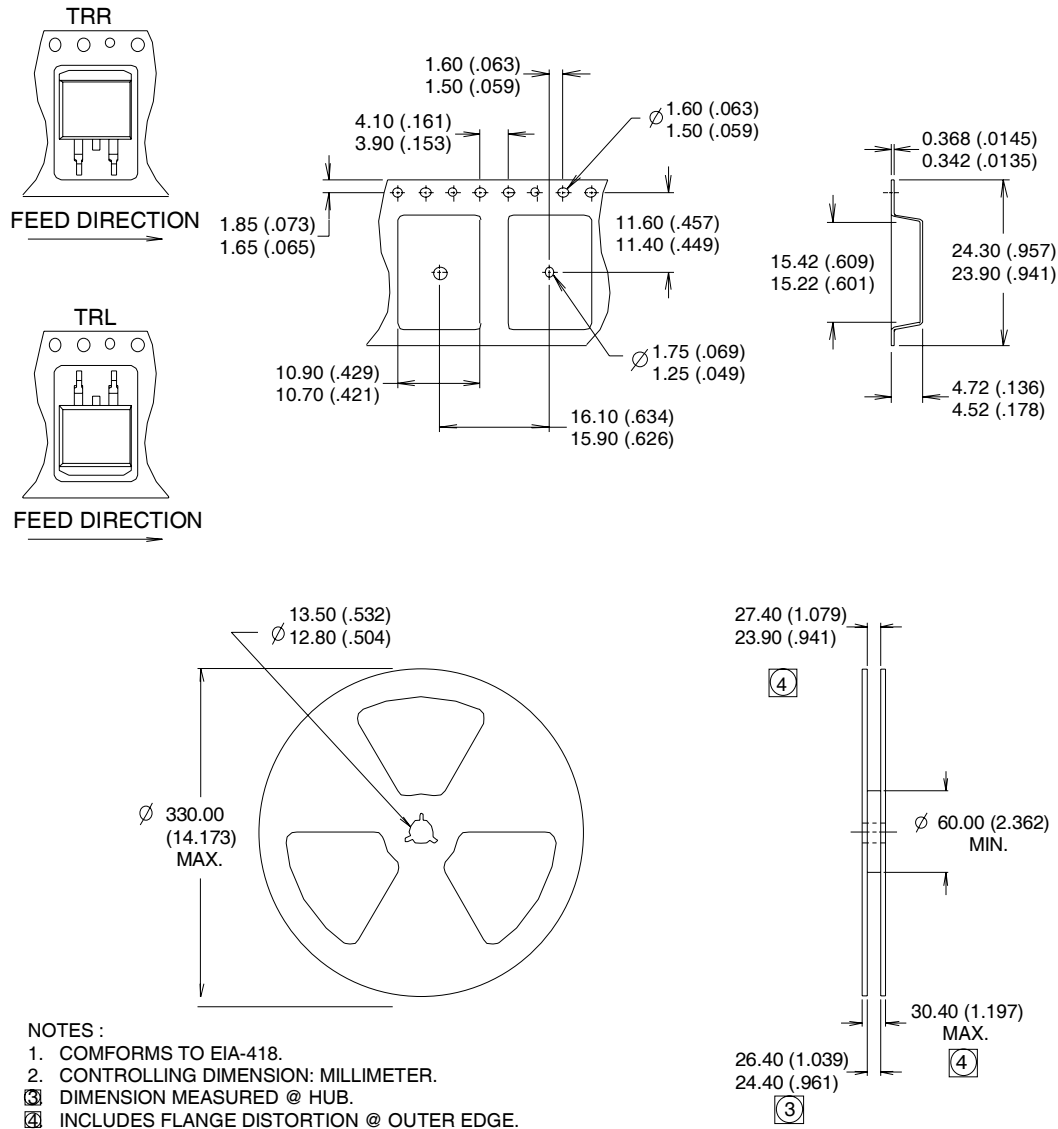
1.- GATE	1.- GATE
2, 4.- DRAIN	2, 4.- COLLECTOR
3.- SOURCE	3.- EMITTER

8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.



www.irf.com

D²Pak Tape & Reel Information



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.2/08

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9