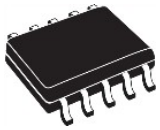
VIPer11

Energy saving offline high voltage converter

Datasheet - production data



SSOP10

Features

- 800 V avalanche-rugged power MOSFET allowing ultra wide VAC input range to be covered
- Embedded HV startup and sense-FET
- Current mode PWM controller
- Drain current limit protection
  - 370 mA (VIPER113)
  - 480 mA (VIPER114)
  - 590 mA (VIPER115)
- Wide supply voltage range: 4.5 V to 30 V
- Minimized system input power consumption:
  - Less than 10 mW at 230 V_{AC} in no-load condition
  - Less than 400 mW at 230 V_{AC} with 250 mW load
- Jittered switching frequency reduces the EMI filter cost:
  - 30 kHz ± 7% (type X)
  - 60 kHz ± 7% (type L)
  - 120kHz ± 7%(type H)
- Embedded E/A with 1.2 V reference
- Protections with automatic restart: overload/short-circuit (OLP), line or output OVP, max. duty cycle counter, VCC clamp
- Pulse-skip protection to prevent flux- runaway
- Embedded thermal shutdown
- Built-in soft-start for improved system reliability

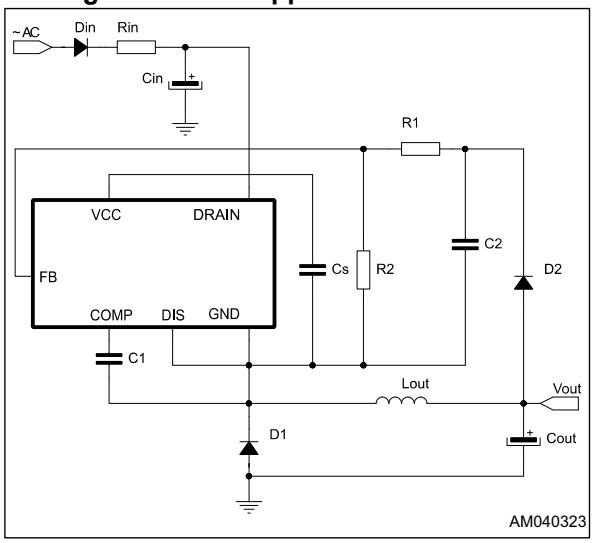
Applications

- Low power SMPS for home appliances, home automation, industrial, consumer, lighting
- Low power adapters

Description

The device is a high voltage converter smartly integrating an 800 V avalanche-rugged power MOSFET with PWM current mode control. The power MOSFET with 800 V breakdown voltage allows the extended input voltage range to be applied, as well as the size of the DRAIN snubber circuit to be reduced. This IC meets the most stringent energy-saving standards as it has very low consumption and operates in pulse frequency modulation under light load. The design of flyback, buck and buck boost converters is supported. The integrated HV startup, sense-FET, error amplifier and oscillator with jitter allow a complete application to be designed with the minimum number of components.

Figure 1. Basic application schematic



Contents

1 Pin setting

Figure 2. Connection diagram

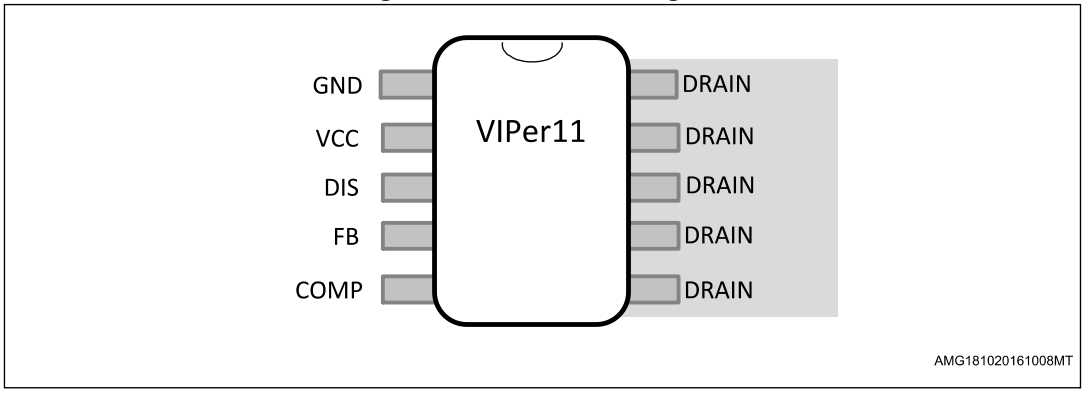


Table 1. Pin description

SSOP10	Name	Function
1	GND	**Ground and MOSFET source.** Connection of source of the internal MOSFET and the return of the bias current of the device. All groundings of bias components must be tied to a trace going to this pin and kept separate from the pulsed current return.
2	VCC	**Controller supply.** An external storage capacitor has to be connected across this pin and GND. The pin, internally connected to the high voltage current source, provides the VCC capacitor charging current at startup. A small bypass capacitor (0.1 µF typ.) in parallel, placed as close as possible to the IC, is also recommended, for noise filtering purpose.
3	DIS	**Disable.** If its voltage exceeds the internal threshold V_{DIS_th} (1.2 V typ.) for more than t_{DEB} time (1 ms, typ.), the PWM is disabled for $t_{DIS\_RESTART}$ (500msec, typ.) in auto-restart mode, resuming normal operation as soon as V_{DIS} falls below V_{DIS_th}. An input overvoltage protection can be built by connecting a voltage divider between the DIS pin and the rectified mains. In case of non-isolated topologies, with the same principle an output overvoltage protection can be implemented. If the disable function is not required, the DIS pin must be soldered to GND, which excludes the function.
4	FB	**Direct feedback.** It is the inverting input of the internal transconductance E/A, which is internally referenced to 1.2 V with respect to GND. In case of non-isolated converter, the output voltage information is directly fed into the pin through a voltage divider. In case of primary regulation, the FB voltage divider is connected to the VCC. The E/A is disabled soldering FB to GND.

Table 1. Pin description (continued)

SSOP10	Name	Function
5	COMP	**Compensation.** It is the output of the internal E/A. A compensation network is placed between this pin and GND to achieve stability and good dynamic performance of the control loop. In case of secondary feedback, the internal E/A must be disabled and the COMP directly driven by the optocoupler to control the DRAIN peak current setpoint.
6 to 10	DRAIN	**MOSFET drain.** The internal high voltage current source sinks current from this pin to charge the VCC capacitor at startup and during steady-state operation. These pins are mechanically connected to the internal metal PAD of the MOSFET in order to facilitate heat dissipation. On the PCB a copper area must be placed under these pins in order to decrease the total junction-to-ambient thermal resistance thus facilitating the power dissipation.

2 Electrical and thermal ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter[1], [2]	Min.	Max.	Unit
V_{DS}	6 to 10	Drain-to-source (ground) voltage	-	800	V
I_{DRAIN}	6 to 10	Pulsed drain current (pulse-width limited by SOA)	-	2	A
V_{CC}	2	VCC voltage	-0.3	Internally limited	V
I_{CC}	2	VCC internal Zener current (pulsed)	-	45[3]	mA
V_{DIS}	3	DIS voltage	-0.3	5[4]	V
V_{FB}	4	FB voltage	-0.3	5[4]	V
V_{COMP}	5	COMP voltage	-0.3	5([4]	V
P_{TOT}	-	Power dissipation at T_{amb} < 50 °C	-	1[5]	W
T_J	-	Junction temperature operating range	-40	150	°C
T_{STG}	-	Storage temperature	-55	150	°C

1. Stresses beyond those listed absolute maximum ratings may cause permanent damage to the device.
2. Exposure to absolute-maximum-rated conditions for extended periods may affect the device reliability.
3. Pulse-width limited by maximum power dissipation, P_{TOT}.
4. The AMR value is intended when $V_{CC} \geq 5$ V, otherwise the value V_{CC} + 0.3 V has to be considered.
5. When mounted on a standard single side FR4 board with 100 mm² (0.1552 inch) of Cu (35 µm thick).

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
R_{TH-JC}	Thermal resistance junction to case[1] (Dissipated power = 1 W)	10	°C/W
R_{TH-JA}	Thermal resistance junction ambient[1] (Dissipated power = 1 W)	155	°C/W
R_{TH-JC}	Thermal resistance junction to case[2] (Dissipated power = 1 W)	5	°C/W
R_{TH-JA}	Thermal resistance junction ambient[2] (Dissipated power = 1 W)	95	°C/W

1. When mounted on a standard single side FR4 board with minimum copper area.
2. When mounted on a standard single side FR4 board with 100 mm^2 (0.155 sq in) of Cu (35 µm thick).

Figure 3. R_{thJA} / (R_{thJA} at A = 100 mm²)

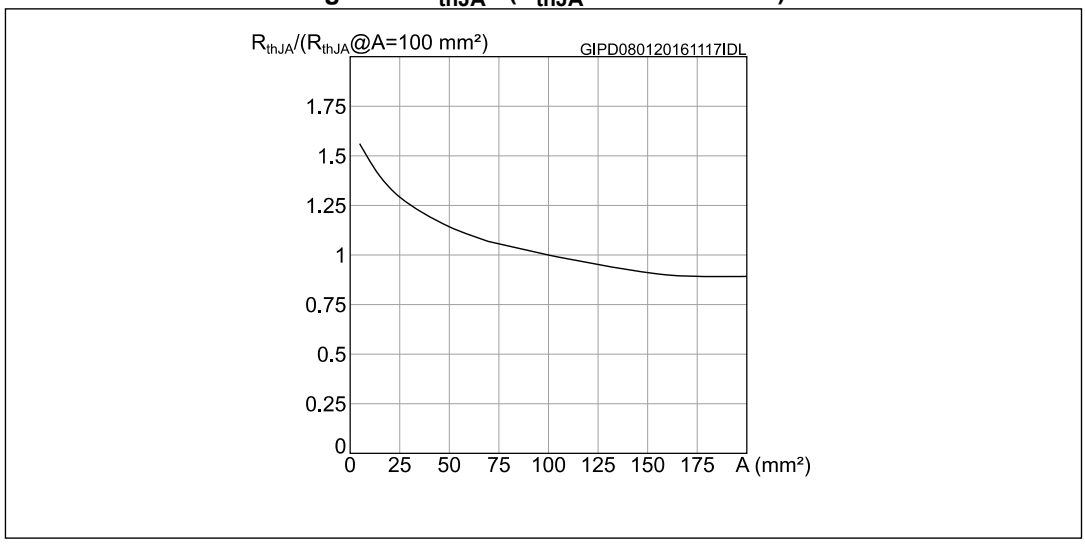


Table 4. Avalanche characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{AR}	Avalanche current	Repetitive and non-repetitive. Pulse-width limited by T_{Jmax}	-	-	0.8	A
E_{AS}	Single pulse avalanche energy(1)	I_{AS} = $I_{AR\ VDS}$ = 100 V Starting T_J = 25 °C	-	-	1	mJ

1. Parameter derived by characterization.

3 Electrical characteristics

T_j = -40 to 125 °C, V_{CC} = 9 V (unless otherwise specified).

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BVDSS}	Breakdown voltage	I_{DRAIN} = 1 mA V_{COMP} = GND T_J = 25 °C	800	-	-	V
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V V_{COMP} = GND T_J = 25 °C	-	-	1	µA
I_{OFF}	OFF-state drain current	V_{DRAIN} = max. rating V_{COMP} = GND T_J = 25 °C	-	-	45	
$R_{DS(on)}$	Static drain-source ON-resistance	I_{DRAIN} = 295 mA T_J = 25 °C	-	-	17	Ω
		I_{DRAIN} = 295 mA T_J = 125 °C	-	-	34	

Table 6. Supply section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
High voltage start-up current source						
V_{BVDSS_SU}	Breakdown voltage of start-up MOSFET	T_J = 25 °C	800	-	-	V
V_{HV_START}	Drain-source start-up voltage	-	-	-	26	V
R_G	Start-up resistor	$V_{FB} > V_{FB\_REF}$ V_{DRAIN} = 400 V V_{DRAIN} = 600 V	28	34	40	MΩ
I_{CH1}	VCC charging current at startup	V_{DRAIN} = 100 V V_{CC} = 0 V	0.7	1	1.3	mA
I_{CH2}	VCC charging current at startup	$V_{FB} > VF_{FB\_REF}$ V_{DRAIN} = 100 V V_{CC} = 6 V	2	3	4	
I_{CH3}(1)	Max. VCC charging current in self-supply	$V_{FB} > V_{FB\_REF}$ V_{DRAIN} = 100 V V_{CC} = 6 V	6.5	7.5	8.5	
IC supply and consumptions						
V_{CC}	Operating voltage range	VGND = 0 V	4.5	-	30	V
$V_{CCclamp}$	Clamp voltage	$I_{CC} = I_{clamp\_max}$	30	32.5	35	V

Table 6. Supply section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{clamp\ max}$	Clamp shutdown current	(2)	30	35	40	mA
$t_{clamp\ max}$	Clamp time before shutdown	-	325	500	675	µs
V_{CCon}	VCC start-up threshold	V_{FB} = 1.2 V V_{DRAIN} = 400 V	15	16	17	V
V_{CSon}	HV current source turn-on threshold	V_{CC} falling	4	4.25	4.5	V
V_{CCoff}	UVLO	V_{FB} = 1.2 V V_{DRAIN} = 400 V	3.75	4	4.25	V
I_q	Quiescent current	Not switching $V_{FB} > V_{FB\_REF}$	-	0.3	0.45	mA
I_{CC}	Operating supply current, switching	V_{DS} = 150 V V_{COMP} = 1.2 V F_{OSC} = 30 kHz	-	1	1.2	mA
		V_{DS} = 150 V V_{COMP} = 1.2 V F_{OSC} = 60 kHz	-	1.25	1.5	
		V_{DS} = 150 V V_{COMP} = 1.2 V F_{OSC} = 120 kHz	-	1.5	1.8	

1. Current supplied during the main MOSFET OFF time only.
2. Parameter assured by design and characterization.

Table 7. Controller section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E/A						
V_{FB_REF}	Reference voltage	-	1.175	1.2	1.225	V
V_{FB_DIS}	E/A disable voltage	-	150	180	210	mV
$I_{FB\ PULL\ UP}$	Pull-up current	-	0.9	1	1.1	µA
G_M	Transconductance	V_{COMP} = 1.5 V $V_{FB} > V_{FB\_REF}$	350	500	650	µA/V
I_{COMP1}	Max. source current	V_{COMP} = 1.5 V V_{FB} = 0.5 V	75	100	125	µA
I_{COMP2}	Max. sink current	V_{FB} = 2 V V_{COMP} = 1.5 V	75	100	125	µA
$R_{COMP(DYN)}$	Dynamic resistance	V_{COMP} = 2.7 V V_{FB} = GND	55	65	75	kΩ

Table 7. Controller section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
H_{COMP}	ΔV_{COMP} / ΔI_{DRAIN}	VIPer11**3***	5.9		10.5	V/A
		VIPer11**4***	4.3		8	
		VIPer11**5***	3.8		7	
V_{COMPH}	Current limitation threshold	-	-	3	-	V
V_{COMPL}	PFM threshold	-	-	0.8	-	V
OLP and timing						
I_{DLIM}	Drain current limitation	T_J = 25 °C VIPER11**3***	350	370	389	mA
		T_J = 25 °C VIPER11**4***	456	480	504	
		T_J = 25 °C VIPER11**5***	560	590	620	
I^2f	Power coefficient	$I_{DLIM\_TYP}^2$ x F_{OSC_TYPP}	0.9 ·I^2f	I^2f	1.1 ·I^2f	A^2·kHz
I_{DLIM_PFM}	Drain current limitation at light load	T_J = 25 °C V_{COMP} = V_{COMPL} (1) VIPER11**3***	75	100	135	mA
		T_J = 25 °C V_{COMP} = V_{COMPL} (1) VIPER11**4***	90	115	140	
		T_J = 25 °C V_{COMP} = V_{COMPL} (1) VIPER11**5***	105	130	155	
V_{DIS_th}	Disable threshold voltage	V_{CC} = 9 V V_{COMP} = 1 V V_{FB} = V_{FB_REF}	1.15	1.2	1.25	V
t_{DIS}	Debounce time before DIS protection tripping	-	0.65	1	1.35	ms
$t_{DIS\_RESTART}$	Restart time after DIS protection tripping	-	325	500	675	ms
t_{OVL}	Overload delay time	-	45	50	55	ms
t_{OVL_MAX}	Max. overload delay time	VIPER11*X F_{OSC} = $F_{OSC\ MIN}$	90	100	110	ms
		VIPER11*L F_{OSC} = $F_{OSC\ MIN}$	180	200	220	
		VIPER11*H F_{OSC} = $F_{OSC\ MIN}$	360	400	440	
t_{SS}	Soft-start time	-	5	8	11	ms

Table 7. Controller section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{ON_MIN}	Minimum turn-on time	V_{CC} = 9 V V_{COMP} = 1 V V_{FB} = V_{FB_REF}	250	300	350	ns
$t_{RESTART}$	Restart time after fault	-	0.65	1	1.35	s
Oscillator						
F_{OSC}	Switching frequency	T_J = 25 °C VIPER11*X	27	30	33	kHz
		T_J = 25 °C VIPER11*L	54	60	66	
		T_J = 25 °C VIPER11*H	108	120	132	
F_{OSC_MIN}	Minimum switching frequency	T_J = 25 °C(2)	13.5	15	16.5	kHz
F_D	Modulation depth	(3)	-	±7 FOSC	-	%
F_M	Modulation frequency	(3)	-	260	-	Hz
D_{MAX}	Max. duty cycle	(3)	70		80	%
Thermal shutdown						
T_{SD}	Thermal shutdown temperature	(3)	150	160		°C

1. See *Section 5.10: Pulse frequency modulation on page 21*.
2. See *Section 5.7: Pulse-skipping on page 20*.
3. Parameter assured by design and characterization.

4 Typical electrical characteristics

Figure 4. I_{DLIM} vs T_J

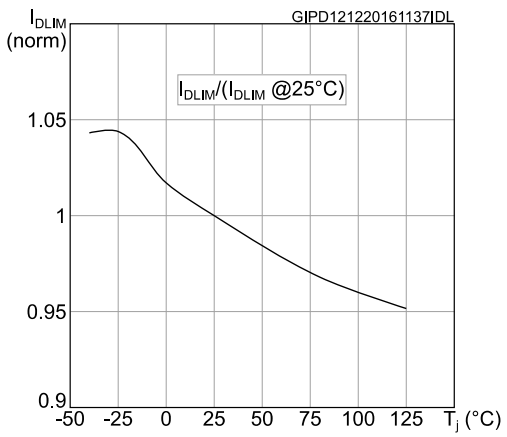


Figure 5. I_{FOSC} vs T_J

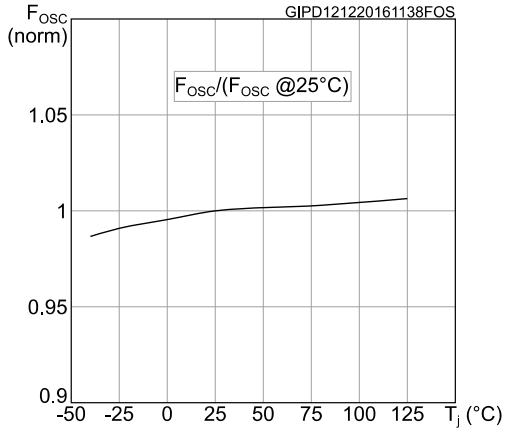


Figure 6. V_{HV_START} vs T_J

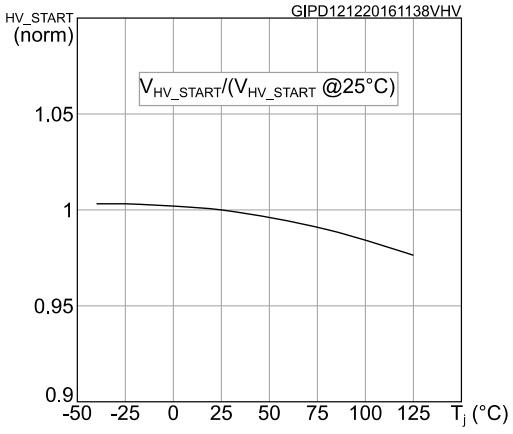


Figure 7. V_{FB_REF} vs T_J

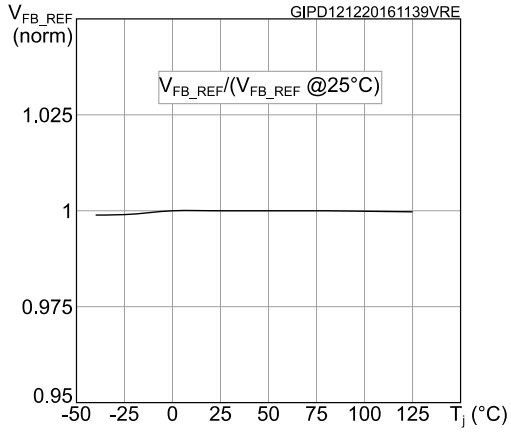


Figure 8. Quiescent current Iq vs T_J

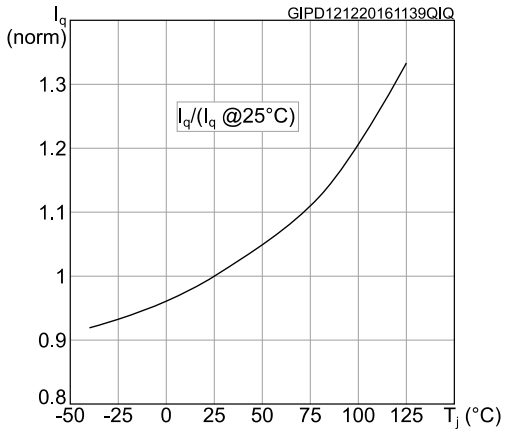


Figure 9. Operating current I_{CC} vs T_J

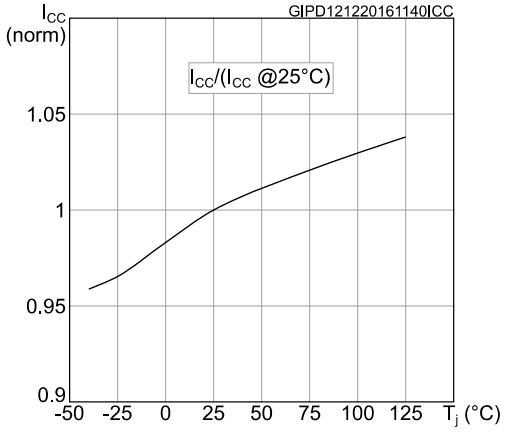


Figure 10. I_{CH1} vs T_J

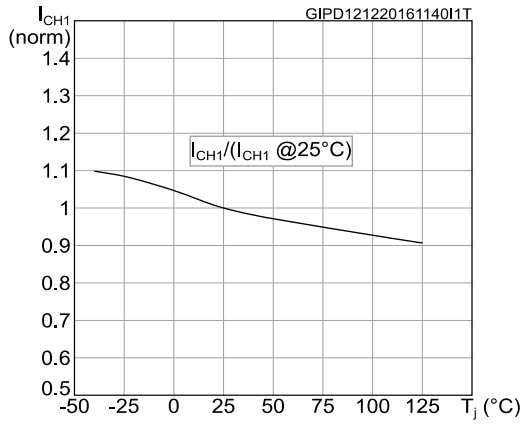


Figure 11. I_{CH1} vs V_{DRAIN}

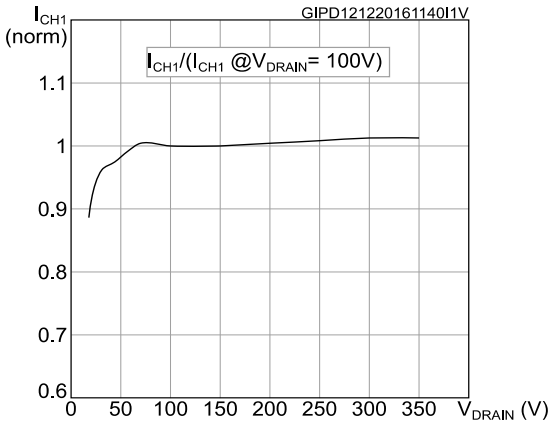


Figure 12. I_{CH2} vs T_J

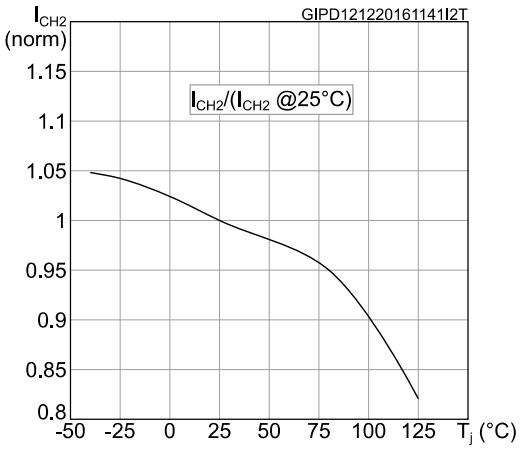


Figure 13. I_{CH2} vs V_{DRAIN}

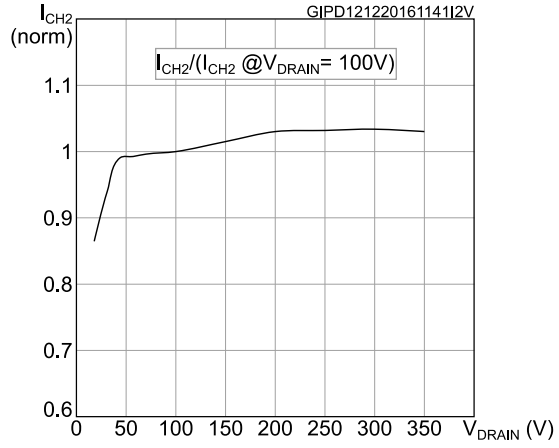


Figure 14. I_{CH3} vs T_J

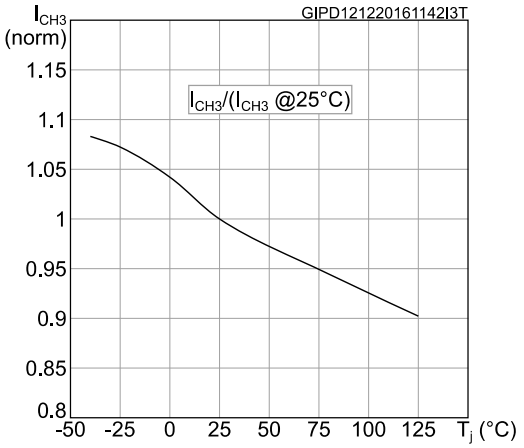


Figure 15. I_{CH3} vs V_{DRAIN}

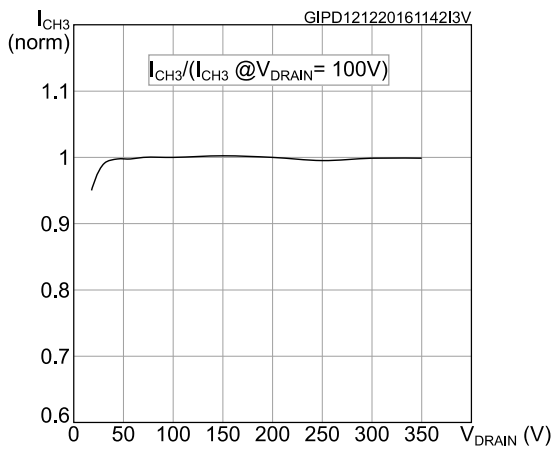


Figure 16. G_M vs T_J

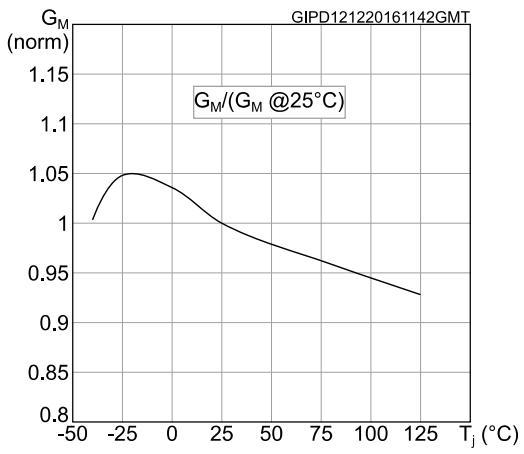


Figure 17. I_{COMP} vs T_J

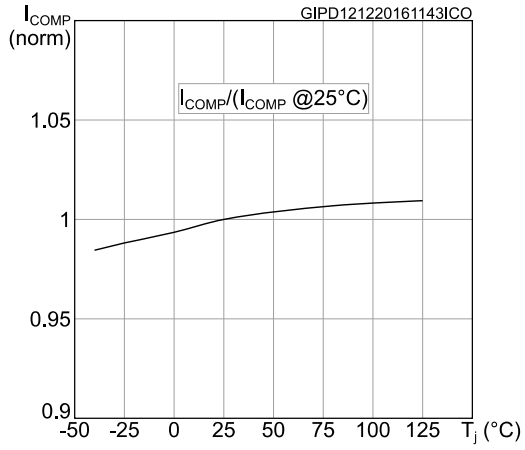


Figure 18. $R_{DS(on)}$ vs T_J

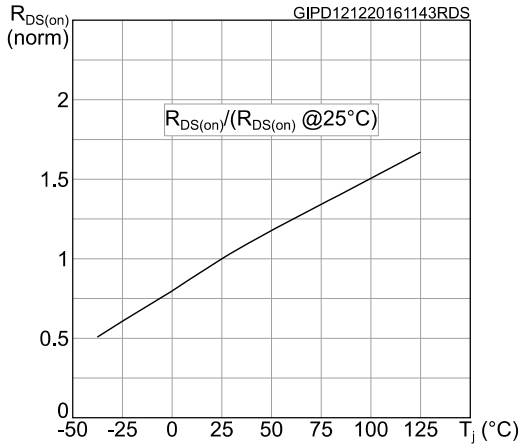


Figure 19. Static drain-source on-resistance

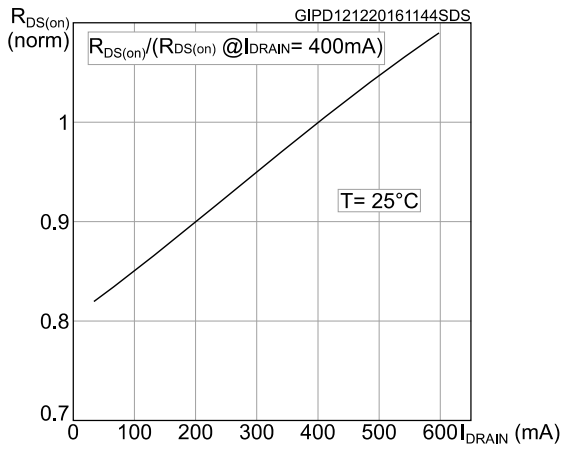


Figure 20. Power MOSFET capacitance variation vs VDS @ VGS=0, f=1MHz

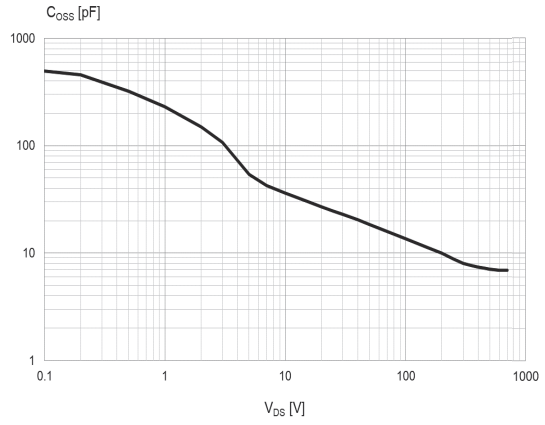


Figure 21. VBVDSS vs. TJ

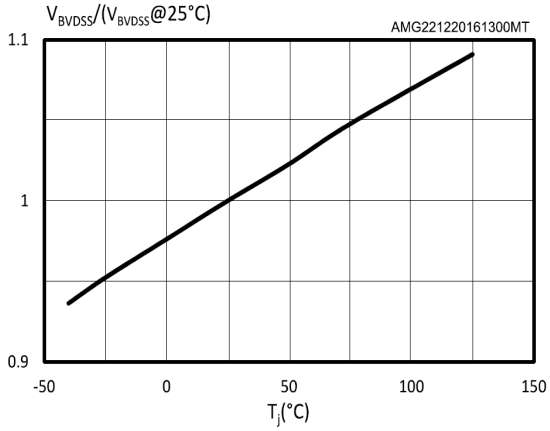


Figure 22. Output characteristic

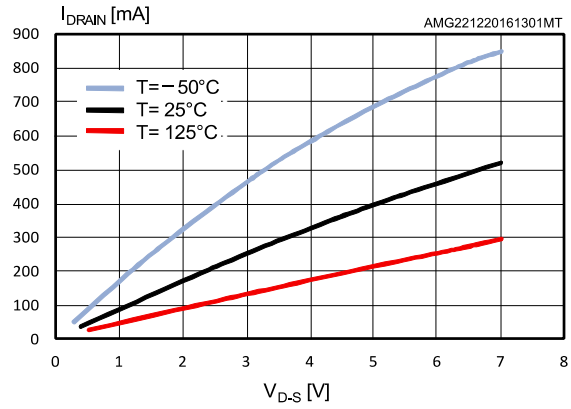
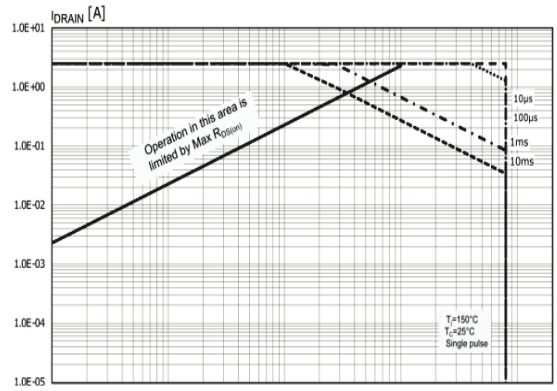
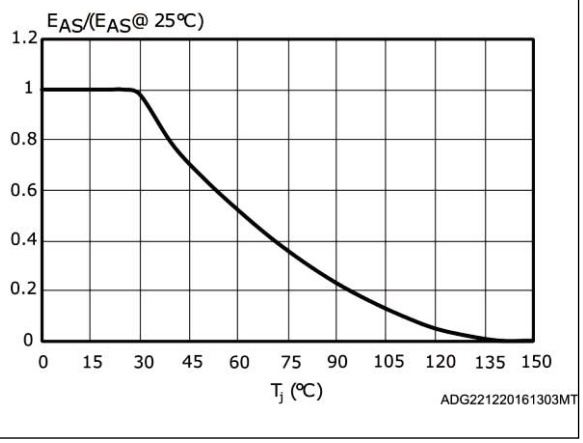


Figure 23. SOA SSOP10 package



* When mounted on a standard single side FR4 board with 50 mm² (0.077 sq in) of Cu (35 µm thick).

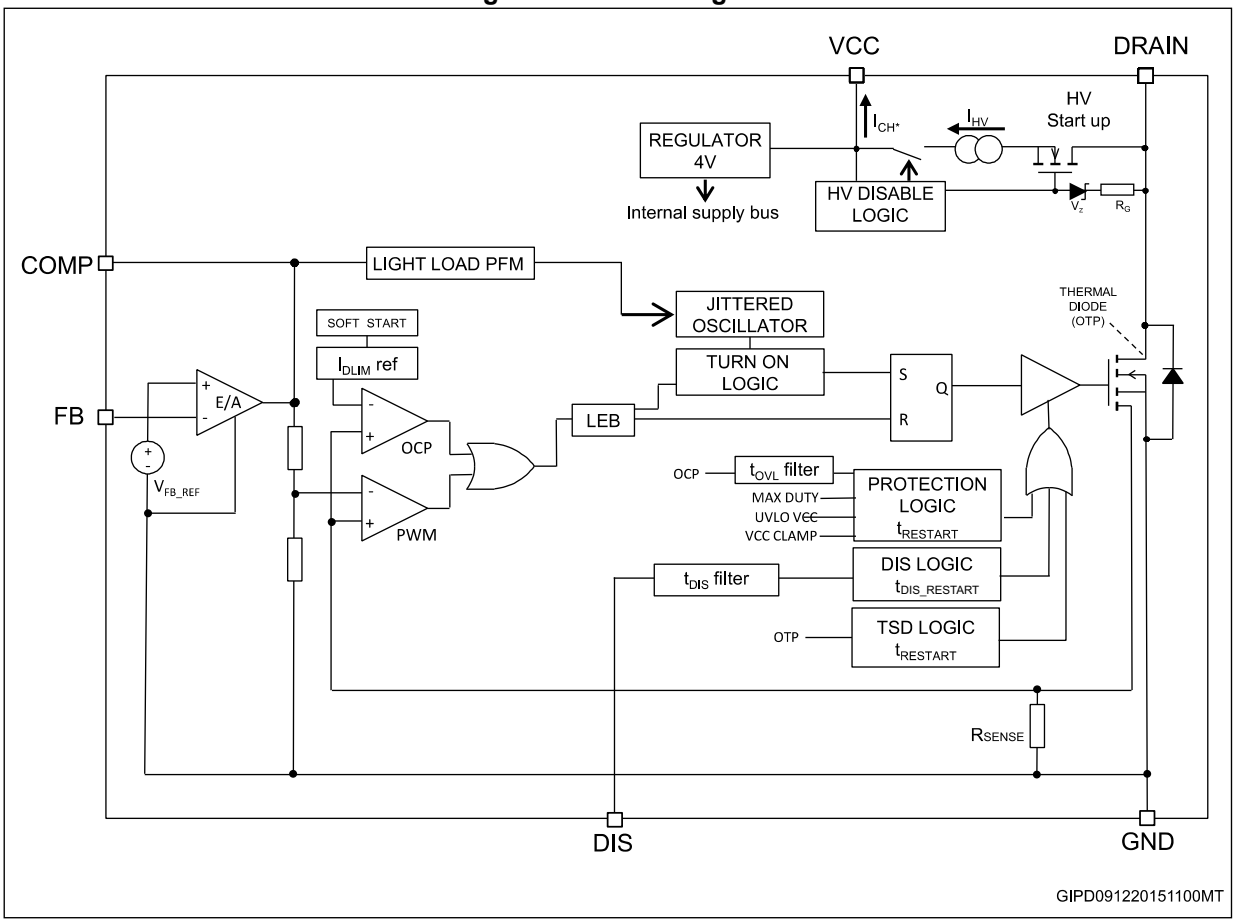
Figure 24. Maximum avalanche energy vs TJ



5 General description

5.1 Block diagram

Figure 25. Block diagram



5.2 Typical power capability

Table 8. Typical power

Vin: 230 V_{AC}		Vin: 85-265 V_{AC}	
Adapter(1)	**Open frame(2)**	**Adapter**	**Open frame**
10 W	12 W	6 W	7 W

1. Typical continuous power in non-ventilated enclosed adapter measured at 50 °C ambient.
2. Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heat-sinking.

5.3 Primary MOSFET

The primary switch is implemented with an avalanche-rugged N-channel MOSFET with minimum breakdown voltage 800 V, V_{BVDSS}, and maximum on-resistance of 20 Ω, $R_{DS(on)}$. The sense-FET is embedded and it allows a virtually lossless current sensing.

The MOSFET gate driver controls the gate current during both turn-on and turn-off in order to minimize EMI. Under UVLO conditions the embedded pull-down circuit holds the gate low in order to ensure that the MOSFET cannot be turned on accidentally.

5.4 High voltage startup

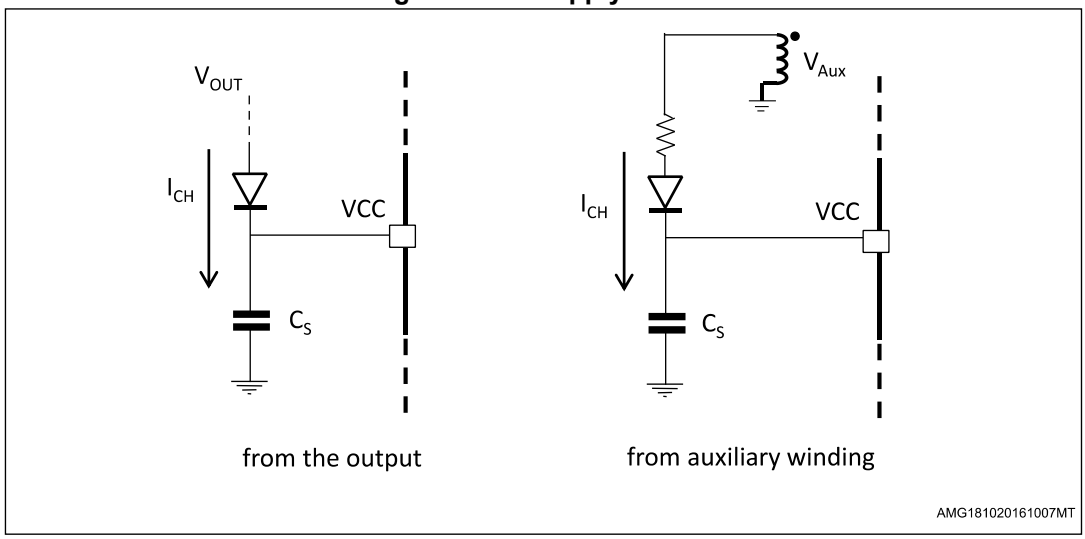
The embedded high voltage startup includes both the 800V-rated auxiliary N-channel power MOSFET, whose gate is biased through the resistor R_G, and the switchable HV current source, delivering the current I_{HV}. The major portion of I_{HV}, (I_{CH}), charges the capacitor connected to VCC. A minor portion is sunk by the controller block.

At startup, as the voltage across the DRAIN pin exceeds the V_{HV_START} threshold, the HV current source is turned on, charging linearly the C_S capacitor. At the very beginning of the startup, when Cs is fully discharged, the charging current is low, I_{CH1}, in order to avoid IC damaging in case V_{CC} is accidentally shorted to GND. As V_{CC} exceeds 1 V, I_{CH} is increased to I_{CH2} in order to speed up the charging of C_S.

As V_{CC} reaches the start-up threshold V_{CCon} the chip starts operating, the primary MOSFET is enabled to switch, the HV current source is disabled and the device is powered by the energy stored in the C_S capacitor.

In steady-state the IC can be supplied from the output (in case of non-isolated topologies) or through an auxiliary winding (in case of isolated topologies), as shown in *Figure 26*.

Figure 26. IC supply modes



In external supply the HV current source is always kept off by maintaining the V_{CC} above V_{CSon}. In this case the residual consumption is given by the power dissipated on R_G, calculated as follows:

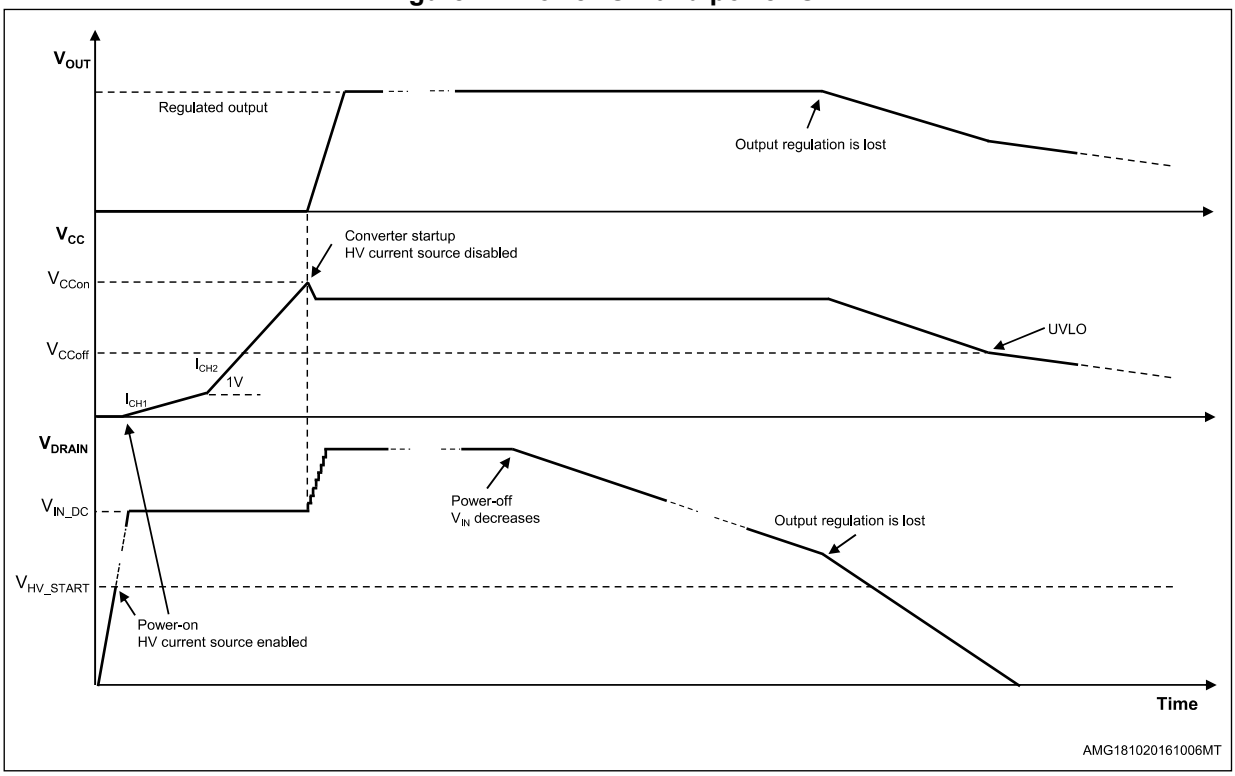
Equation 1

$$P = \frac{V^2_{INDC}}{R_G}$$

At the nominal input voltage, 230 V_{AC}, the typical consumption (R_G = 34 MΩ) is 3.2 mW and the worst-case consumption (R_G = 28 MΩ) is 3.9 mW.

When the IC is disconnected from the mains, or there is a mains interruption, for some time the converter keeps on working, powered by the energy stored in the input bulk capacitor. When it is discharged below a critical value, the converter is no longer able to keep the output voltage regulated. During the power down, when the DRAIN voltage becomes too low, the HV current source (I_{HV}) remains off and the IC is stopped as soon as the V_{CC} drops below the UVLO threshold, V_{CCoff}.

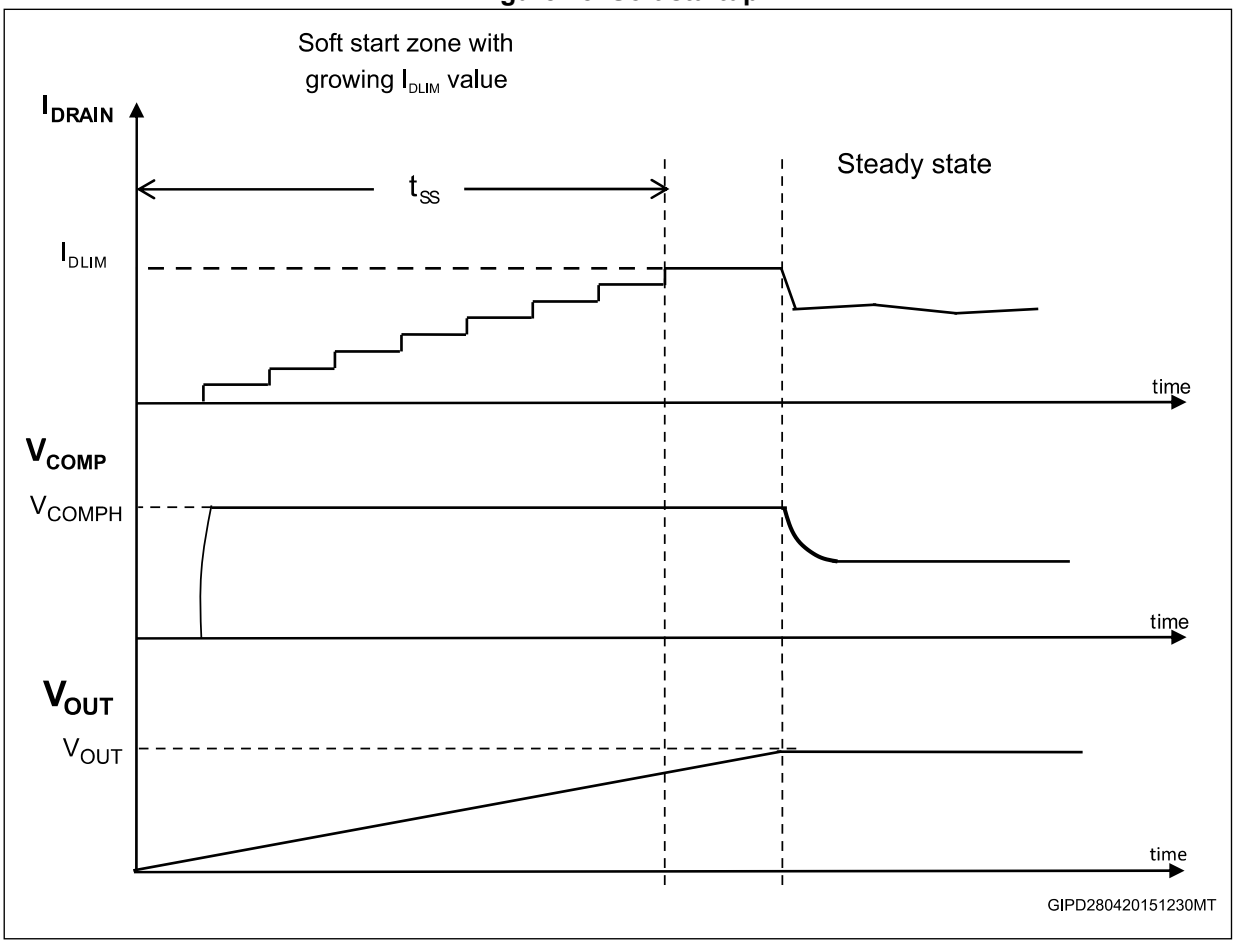
Figure 27. Power-ON and power-OFF



5.5 Soft-start

The internal soft-start function of the device progressively increases the cycle-by-cycle current limitation set point from zero up to I_{DLIM} in 8 steps. The soft-start time, t_{SS}, is internally set at 8 ms. This function is activated at any attempt of converter startup and at any restart after a fault event. The feature protects the system at startup, when the converter would run at its maximum drain current limitation because the output capacitor is fully discharged and behaves like a short-circuit.

Figure 28. Soft startup



5.6 Oscillator

The IC embeds a fixed frequency oscillator with jittering feature. The switching frequency is modulated by approximately ± 7% kHz F_{OSC} at 260 Hz rate. The purpose of the jittering is to get a spread-spectrum action that distributes the energy of each harmonic of the switching frequency over a number of frequency bands, having the same energy on the whole but smaller amplitudes. This helps to reduce the conducted emissions, especially when measured with the average detection method or, which is the same, to pass the EMI tests with an input filter of smaller size than that needed in absence of jittering feature.

Three options with different switching frequencies, F_{OSC}, are available: 30 (X type), 60 kHz (L type) and 120 kHz (H type).

5.7 Pulse-skipping

The IC embeds a pulse-skip circuit that operates in the following ways:

- Each time the DRAIN peak current exceeds I_{DLIM} level within t_{ON_MIN}, one switching cycle is skipped. The cycles can be skipped until the minimum switching frequency is reached, F_{OSC_MIN} (15 kHz).
- Each time the DRAIN peak current does not exceed I_{DLIM} within t_{ON_MIN}, one switching cycle is restored. The cycles can be restored until the nominal switching frequency is reached, F_{OSC} (30, 60 or 120 kHz).

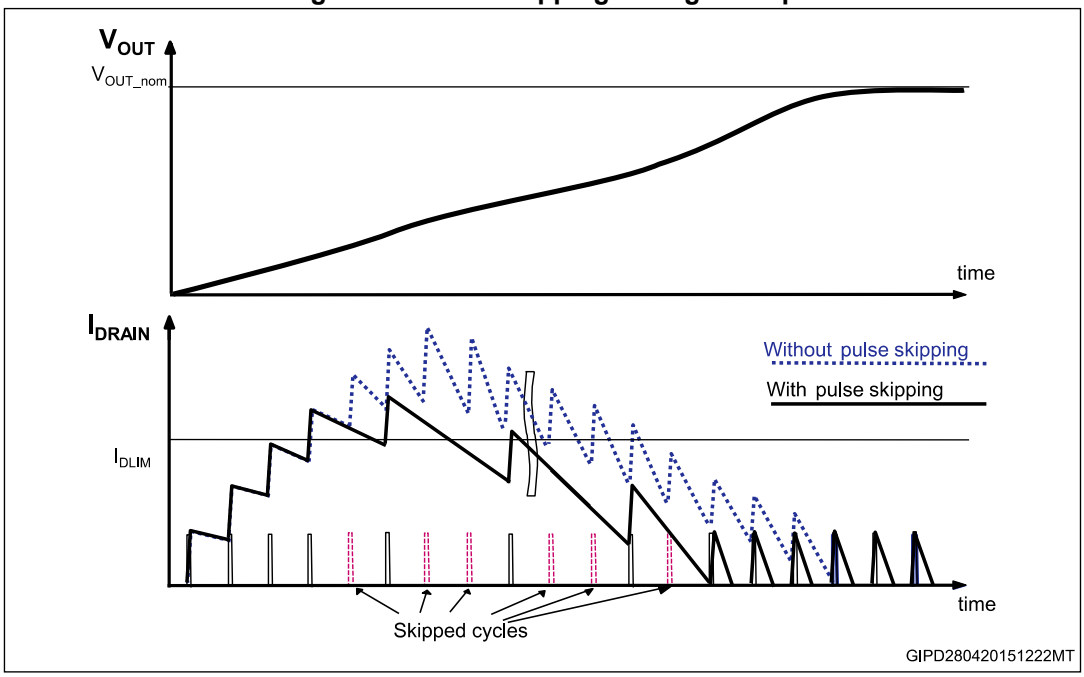
The protection is intended to avoid the so called “flux-runaway” condition often present at converter startup and due to the fact that the primary MOSFET, which is turned on by the internal oscillator, cannot be turned off before the minimum on-time.

During the on-time, the inductor is charged by the input voltage and if it cannot be discharged by the same amount during the off-time, in every switching cycle there is a net increase of the average inductor current, that can reach dangerously high values until the output capacitor is not charged enough to ensure the inductor discharge rate needed for the volt-second balance. This condition may happen at converter startup, because of the low output voltage.

In *Figure 29* the effect of pulse-skipping feature on the DRAIN peak current shape is shown (solid line), compared with the DRAIN peak current shape when pulse-skipping feature is not implemented (dashed line).

Providing more time for cycle-by-cycle inductor discharge when needed, this feature is effective by keeping low the maximum DRAIN peak current avoiding the flux-runaway condition.

Figure 29. Pulse-skipping during startup



5.8 Direct feedback

The IC embeds a transconductance type error amplifier (E/A) whose inverting input and output are FB and COMP, respectively. The internal reference voltage of the E/A is V_{FB_REF} (1.2 V typical value referred to GND). In non-isolated topologies, positive output voltages are tightly set through a simple voltage divider applied to the output voltage terminal, FB and GND.

The E/A output is scaled down and fed into the PWM comparator, where it is compared with the voltage across the sense resistor in series to the sense-FET, thus setting the cycle-by-cycle drain current limitation.

An R-C network connected across COMP (the output of the E/A) and GND pins is usually used to stabilize the overall control loop.

The FB is provided with an internal pull-up to prevent a wrong IC behavior when the pin is accidentally left floating.

The E/A is disabled if the FB voltage is lower than V_{FB_DIS} (200 mV, typ.).

5.9 Secondary feedback

When a secondary feedback is required, the internal E/A has to be disabled shorting FB to GND ($V_{FB} < V_{FB\_DIS}$). With this setting, COMP is internally connected to a pre-regulated voltage through the pull-up resistor $R_{COMP(DYN)}$ and the voltage across COMP is set by the current sunk.

This allows the output voltage value to be set through an external error amplifier (TL431 or similar) placed on the secondary side, whose error signal is used to set the DRAIN peak current setpoint corresponding to the output power demand. If isolation is required, the error signal must be transferred through an optocoupler, with the phototransistor collector connected across COMP and GND.

5.10 Pulse frequency modulation

If the output load is decreased, the feedback loop reacts lowering the V_{COMP} voltage, which reduces the DRAIN peak current setpoint, down to the minimum value of I_{DLIM_PFM} when the V_{COMPL} threshold is reached.

If the load is furtherly decreased, the DRAIN peak current value is maintained at I_{DLIM_PFM} and some PWM cycles are skipped. This kind of operation is referred to as “pulse frequency modulation” (PFM), the number of the skipped cycles depends on the balance between the output power demand and the power transferred from the input. The result is an equivalent switching frequency which can go down to some hundreds Hz, thus reducing all the frequency-related losses.

This kind of operation, together with the extremely low IC quiescent current, allows very low input power consumption in no-load and light load, while the low DRAIN peak current value, I_{DLIM_PFM}, prevents any audible noise which could arise from low switching frequency values. When the load is increased, V_{COMP} increases and PFM is exited. V_{COMP} reaches its maximum at V_{COMPH} and corresponding to that value, the DRAIN current limitation (I_{DLIM}) is reached.

5.11 Overload protection

To manage the overload condition, the IC embeds the following main blocks: the OCP comparator to turn off the power MOSFET when the drain current reaches its limit (I_{DLIM}) , the up and down OCP counter to define the turn-off delay time in case of continuous overload (t_{OVL} = 50 ms typ.) and the timer to define the restart time after protection tripping ($t_{RESTART}$ = 1 s typ.).

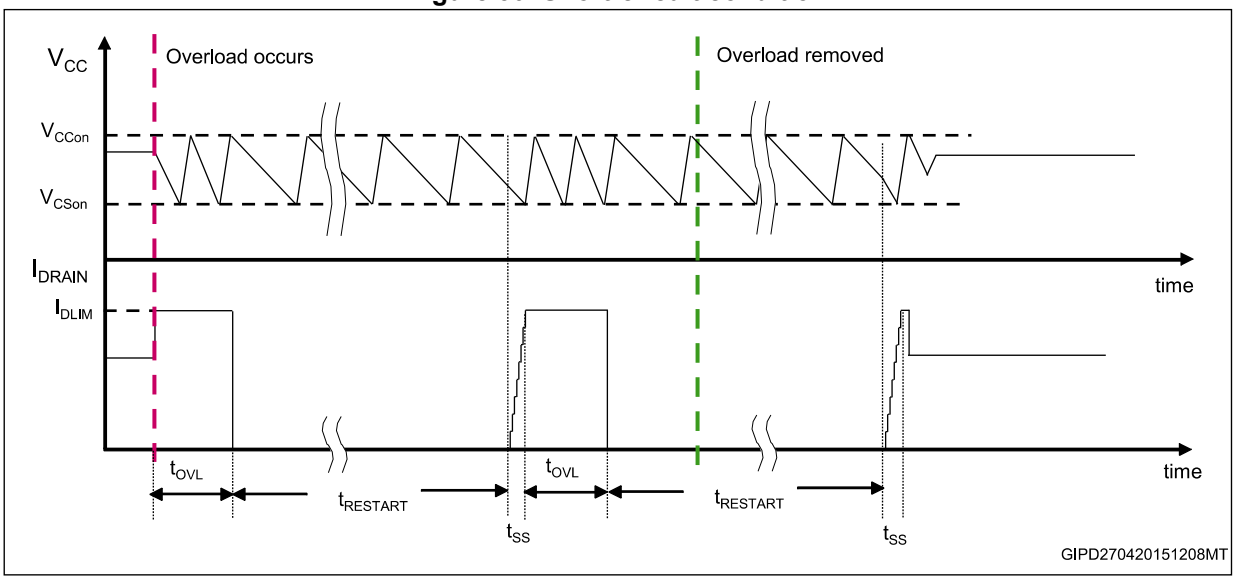
In case of short-circuit or overload, the control level on the inverting input of the PWM comparator is greater than the reference level fed into the inverting input of the OCP comparator. As a result, the cycle-by-cycle turn-off of the power switch is triggered by the OCP comparator instead of PWM comparator. Every cycle where this condition is met, the OCP counter is incremented. If the fault condition lasts longer than t_{OVL} (corresponding to the counter end-of-count), the protection is tripped, the PWM is disabled for $t_{RESTART}$, then it resumes switching with soft-start and, if the fault is still present, it is disabled again after t_{OVL}. If the converter is definitively operated at F_{OSC_MIN}, (see *Section 5.7: Pulse-skipping*), the IC is turned off after the time t_{OVL_MAX} (100 ms or 200 ms or 400 ms typ., depending on F_{OSC}) and then automatically restarted with soft-start phase, after $t_{RESTART}$.

The OLP management prevents IC from operating indefinitely at I_{DLIM} and the low repetition rate of the restart attempts of the converter avoids IC overheating in case of repeated fault events.

After the fault removal, the IC resumes working normally. If the fault is removed earlier than the protection tripping (before t_{OVL}), the t_{OVL}-counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped. If the fault is removed during $t_{RESTART}$, the IC waits for the $t_{RESTART}$ period has elapsed before resuming switching.

In fault condition the V_{CC} ranges between V_{CSon} and V_{CCon} levels, due to the periodical activation of the HV current source recharging the V_{CC} capacitor.

Figure 30. Short-circuit condition



5.12 Max. duty cycle counter protection

The IC embeds a max. duty cycle counter, which disables the PWM if the MOSFET is turned off by max. duty cycle (70% min., 80% max.) for ten consecutive switching cycles. After protection tripping, the PWM is stopped for $t_{RESTART}$ and then activated again with soft- start phase until the fault condition is removed.

In some cases (i.e. breaking of the loop) even if V_{COMP} is saturated high, the OLP cannot be triggered because at every switching cycle the PWM is turned off by maximum duty cycle before than DRAIN peak current reaches the I_{DLIM} setpoint. As a result, the output voltage V_{OUT} can increase without control by keeping a value much higher than the nominal one with the risk for the output capacitor, the output diode and the IC itself. The max. duty cycle counter protection avoids this kind of failures.

5.13 VCC clamp protection

This protection can occur when the IC is supplied by auxiliary winding or diode from the output voltage, when an output overvoltage produces an increase of V_{CC}.

If VCC reaches the clamp level $V_{CCclamp}$ (30 V, min. referred to GND) the current injected into the pin is monitored and if it exceeds the internal threshold I_{clamp_max} (30 mA, typ.) for more than t_{clamp_max} (500 µs, typ.), the PWM is disabled for $t_{RESTART}$ (1 s, typ.) and then activated again in soft-start phase. The protection is disabled during the soft-start time.

5.14 Disable function

When the voltage across the DIS pin exceeds the internal threshold V_{DIS_th} (1.2 V typ.), a time filter t_{DIS} (1 msec, typ.) is activated.

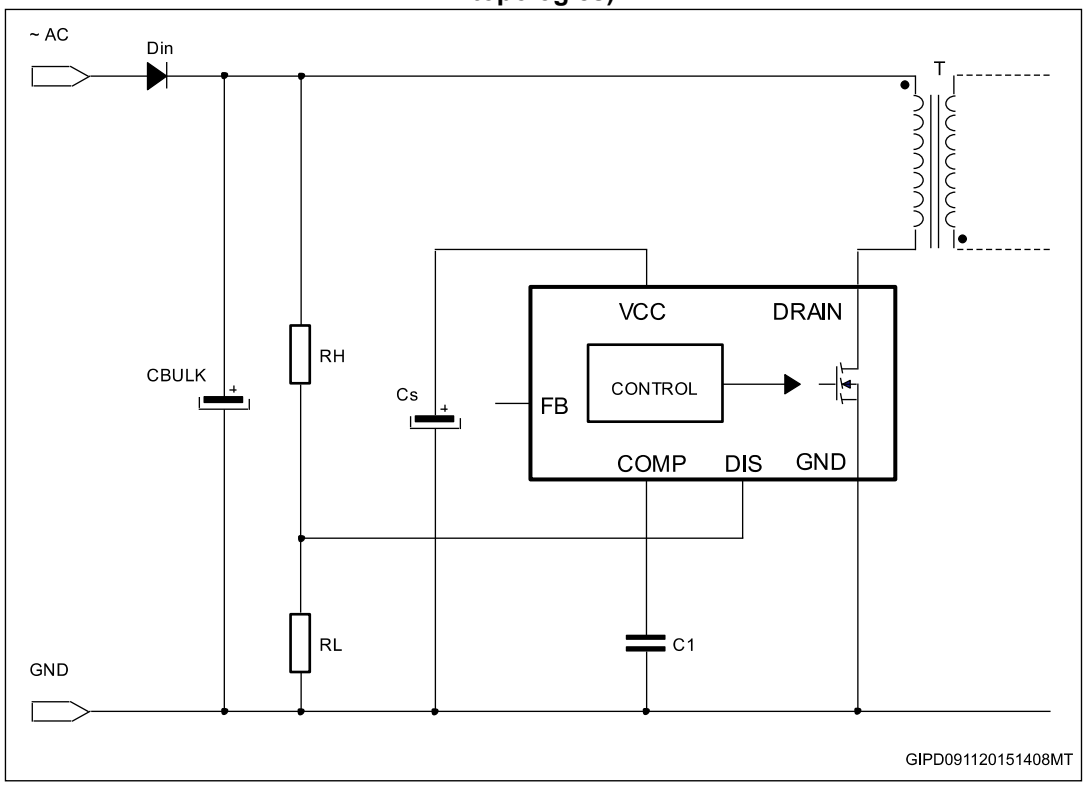
If, at the end of t_{DIS}, the condition is no more met, the occurrence of a temporary disturbance is assumed and the IC continues to work normally; otherwise, a fault condition is recognized and the IC is disabled in auto-restart for $t_{DIS\_RESTART}$ (500 msec, typ.).

When V_{DIS} falls below V_{DIS_th}, the IC completes the current $t_{DIS\_RESTART}$, then resumes normal operation.

During the fault, the VCC voltage is maintained between V_{CCSON} and V_{CCoN} through the HV current source periodical activation.

A simple input overvoltage protection can be realized by connecting a voltage divider between the DIS pin and the rectified mains, as shown in *Figure 31*.

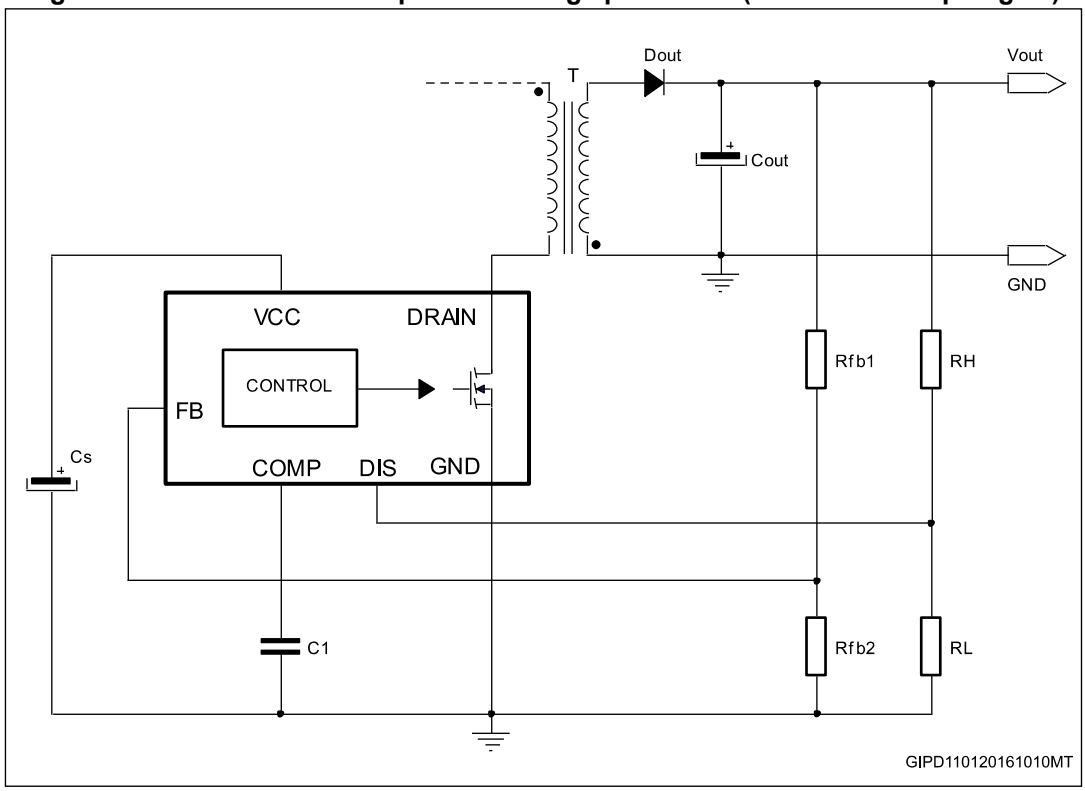
Figure 31. Connection for input overvoltage protection (isolated or non-isolated topologies)



In case of non-isolated topologies, with the same principle an output overvoltage protection can be implemented, as shown in *Figure 32*.

If the Disable function is not required, DIS pin must be soldered to GND, which excludes the function.

Figure 32. Connection for output overvoltage protection (non-isolated topologies)



If V_{OVP} is the desired input/output overvoltage threshold, the resistors R_H and R_L of the voltage divider are to be selected according to the following formula:

Equation 2

$$R_H = (V_{OVP} / V_{DIS\_th} - 1) \times R_L$$

The power dissipation associated to the DIS network is:

Equation 3

$$P_{DIS}(V_{IN}) = P_{RH} + P_{RL} = \frac{(V_{IN} - V_{DIS})^2}{R_H} + \frac{V_{DIS}^2}{R_L}$$

in case of connection for the input overvoltage detection and

Equation 4

$$P_{DIS}(V_{OUT}) = P_{RH} + P_{RL} = \frac{(V_{OUT} - V_{DIS})^2}{R_H} + \frac{V_{DIS}^2}{R_L}$$

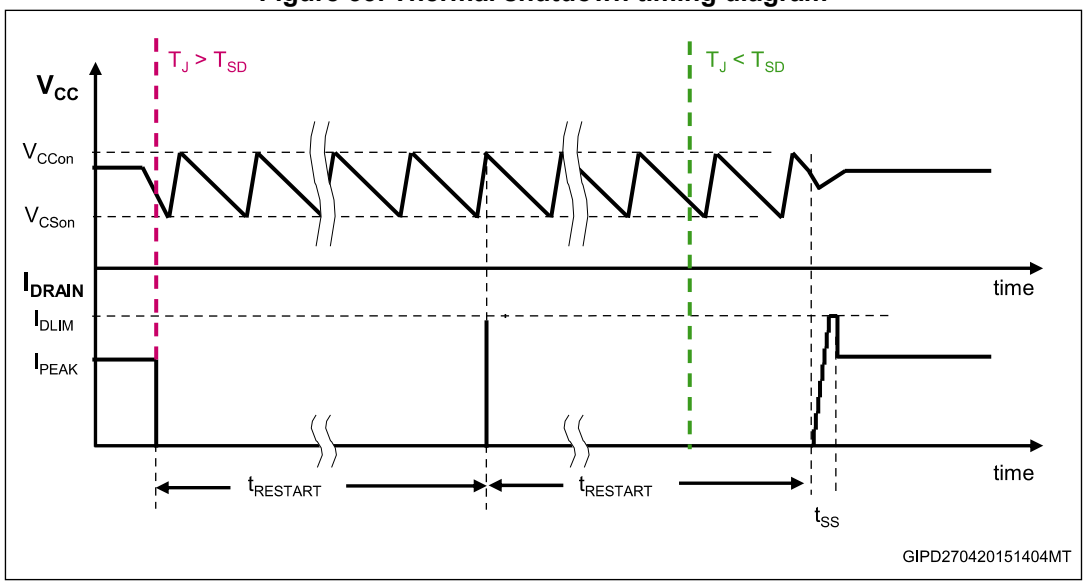
in case of connection for the output overvoltage detection.

5.15 Thermal shutdown

If the junction temperature becomes higher than the internal threshold T_{SD} (160 °C, typ.), the PWM is disabled. After $t_{RESTART}$ time, a single switching cycle is performed, during which the temperature sensor embedded in the power MOSFET section is checked. If a junction temperature above T_{SD} is still measured, the PWM is maintained disabled for $t_{RESTART}$ time, otherwise it resumes switching with soft-start phase.

During $t_{RESTART}$ V_{CC} is maintained between V_{CSon} and V_{CCon} levels by the HV current source periodical activation. Such a behavior is summarized in below figure:

Figure 33. Thermal shutdown timing diagram



5.16 Auto-restart

When a fault occurs, the PWM is disabled in auto-restart until the fault is removed.

This means that:

1. PWM stops switching for a restart time, namely:

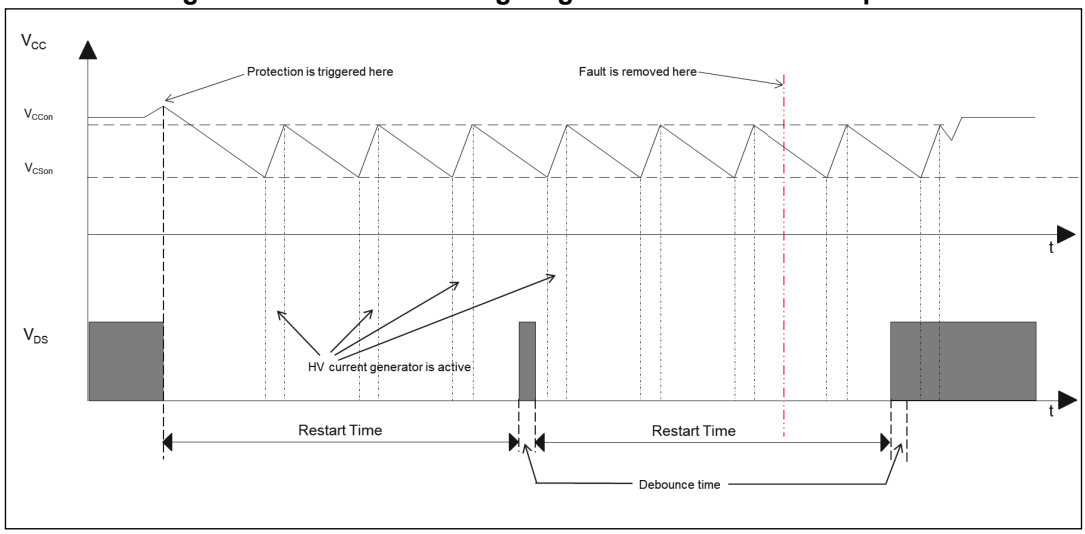
- $t_{RESTART}$ (1 sec, typ.), in case the fault is one of the following: overload/short-circuit, max. duty cycle counter, V_{CC} clamp, overtemperature.
- $t_{DIS\_RESTART}$ (0.5 sec, typ.), in case the fault is triggered at the DIS pin (input/output overvoltage).

2. At the end of restart time:
   – if the fault is still present, the protection is tripped in the same way after a debounce time (see *Figure 34*), namely:

- $t_{SS} + t_{OVL}$ (8 + 50msec, typ.) in case the fault is overload/short-circuit;
- t_{clamp_max} (0.5 msec, typ.) in case the fault is V_{CC} clamp;
- t_{DIS} (1 msec, typ) in case the fault is triggered at the DIS pin (input/output overvoltage);
- 10 switching cycles in case the fault is max. duty cycle counter;
- 1 switching cycle in case the fault is overtemperature;
  – if the fault is no longer present, normal operation is restored, as shown in *Figure 34*.

3. During restart time, the HV generator is activated periodically, maintaining the VCC pin voltage between V_{CSon} and V_{CCon}.

Figure 34. Protection timing diagram with auto-restart option



6 Application information

6.1 Typical schematics

Figure 35. Flyback converter (non-isolated)

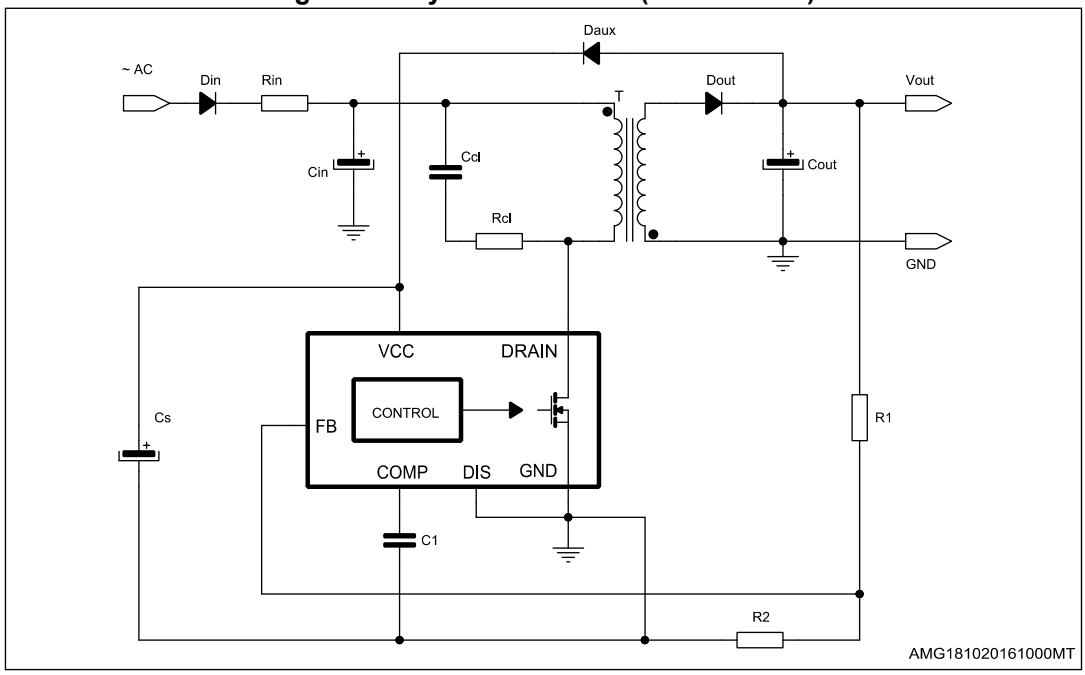


Figure 36. Flyback converter with line OVP (non-isolated)

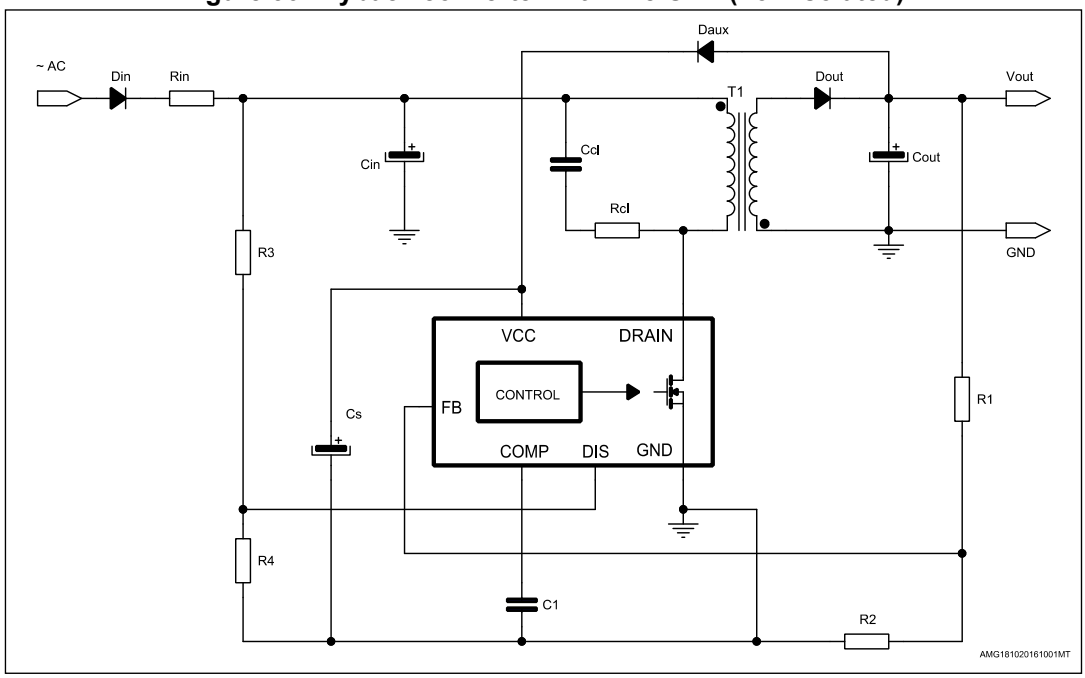


Figure 37. Flyback converter (isolated)

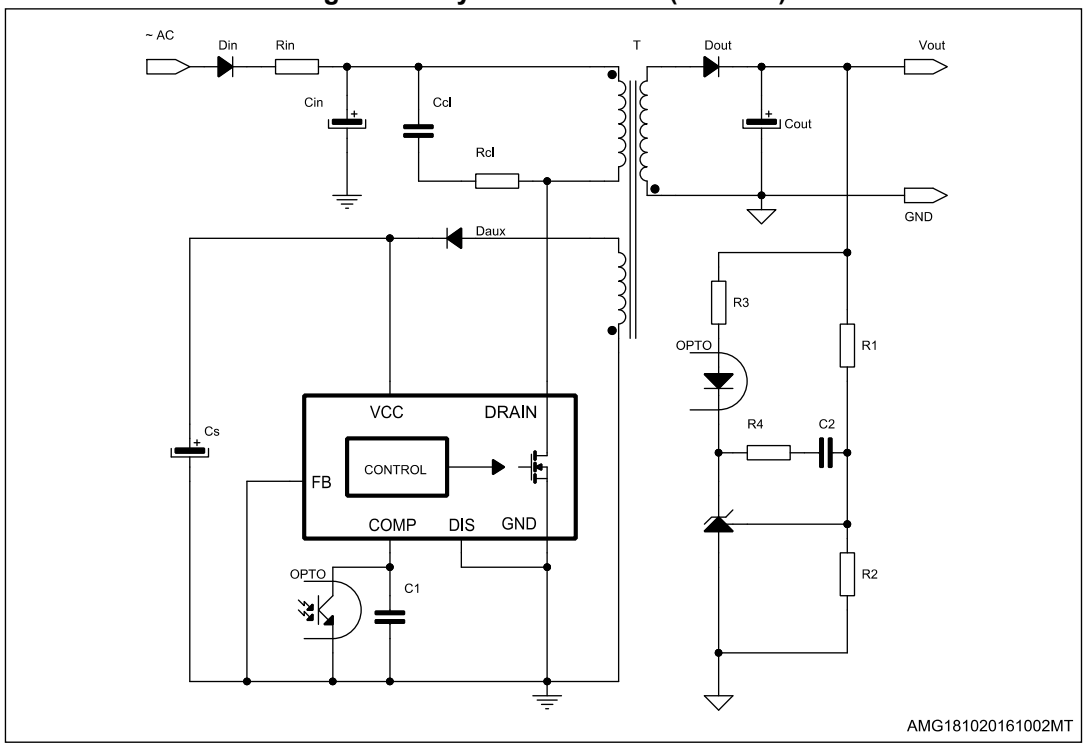


Figure 38. Primary side regulation isolated flyback converter

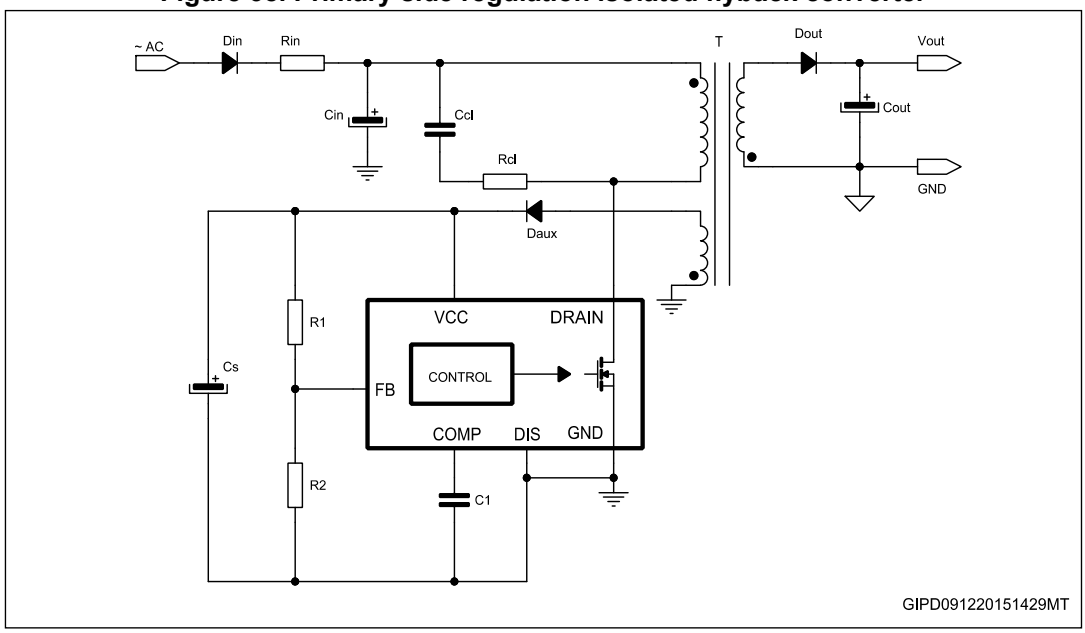


Figure 39. Buck converter (positive output)

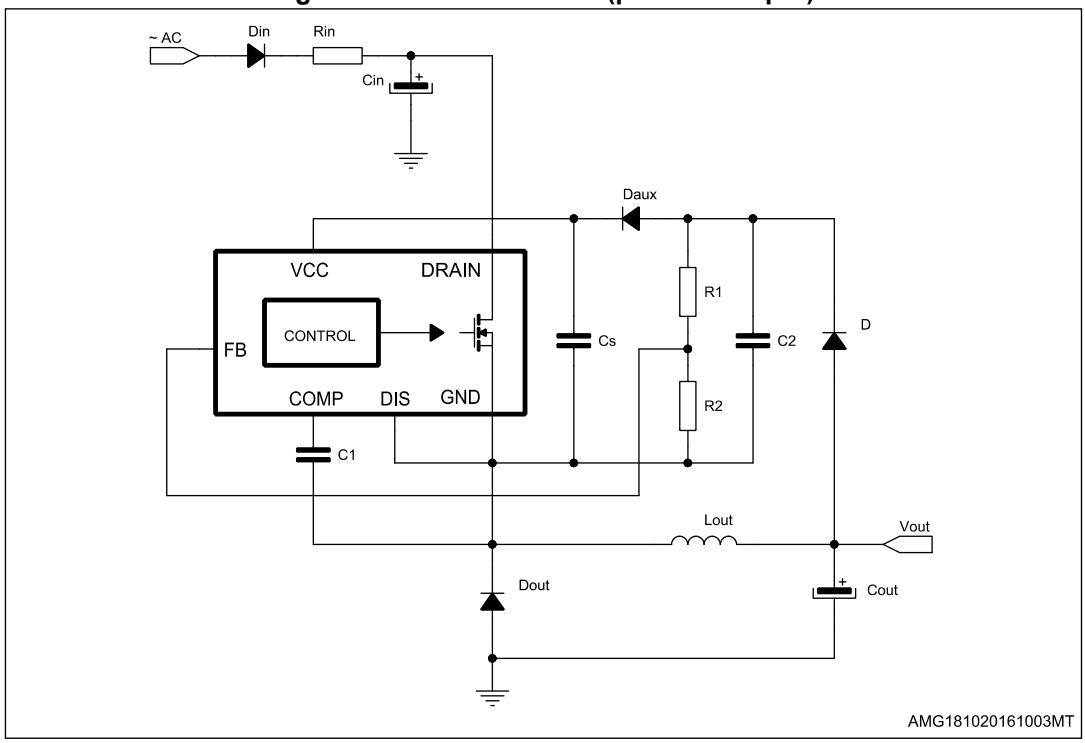
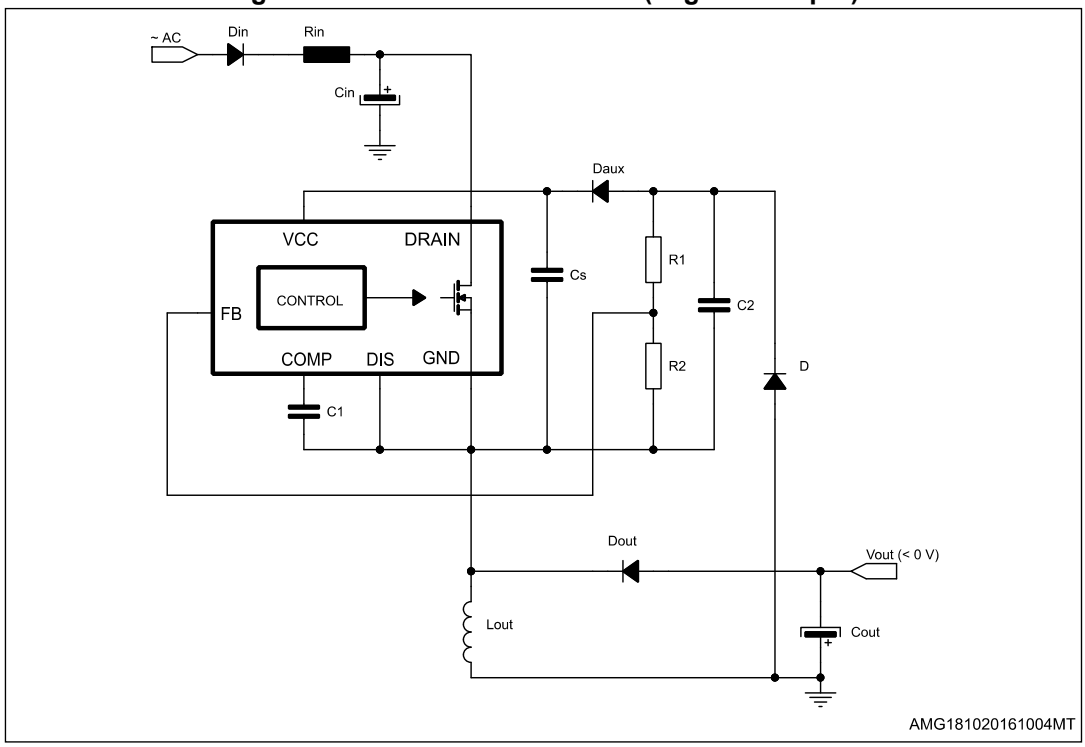


Figure 40. Buck-boost converter (negative output)



6.2 Energy saving performance

The device allows designing applications to be compliant with the most stringent energy saving regulations. In order to show the typical performance is achievable, the active mode average efficiency and the efficiency at 10% of the rated output power of a 5 V/1.6 A non-isolated flyback and 5 V/360 mA buck converters adopting VIPer11, have been measured and are reported in *Table 9*. In addition, no-load and light load consumptions are shown from *Figure 41* to *Figure 44*.

Table 9. Power supply efficiency, V_{OUT} = 5 V

Parameter	VIN	10 % output load efficiency [%]	Active mode average efficiency [%]	Pin at no-load [mW]
Flyback non iso. 5 V/1.6 A	115 V_{AC}	78.3	78.5	3.9
	230 V_{AC}	71.4	79.4	8.2
Buck 5 V/360 mA(1)	115 V_{AC}	73.9	71.6	12.1
	230 V_{AC}	69.1	69.8	16.2

1. 5 mW bleeder connected at the output.

Figure 41. P_{IN} versus V_{IN} in no-load non isolated flyback converter (5 V/1.6 A)

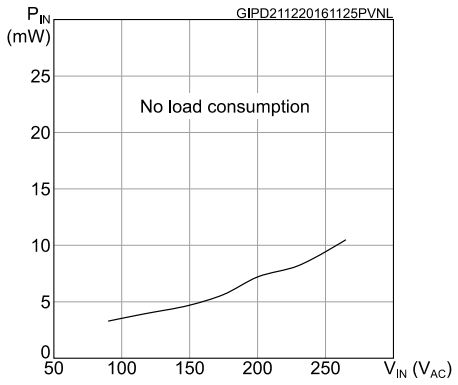


Figure 42. P_{IN} versus V_{IN} in light load non isolated flyback converter (5 V/1.6 A)

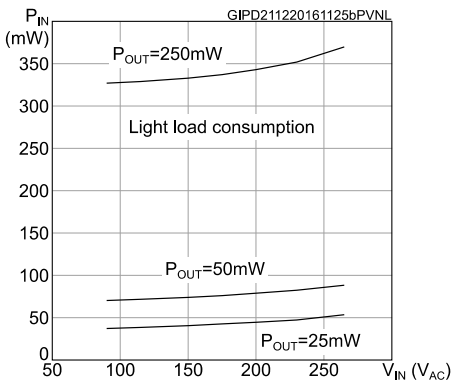


Figure 43. P_{IN} versus V_{IN} in no-load non isolated buck converter (5 V/360 mA)

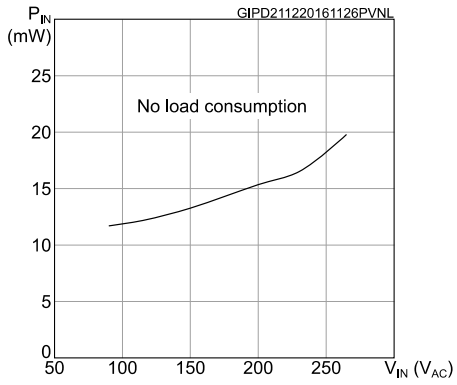
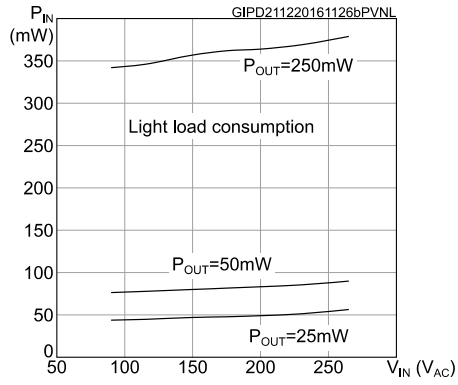


Figure 44. P_{IN} versus V_{IN} in light load non isolated buck converter (5 V/360 mA)



6.3 Layout guidelines and design recommendations

A proper printed circuit board layout ensures the correct operation of any switch-mode converter and this is true for the VIPer as well. The main reasons to have a proper PCB layout are:

- Providing clean signals to the IC, ensuring good immunity against external and switching noises.
- Reducing the electromagnetic interferences, both radiated and conducted, to pass the EMC tests more easily.

If the VIPer is used to design a SMPS, the following basic rules should be considered:

- **Separating signal from power tracks.** Generally, traces carrying signal currents should run far from others carrying pulsed currents or with fast swinging voltages. Signal ground traces should be connected to the IC signal ground, GND, using a single “star point”, placed close to the IC. Power ground traces should be connected to the IC power ground, GND. The compensation network should be connected to the COMP, maintaining the trace to GND as short as possible. In case of two-layer PCB, it is a good practice to route signal traces on one PCB side and power traces on the other side.
- **Filtering sensitive pins.** Some crucial points of the circuit need or may need filtering. A small high-frequency bypass capacitor to GND might be useful to get a clean bias voltage for the signal part of the IC and protect the IC itself during EFT/ESD tests. A low ESL ceramic capacitor (a few hundreds pF up to 0.1 μF) should be connected across VCC and GND, placed as close as possible to the IC. With flyback topologies, when the auxiliary winding is used, it is suggested to connect the VCC capacitor on the auxiliary return and then to the main GND using a single track.
- **Keeping power loops as confined as possible.** The area circumscribed by current loops where high pulsed current flow should be minimized to reduce its parasitic self-inductance and the radiated electromagnetic field. As a consequence, the electromagnetic interferences produced by the power supply during the switching are highly reduced. In a flyback converter the most critical loops are: the one including the input bulk capacitor, the power switch, the power transformer, the one including the snubber, the one including the secondary winding, the output rectifier and the output capacitor. In a buck converter the most critical loop is the one including the input bulk capacitor, the power switch, the power inductor, the output capacitor and the free-wheeling diode.
- **Reducing line lengths.** Any wire acts as an antenna. With the very short rise times exhibited by EFT pulses, any antenna can receive high voltage spikes. By reducing line lengths, the level of received radiated energy is reduced, and the resulting spikes from electrostatic discharges are lower. This also keeps both resistive and inductive effects to a minimum. In particular, all traces carrying high currents, especially if pulsed (tracks of the power loops) should be as short and wide as possible.
- **Optimizing track routing.** As levels of pickup from static discharges are likely greater near the edges of the board, it is wise to keep any sensitive lines away from these areas. Input and output lines often need to reach the PCB edge at some stage, but they can be routed away from the edge as soon as possible where applicable. Since vias are to be considered inductive elements, it is recommended to minimize their number in the signal path and avoid them in the power path.
- **Improving thermal dissipation.** An adequate copper area has to be provided under the DRAIN pins as heatsink, while it is not recommended to place large copper areas on the GND.

Figure 45. Recommended routing for flyback converter

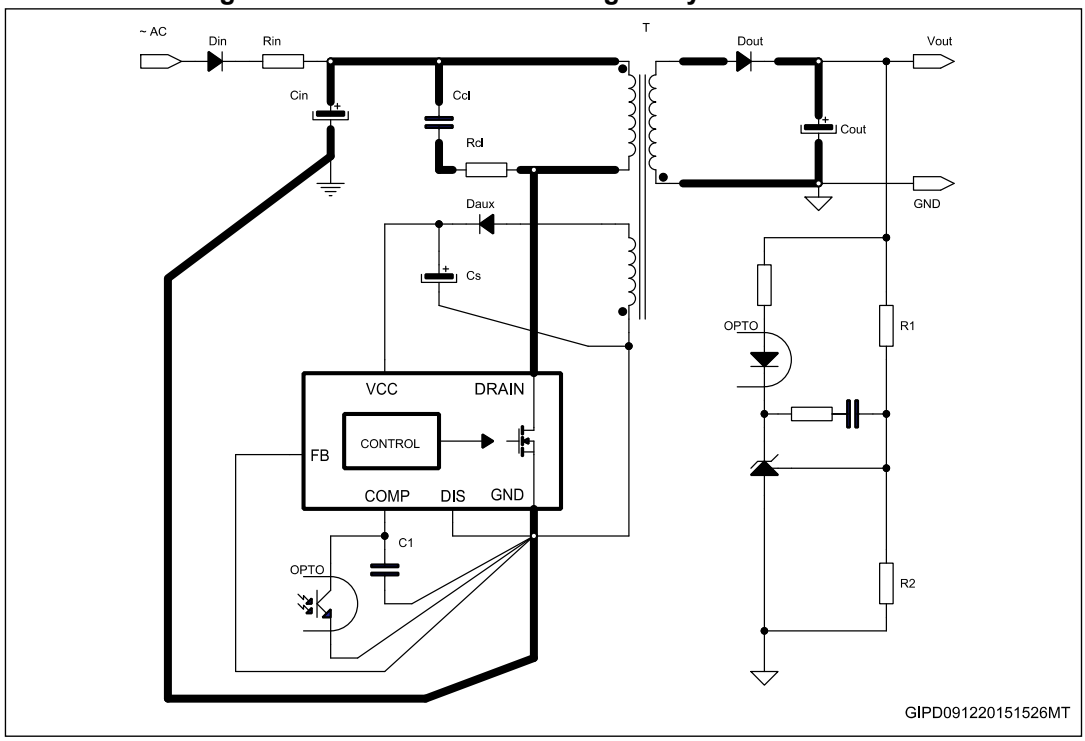
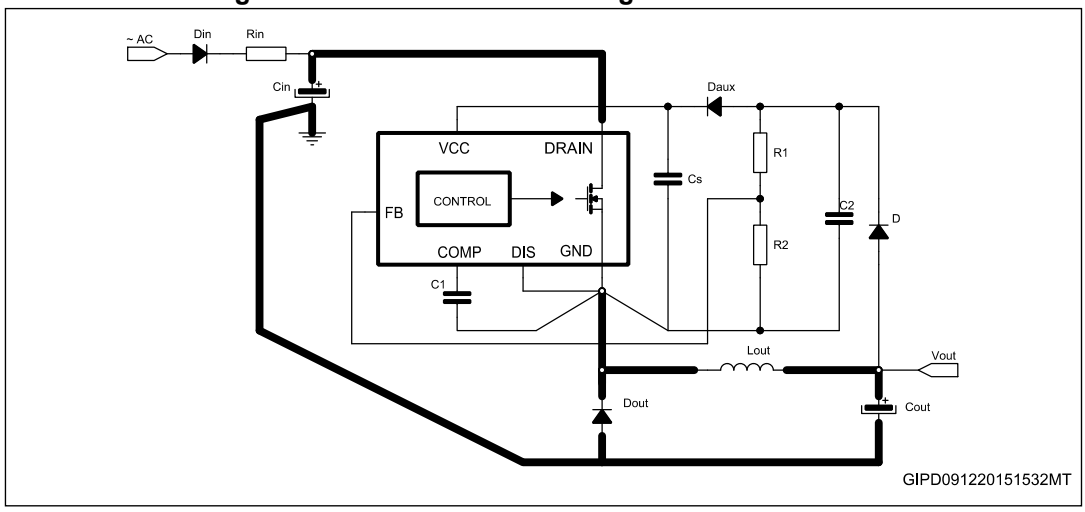


Figure 46. Recommended routing for buck converter



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 SSOP10 package information

Figure 47. SSOP10 package outline

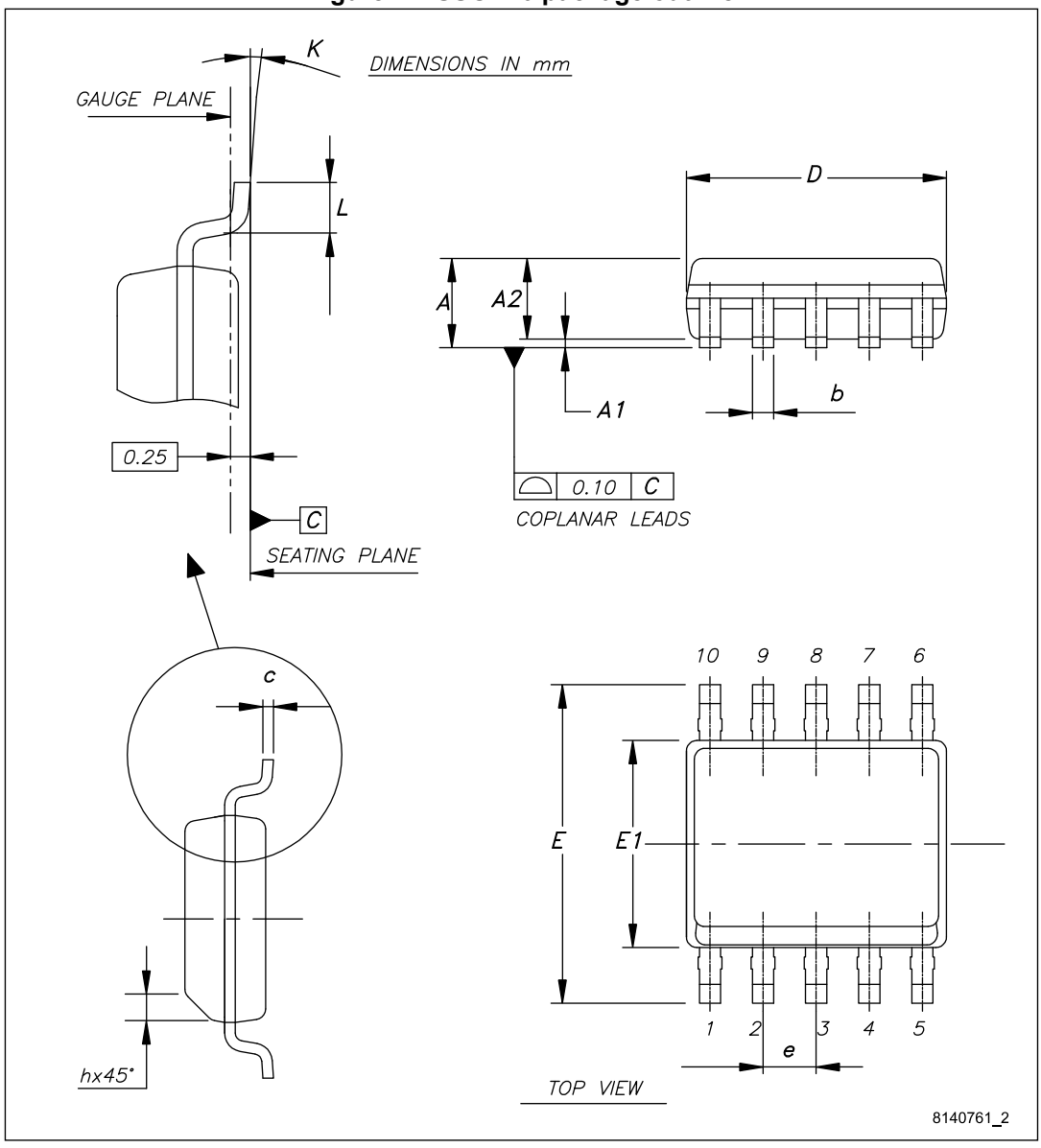
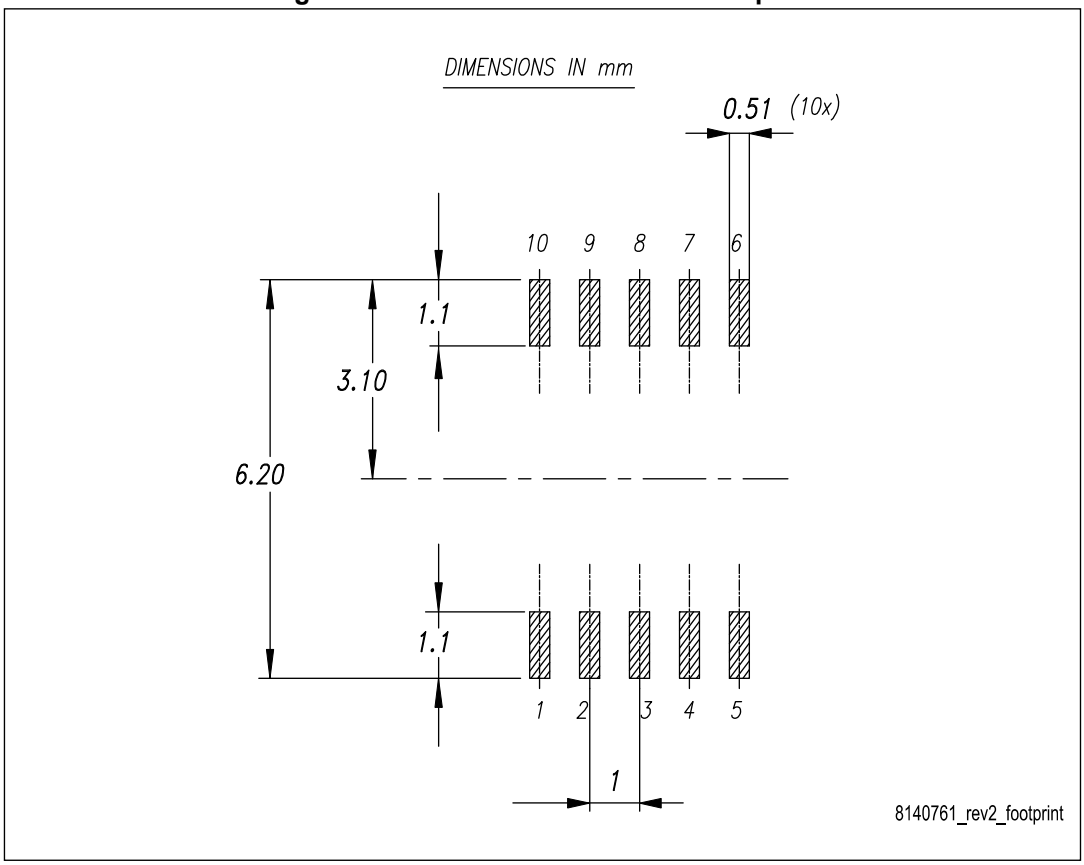


Table 10. SSOP10 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.17	-	0.25
D	4.80	4.90	5
E	5.80	6	6.20
E1	3.80	3.90	4
e	-	1	-
h	0.25	-	0.50
L	0.40	-	0.90
K	0°	-	8°

Figure 48. SSOP10 recommended footprint



8 Ordering information

Table 11. Order code

Order code	I_{DLIM} (OCP)	F_{OSC} ± jitter	Package
VIPER113XSTR	**3**70 mA	30 kHz ± 7%	SSOP10 tape and reel
VIPER114XSTR	**4**80 mA		
VIPER115XSTR	**5**90 mA		
VIPER113LSTR	**3**70 mA	60 kHz ± 7%	
VIPER114LSTR	**4**80 mA		
VIPER115LSTR	**5**90 mA		
VIPER114HSTR	**4**80 mA	120 kHz ± 7%	
VIPER115HSTR	**5**90 mA		

9 Revision history

Table 12. Document revision history

Date	Revision	Changes
11-Apr-2018	1	Initial release.
19-Apr-2018	2	Document status changed from preliminary to production data.
14-Dec-2018	3	Updated *Table 7*, amended *Section 5.16*.
02-Sept-2019	4	Amended the Features on page 1, Updated Tables *3*, *6*, *7*, and *11*. Amended *Table 1*, amended Figures *25*, *29*, *30*, *34*. Minor changes in sections *5.3*; *5.4*; *5.5*; *5.6*; *5.7*; *5.8*. Amended sections *5.11*; *5.14*; *5.15*.
07-Apr-2020	5	Update to a value in *Table 2*.

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9