

#### **General Description**

The MAX16016/MAX16020/MAX16021 supervisory circuits monitor power supplies, provide battery-backup control, and chip-enable (CE) gating to write protect memory in microprocessor (µP)-based systems. These low-power devices improve system reliability by providing several supervisory functions in a small, single integrated

The MAX16016/MAX16020/MAX16021 perform four basic system functions:

- 1) Provide a µP reset output during VCC supply powerup, power-down, and brownout conditions.
- 2) Control VCC to battery-backup switching internally to maintain data or low-power operation for memories, real-time clocks (RTCs), and other digital logic when the main power is removed.
- 3) Provide memory write protection through internal chip-enable gating during brownout.
- 4) Provide a combination of additional supervisory functions listed in the Features section.

The MAX16016/MAX16020/MAX16021 operate from a 1.53V to 5.5V supply voltage and offer fixed reset thresholds for monitoring 5V, 3.3V, 3V, 2.5V, and 1.8V systems. Each device is available with either a pushpull or open-drain reset output.

The MAX16016/MAX16020/MAX16021 are available in small TDFN/TQFN packages and are fully specified for an operating temperature range of -40°C to +85°C.

### **Applications**

Main/Backup Power for RTCs, CMOS Memories

Industrial Control

**GPS Systems** 

Set-Top Boxes

Point-of-Sale Equipment

Portable/Battery Equipment

#### **Features**

- System Monitoring for 5V, 3.3V, 3V, 2.5V, or 1.8V **Power-Supply Voltages**
- ♦ 1.53V to 5.5V Operating Voltage Range
- Low 1.2µA Supply Current (0.25µA in Battery-Backup Mode)
- ♦ 145ms (min) Reset Timeout Period
- ♦ Battery Freshness Seal
- On-Board Gating of CE Signals, 1.5ns Propagation Delay (MAX16020/MAX16021)
- **Debounced Manual Reset Input**
- Watchdog Timer, 1.2s (typ) Timeout
- Power-Fail Comparator and Low-Line Indicator for **Monitoring Voltages Down to 0.6V**
- Battery-On, Battery-OK, and Battery Test **Indicators**
- ♦ Small 10-Pin TDFN or 16-Pin TQFN Packages
- ◆ UL®-Certified to Conform to IEC 60950-1

#### **Ordering Information**

PART	TEMP RANGE	PIN-PACKAGE
MAX16016_TB_+T	-40°C to +85°C	10 TDFN-EP*

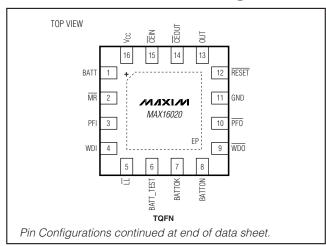
The first placeholder " " designates all output options. Letter "L" indicates push-pull outputs and letter "P" indicates opendrain outputs. The last placeholder "\_" designates the reset threshold (see Table 1).

T = Tape and reel.

+Denotes a lead(Pb)-free/RoHS-compliant package.

Ordering Information continued at end of data sheet. Selector Guide located at end of data sheet.

### Pin Configurations



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Maxim Integrated Products 1

<sup>\*</sup>EP = Exposed pad.

#### **ABSOLUTE MAXIMUM RATINGS**

VCC, BATT, OUT, BATT_TEST to GND0.3V to +6V RESET, RESET, PFO, BATTOK, WDO, BATTON, BATT_TEST, LL, (all open-drain) to GND0.3V to +6V RESET, RESET, BATTOK, WDO, BATTON, LL (all push-pull) to GND0.3V to (Vout + 0.3V) WDI, PFI to GND0.3V to (Vout + 0.3V) CEIN, CEOUT to GND0.3V to (Vout + 0.3V) MR to GND0.3V to (Voct + 0.3V) Input Current VCC Peak Current1A VCC Continuous Current250mA	Output Current OUT Short Circu RESET, RESET, BA Continuous Power 10-Pin TDFN (da 16-Pin TQFN (da Operating Tempera Junction Temperations Lead Temperature Soldering Tempera

Output Current	
OUT Short Circuit to GND Duration	10s
RESET, RESET, BATTON	20mA
Continuous Power Dissipation ( $T_A = +70$ °C)	
10-Pin TDFN (derate 24.4mW/°C above +70°C)	1951mW
16-Pin TQFN (derate 25mW/°C above +70°C)	2000mW
Operating Temperature Range40°0	C to +85°C
Junction Temperature	+150°C
Storage Temperature Range65°C	to +150°C
Lead Temperature (soldering, 10s)	
Soldering Temperature (reflow)	
TDFN	+260°C
TQFN	+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### PACKAGE THERMAL CHARACTERISTICS (Note 1)

TDFN	TQFN
Junction-to Ambient Thermal Resistance (θJA)41°C/W	Junction-to Ambient Thermal Resistance (θJA)40°C/W
Junction-to Case Thermal Resistance (θ <sub>JC</sub> )9°C/W	Junction-to Case Thermal Resistance (θ <sub>JC</sub> )6°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to <a href="https://www.maxim-ic.com/thermal-tutorial">www.maxim-ic.com/thermal-tutorial</a>.

#### **ELECTRICAL CHARACTERISTICS**

 $(V_{CC} = 1.53V \text{ to } 5.5V, V_{BATT} = 3V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at } T_A = +25^{\circ}\text{C.})$  (Note 2)

PARAMETER	SYMBOL	CONDITIO	ONS	MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 3)	VCC, VBATT	VCC or VBATT > VTH		0		5.5	V
			$V_{CC} = 1.62V$		1.2	2	
Supply Current	loo	V00 > V=	$V_{CC} = 2.8V$		1.9	3	
Supply Current	Icc	VCC > VTH	$V_{CC} = 3.6V$		2.3	3.5	μA
			$V_{CC} = 5.5V$		3.4	5	
Supply Current in Battery-Backup Mode	IBATT	V <sub>C</sub> C = 0V			0.25	0.5	μA
V <sub>CC</sub> Switchover Threshold Voltage		V <sub>CC</sub> rising, V <sub>CC</sub> - V <sub>BATT</sub>			0.1 x V <sub>CC</sub>		٧
BATT Switchover Threshold Voltage		V <sub>CC</sub> falling, V <sub>CC</sub> < V <sub>TH</sub> ,	VCC - VBATT		0		mV
BATT Standby Current		V <sub>CC</sub> > V <sub>BATT</sub> + 0.2V		-10		+10	nA
BATT Freshness Leakage Current		V <sub>BATT</sub> = 5.5V				20	nA
		$V_{CC} = 4.75V, I_{OUT} = 150$	0mA		1.4	4.5	
V <sub>CC</sub> to OUT On-Resistance	D	V <sub>CC</sub> = 3.15V, I <sub>OUT</sub> = 65mA			1.7	4.5	Ω
	Ron	V <sub>CC</sub> = 2.35V, I <sub>OUT</sub> = 25mA			2.1	5.0	
		V <sub>C</sub> C = 1.91V, I <sub>OUT</sub> = 10	mA		2.6	5.5	]
Output Voltage in	Value	V <sub>BATT</sub> = 4.5V, I <sub>OUT</sub> = 20	)mA	V <sub>BATT</sub> - C	).1		V
Battery-Backup Mode	Vout	V <sub>BATT</sub> = 2.5V, I <sub>OUT</sub> = 20	)mA	V <sub>BATT</sub> - 0	.15	•	]

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{CC} = 1.53V \text{ to } 5.5V, V_{BATT} = 3V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at } T_A = +25^{\circ}\text{C.})$  (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET OUTPUT (RESET, RESE	T)					
Reset Threshold	VTH		(se	ee Table	e 1)	V
V <sub>CC</sub> Falling to Reset Delay	t <sub>RD</sub>	V <sub>CC</sub> falling at 10V/ms		20		μs
Reset Timeout Period	t <sub>RP</sub>		145	215	285	ms
		V <sub>CC</sub> ≥ 3.3V, I <sub>SINK</sub> = 3.2mA, RESET asserted			0.3	
RESET Output Low Voltage	Vol	V <sub>CC</sub> ≥ 1.6V, I <sub>SINK</sub> = 1mA, RESET asserted			0.3	V
		V <sub>CC</sub> ≥ 1.2V, I <sub>SINK</sub> = 100µA, RESET asserted			0.3	
RESET Output High Voltage (Push-Pull Output)	VoH	V <sub>CC</sub> = 1.1 x V <sub>TH</sub> , I <sub>SOURCE</sub> = 100μA, RESET deasserted	V <sub>OUT</sub> - 0.3			V
RESET Output Leakage Current (Open-Drain Output)		V <sub>RESET</sub> = 5.5V, RESET deasserted			1	μΑ
DESET Output Low Voltage	Voi	V <sub>CC</sub> ≥ 3.3V, I <sub>SINK</sub> = 3.2mA, RESET deasserted			0.3	V
RESET Output Low Voltage	V <sub>OL</sub>	V <sub>CC</sub> ≥ 1.8V, I <sub>SINK</sub> = 1.0mA, RESET deasserted			0.3	V
RESET Output High Voltage (Push-Pull Output)	Vон	V <sub>CC</sub> = 0.9 x V <sub>TH</sub> , I <sub>SOURCE</sub> = 100μA, RESET asserted	V <sub>OUT</sub> - 0.3			V
RESET Output Leakage Current (Open-Drain Output)		V <sub>RESET</sub> = 5.5V, RESET asserted			1	μΑ
POWER-FAIL COMPARATOR						
PFI, Input Threshold	VPFT	$V_{IN}$ falling, 1.6V $\leq$ $V_{CC} \leq$ 5.5V	0.572	0.590	0.611	V
PFI, Hysteresis	V <sub>PFT-HYS</sub>			30		mV
PFI Input Current		$V_{CC} = 5.5V$	-1		+1	μΑ
		V <sub>CC</sub> ≥ 1.6V, I <sub>SINK</sub> = 1mA, output asserted			0.3	
PFO Output Low Voltage	V <sub>OL</sub>	V <sub>CC</sub> ≥ 1.2V, I <sub>SINK</sub> = 100µA, output asserted			0.3	V
PFO Output Voltage High (Push-Pull Output)	Voh	V <sub>CC</sub> = 1.1 x V <sub>TH</sub> , I <sub>SOURCE</sub> = 100μA, output asserted	V <sub>OUT</sub> - 0.3			V
PFO, Leakage Current (Open-Drain Output)		VPFO = 5.5V, output deasserted			1	μΑ
PFO, Delay Time		VPFT + 100mV to VPFT - 100mV		20		μs
MANUAL RESET (MR)						
Input Low Voltage	V <sub>IL</sub>				0.3 x V <sub>CC</sub>	V
Input High Voltage	V <sub>IH</sub>		0.7 x V <sub>CC</sub>			V
Pullup Resistance			20	30		kΩ
Glitch Immunity		Vcc = 3.3V		100		ns
MR to Reset Delay				120		ns

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{CC} = 1.53V \text{ to } 5.5V, V_{BATT} = 3V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at } T_A = +25^{\circ}\text{C.})$  (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WATCHDOG TIMER (WDI, WDO)						
Watchdog Timeout Period	twD		0.83	1.235	1.64	S
Minimum WDI Input Pulse Width	t <sub>WDI</sub>		320			ns
WDI Input Low Voltage	V <sub>IL</sub>	(Note 6)			0.3 x V <sub>CC</sub>	V
WDI Input High Voltage	VIH	(Note 6)	0.7 x V <sub>C</sub> C			٧
WDI Input Current (Note 7)		V <sub>WDI</sub> = 0V or 5.5V, time average	-1		+1	μΑ
WDO Output Low Voltage	V <sub>OL</sub>	V <sub>CC</sub> = 5.0V, I <sub>SINK</sub> = 1mA, WDO asserted			0.3	V
WDO Output High Voltage (Push-Pull Output)	V <sub>OH</sub>	V <sub>CC</sub> = 1.1 x V <sub>TH</sub> , I <sub>SOURCE</sub> = 100μA, WDO deasserted	V <sub>OUT</sub> - 0.3			V
WDO Leakage Current (Open-Drain Output)		V <sub>WDO</sub> = 5.5V, <del>WDO</del> deasserted			1	μΑ
BATTERY-ON INDICATOR (BAT	TON)					
Output Low Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 3.2mA, V <sub>BATT</sub> = 2.1V			0.3	V
BATTON Leakage Current		VBATTON = 5.5V			1	μΑ
BATTON Output High Voltage	V <sub>OH</sub>	V <sub>CC</sub> = 0.9 x V <sub>TH</sub> , I <sub>SOURCE</sub> = 100μA, BATTON asserted	V <sub>OUT</sub> - 0.3			V
Output Short-Circuit Current (Note 4)		Sink current, V <sub>CC</sub> = 5V		60		mA
CE GATING (CEIN, CEOUT)	•					•
CEIN Leakage Current		Reset asserted, V <sub>CC</sub> = 0.9 x V <sub>TH</sub> or 0V	-1		+1	μΑ
CEIN to CEOUT Resistance		Reset not asserted (Note 5)		8	50	Ω
CEOUT Short-Circuit Current		Reset asserted, $\overline{\text{CE}}\text{OUT} = 0$ , $V_{\text{CC}} = 0.9 \times V_{\text{TH}}$		0.75	2	mA
CEIN to CEOUT Propagation Delay		$50\Omega$ source, C <sub>LOAD</sub> = 50pF, V <sub>CC</sub> = 4.75V		1.5	7	ns
Output High Voltage		V <sub>CC</sub> = 5V, V <sub>CC</sub> ≥ V <sub>BATT</sub> , I <sub>SOURCE</sub> = 100μA	0.8 x V <sub>CC</sub>			.,,
Output High Voltage		VCC = 0V, VBATT ≥ 2.2V, ISOURCE = 1µA	V <sub>BATT</sub> - 0.1			
Reset to CEOUT Delay				12		μs

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### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{CC} = 1.53V \text{ to } 5.5V, V_{BATT} = 3V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at } T_A = +25^{\circ}\text{C.})$  (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
LOW LINE (LL)	LOW LINE (LL)						
Low Line to Reset Threshold Voltage		V <sub>CC</sub> falling	(s	ee Table	2)	mV	
V <sub>CC</sub> Falling to LL Delay		V <sub>CC</sub> falling at 10V/ms		20		μs	
LL Output Low Voltage	VOL	V <sub>CC</sub> ≥ 1.6V, I <sub>SINK</sub> = 1mA, LL asserted			0.3		
LE Output Low Voltage	VOL	V <sub>CC</sub> ≥ 1.2V, I <sub>SINK</sub> = 100µA, LL asserted			0.3	7 '	
LL Output High Voltage (Push- Pull Output)	Voн	$V_{CC} = 0.9 \text{ x V}_{TH}_{\overline{LL}}$ , $I_{SOURCE} = 100 \mu A$ , $\overline{LL}$ deasserted	V <sub>OUT</sub> - 0.3			V	
Output Leakage Current		V <sub>LL</sub> = 5.5V, <del>LL</del> deasserted			1	μΑ	
BATTERY-OK INDICATOR (BAT	TOK, BATT_T	EST)					
BATTOK Threshold		Inferred internally from BATT	2.508	2.6	2.673	V	
BATTOK Output Voltage Low	V <sub>OL</sub>	V <sub>CC</sub> = 1.1 x V <sub>TH</sub> , I <sub>SINK</sub> = 1mA, reset asserted			0.3	V	
BATTOK Output High Voltage	Voн	V <sub>CC</sub> = 1.1 x V <sub>TH</sub> , I <sub>SOURCE</sub> = 100μA, BATTOK asserted	V <sub>OUT</sub> - 0.3			V	
BATTOK Output Leakage Current		VBATTOK = 5.5V, deasserted			1	μΑ	
BATT_TEST Output Low Voltage		V <sub>CC</sub> = 1.1 x V <sub>TH</sub> , I <sub>SINK</sub> = 1mA			0.3	V	

- **Note 2:** All devices are 100% production tested at  $T_A = +25^{\circ}C$  and  $T_A = +85^{\circ}C$ . Limits to -40°C are guaranteed by design.
- Note 3: VBATT can be 0V anytime, or VCC can go down to 0V if VBATT is active (except at startup).
- Note 4: Use external current-limit resistor to limit current to 20mA (max).
- **Note 5:**  $\overline{CEIN}/\overline{CEOUT}$  resistance is tested with  $V_{CC} = 5V$  and  $V_{\overline{CEIN}} = 0V$  or 5V.
- Note 6: WDI is internally serviced within the watchdog period if WDI is left unconnected.
- Note 7: The WDI input current is specified as the average input current when the WDI input is driven high or low. The WDI input is designed for a three-stated output device with a 10µA maximum leakage current and capable of driving a maximum capacitive load of 200pF. The three-state device must be able to source and sink at least 200µA when active.

# Table 1a. Reset Threshold Ranges (MAX16016)

SUFFIX	RESET THRESHOLD RANGES (V)					
SUFFIX	MIN	TYP	MAX			
L	4.508	4.63	4.906			
М	4.264	4.38	4.635			
Т	2.991	3.08	3.239			
S	2.845	2.93	3.080			
R	2.549	2.63	2.755			
Z	2.243	2.32	2.425			
Υ	2.117	2.19	2.288			
W	1.603	1.67	1.733			
V	1.514	1.575	1.639			

# Table 1b. Reset Threshold Ranges (MAX16020/MAX16021)

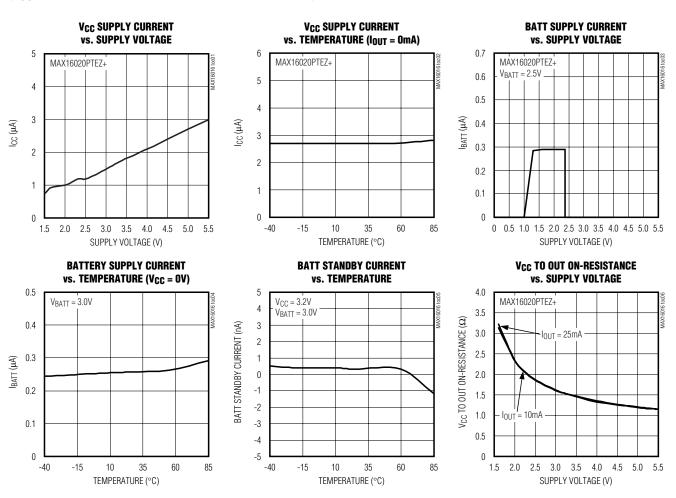
SUFFIX	RESET THRESHOLD RANGES (V)					
SUFFIX	MIN	TYP	MAX			
L	4.520	4.684	4.852			
М	4.275	4.428	4.585			
Т	3.010	3.100	3.190			
S	2.862	2.946	3.034			
R	2.568	2.640	2.716			
Z	2.260	2.323	2.390			
Υ	2.133	2.192	2.255			
W	1.616	1.661	1.710			
V	1.528	1.571	1.618			

**Table 2. Low-Line Threshold Ranges** 

SUFFIX	L	LOW-LINE THRESHOLD RANGES (V)			
	MIN	ТҮР	MAX		
L	4.627	4.806	4.955		
M	4.378	4.543	4.683		
T	3.075	3.181	3.274		
S	2.922	3.023	3.111		
R	2.620	2.409	2.787		
Z	2.309	2.383	2.450		
Υ	2.180	2.246	2.311		
W	1.653	1.704	1.752		
V	1.563	1.612	1.657		

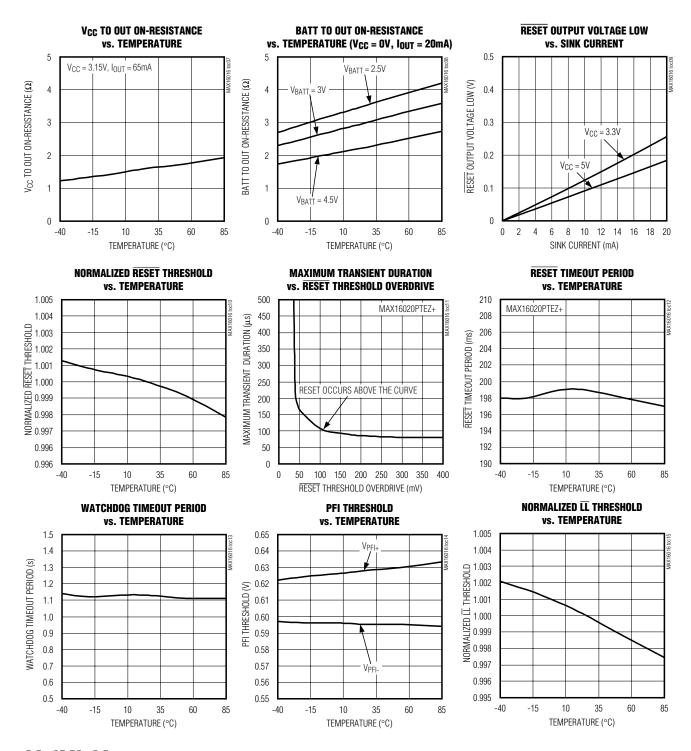
### **Typical Operating Characteristics**

( $V_{CC} = 5V$ ,  $V_{BATT} = 0V$ ,  $T_A = +25$ °C, unless otherwise noted.)



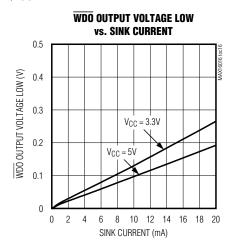
### Typical Operating Characteristics (continued)

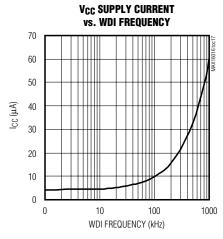
(VCC = 5V, VBATT = 0V, TA = +25°C, unless otherwise noted.)

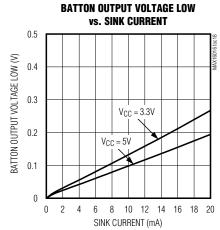


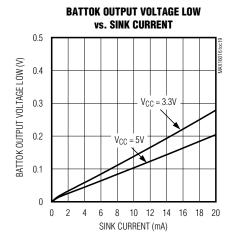
### Typical Operating Characteristics (continued)

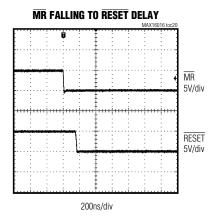
(VCC = 5V, VBATT = 0V, TA = +25°C, unless otherwise noted.)

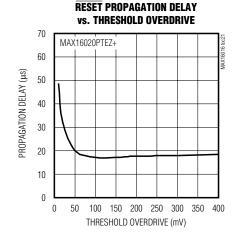


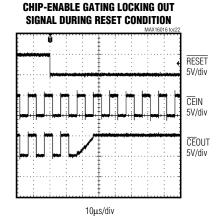












### Pin Description—MAX16016

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PIN	NAME	FUNCTION
1	Vcc	Supply Voltage Input. Bypass V <sub>CC</sub> to GND with a 0.1µF capacitor.
2	BATT	Backup Battery Input. If $V_{CC}$ falls below its reset threshold, and if $V_{BATT} > V_{CC}$ , OUT connects to BATT. If $V_{CC}$ rises above 1.01 x $V_{BATT}$ , OUT connects to $V_{CC}$ . Bypass BATT to GND with a 0.1 $\mu$ F capacitor.
3	MR	Active-Low Manual Reset Input. $\overline{\text{RESET}}$ asserts when $\overline{\text{MR}}$ is pulled low. $\overline{\text{RESET}}$ remains low for the duration of reset timeout period after $\overline{\text{MR}}$ transitions from low to high. Connect $\overline{\text{MR}}$ to $V_{CC}$ or leave unconnected if not used. $\overline{\text{MR}}$ is internally connected to $V_{CC}$ through a $30\text{k}\Omega$ pullup resistor.
4	PFI	Power-Fail Comparator Input. Connect PFI to a resistive divider to set the desired PFI threshold. The PFI input is referenced to an internal VpFT threshold. A VpFT-HYS internal hysteresis provides noise immunity. The power-fail comparator is powered from OUT.
5	WDI	Watchdog Timer Input. If WDI remains high or low for longer than the watchdog timeout period (two), the internal watchdog timer runs out and a reset pulse is triggered for the reset timeout period. The internal watchdog clears when reset asserts or whenever WDI sees a rising or falling edge. To disable the watchdog feature, leave WDI unconnected or three-state the driver connected to WDI.
6	BATTON	Active-High Battery-On Output. BATTON goes high when in battery-backup mode.
7	PFO	Active-Low Power-Fail Comparator Output. PFO goes low when V <sub>PFI</sub> falls below the internal V <sub>PFT</sub> threshold and goes high when V <sub>PFI</sub> rises above V <sub>PFT</sub> + V <sub>PFT-HYS</sub> hysteresis.
8	GND	Ground
9	RESET	Active-Low Reset Output. RESET asserts when V <sub>CC</sub> falls below the reset threshold or $\overline{\text{MR}}$ is pulled low. RESET remains low for the duration of the reset timeout period after V <sub>CC</sub> rises above the reset threshold and $\overline{\text{MR}}$ goes high. RESET also asserts low when the internal watchdog timer runs out.
10	OUT	Switched Output. OUT is connected to $V_{CC}$ when the reset output is not asserted or when $V_{CC}$ is greater than $V_{BATT}$ . OUT connects to BATT when $\overline{RESET}$ is asserted and $V_{BATT}$ is greater than $V_{CC}$ . Bypass OUT to GND with a 0.1µF (min) capacitor.

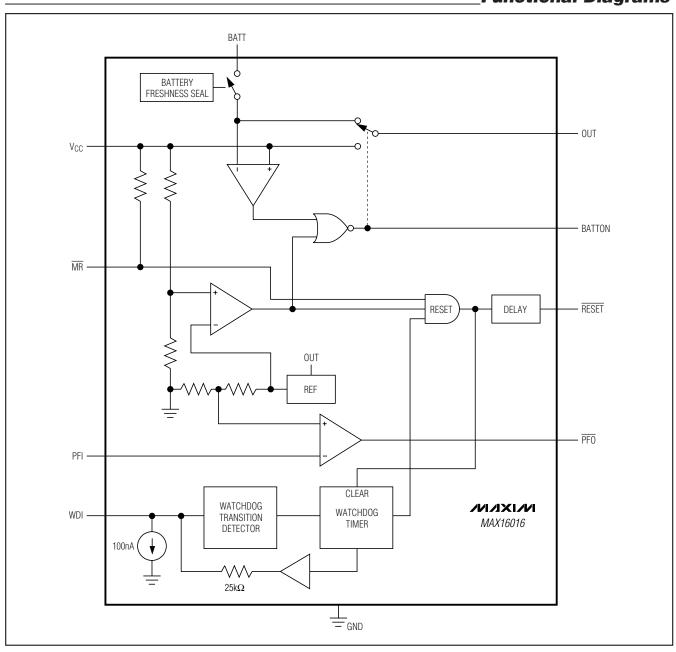
## Pin Description—MAX16020/MAX16021

PIN		NAME	FUNCTION			
MAX16020	MAX16020 MAX16021 NAME		FUNCTION			
1	1	BATT	Backup Battery Input. If $V_{CC}$ falls below its reset threshold, and if $V_{BATT} > V_{CC}$ , OUT connects to BATT. If $V_{CC}$ rises above 1.01 x $V_{BATT}$ , OUT connects to $V_{CC}$ . Bypass BATT to GND with a 0.1 $\mu$ F capacitor.			
2	2	MR	Active-Low Manual Reset Input. $\overline{\text{RESET}}$ asserts when $\overline{\text{MR}}$ is pulled low. $\overline{\text{RESET}}$ remains low for the duration of reset timeout period after $\overline{\text{MR}}$ transitions from low to high. Connect $\overline{\text{MR}}$ to $V_{CC}$ or leave unconnected if not used. $\overline{\text{MR}}$ is internally connected to $V_{CC}$ through a $30\text{k}\Omega$ pullup resistor.			
3	3	PFI	Power-Fail Comparator Input. Connect PFI to a resistive divider to set the desired PFI threshold. The PFI input is referenced to an internal threshold V <sub>PFT</sub> , V <sub>PFT-HYS</sub> internal hysteresis provides noise immunity. The power-fail comparator is powered from OUT.			
4	4	WDI	Watchdog Timer Input. If WDI remains high or low for longer than the watchdog timeout period (twD), the internal watchdog timer runs out and asserts \overline{WDO}. The internal watchdog clears when reset asserts or whenever WDI sees a rising or falling edge. To disable the watchdog feature, leave WDI unconnected or three-state the driver connected to WDI.			
5	5	Ш	Active-Low Low-Line Output. $\overline{LL}$ goes low when V <sub>CC</sub> falls to 2.5% above the reset threshold (Table 2). $\overline{LL}$ provides an early warning of V <sub>CC</sub> failure before reset asserts. Use this output to generate a nonmaskable interrupt (NMI) to initiate an orderly shutdown routine when V <sub>CC</sub> is falling.			
6	_	BATT_TEST	Open-Drain Battery-Test Output. Pulses low for 1.3s every 24 hours during the battery voltage test. If $V_{BATT}$ < 2.6V, BATTOK deasserts low. See Figure 6 for providing additional load during the battery test.			
_	6	RESET	Active-High Reset Output. RESET asserts when $V_{CC}$ falls below the reset threshold or when $\overline{\text{MR}}$ asserts and stays asserted for the reset timeout period after $V_{CC}$ rises above the reset threshold and $\overline{\text{MR}}$ deasserts.			
7	7	BATTOK	Battery-OK Output. BATTOK goes low when the battery voltage falls below the BATTOK threshold (BATTOK is low when in battery-backup mode).			
8	8	BATTON	Active-High Battery-On Output. BATTON goes high when in battery-backup mode.			

### Pin Description—MAX16020/MAX16021 (continued)

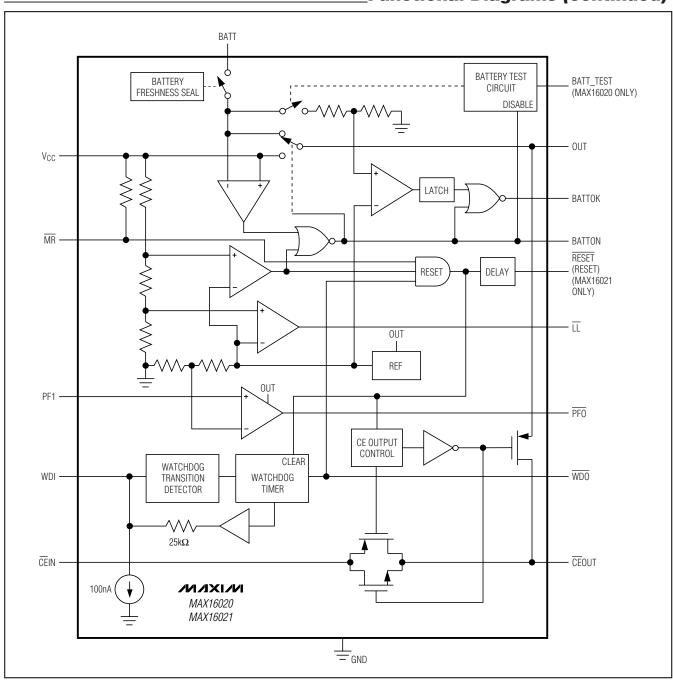
PIN MAX16020 MAX16021		NAME	FUNCTION		
		NAME			
9	9	WDO	Active-Low Watchdog Output. WDO asserts when WDI remains high or low longer than the watchdog timeout period. WDO returns high on the next WDI transition or when a reset is asserted.		
10	10	PFO	Active-Low Power-Fail Comparator Output. PFO goes low when VpFI falls below the internal 0.6V VpFT threshold and goes high when VpFI rises above VpFT + VpFT-HYS hysteresis.		
11	11	GND	Ground		
12	12	RESET	Active-Low Reset Output. $\overline{\text{RESET}}$ asserts when V <sub>CC</sub> falls below the reset threshold or $\overline{\text{MR}}$ is pulled low. $\overline{\text{RESET}}$ remains low for the duration of the reset timeout period after V <sub>CC</sub> rises above the reset threshold and $\overline{\text{MR}}$ goes high.		
13	13	OUT	Switched Output. OUT is connected to $V_{CC}$ when the reset output is not asserted or when $V_{CC}$ is greater than $V_{BATT}$ . OUT connects to BATT when $\overline{RESET}$ is asserted and $V_{BATT}$ is greater than $V_{CC}$ . Bypass OUT to GND with a 0.1µF (min) capacitor.		
14	14	CEOUT	Active-Low Chip-Enable Output. $\overline{\text{CE}}\text{OUT}$ goes low only when $\overline{\text{CE}}\text{IN}$ is low and reset is not asserted. If $\overline{\text{CE}}\text{IN}$ is low when reset is asserted, $\overline{\text{CE}}\text{OUT}$ stays low for 12µs (typ) or until $\overline{\text{CE}}\text{IN}$ goes high, whichever occurs first.		
15	15	CEIN	Chip-Enable Input. The input to CE gating circuitry. Connect to GND or OUT if not used		
16	16	Vcc	Supply Voltage Input. Bypass V <sub>CC</sub> to GND with a 0.1µF capacitor.		
_	_	EP	Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to aid heat dissipation. Do not use EP as the only ground connection for the device.		

### **Functional Diagrams**



12 \_\_\_\_\_\_\_ **/\/**/**X//**/

### **Functional Diagrams (continued)**



### **Detailed Description**

The *Typical Application Circuit* shows a typical connection using the MAX16020. OUT powers the static random-access memory (SRAM). If V<sub>CC</sub> is greater than the reset threshold (V<sub>TH</sub>), or if V<sub>CC</sub> is lower than V<sub>TH</sub>, but higher than V<sub>BATT</sub>, V<sub>CC</sub> connects to OUT. If V<sub>CC</sub> is lower than V<sub>TH</sub> and V<sub>CC</sub> is less than V<sub>BATT</sub>, BATT connects to OUT (see the *Functional Diagrams*). In battery-backup mode, an internal MOSFET connects the backup battery to OUT. The on-resistance of the MOSFET is a function of backup-battery voltage and temperature.

#### **Backup-Battery Switchover**

In a brownout or power failure, it may be necessary to preserve the contents of the RAM. With a backup battery installed at BATT, the MAX16016/MAX16020/MAX16021 automatically switch the RAM to the backup power when V<sub>CC</sub> falls. The MAX16016/MAX16020/MAX16021 have a BATTON output that goes high when in battery-backup mode. These devices require two conditions before switching to battery-backup mode:

- 1) V<sub>CC</sub> must be below the reset threshold.
- 2) VCC must be below VBATT.

Table 3 lists the status of the inputs and outputs in battery-backup mode. The device does not power up if the only voltage source is on BATT. OUT only powers up from VCC at startup.

#### **CE Signal Gating**

The MAX16020/MAX16021 provide internal gating of CE signals to prevent erroneous data from being written to CMOS RAM in the event of a power failure or

Table 3. Input and Output Status in Battery-Backup Mode

PIN	STATUS		
Vcc	Disconnected from OUT		
OUT	Connected to BATT		
BATT	Connected to OUT. Current drawn from the battery is less than 0.55 $\mu$ A (at V <sub>BATT</sub> = 3V, excluding I <sub>OUT</sub> ) when V <sub>CC</sub> = 0V.		
RESET/RESET	Asserted		
BATTON, WDO	High state (push-pull), high impedance (open-drain)		
BATTOK, LL	Low state		
CEIN	Disconnected from CEOUT		
CEOUT	Pulled up to V <sub>OUT</sub>		
PFO	Not affected		

brownout. During normal operation, the CE gate is enabled and passes all CE transitions. When the reset output asserts, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM.  $\overline{\text{CE}\text{OUT}}$  is pulled up to OUT through an internal current source. The 1.5ns propagation delay from  $\overline{\text{CE}\text{IN}}$  to  $\overline{\text{CE}\text{OUT}}$  allows the devices to be used with most  $\mu\text{Ps}$  and high-speed DSPs.

During normal operation (reset not asserted),  $\overline{\text{CEIN}}$  is connected to  $\overline{\text{CEOUT}}$  through a low on-resistance transmission gate. If  $\overline{\text{CEIN}}$  is high when a reset asserts,  $\overline{\text{CEOUT}}$  remains high regardless of any subsequent transition on  $\overline{\text{CEIN}}$  during the reset event.

If  $\overline{\text{CE}}\text{IN}$  is low when reset asserts,  $\overline{\text{CE}}\text{OUT}$  is held low for 12µs to allow completion of the read/write operation. After the 12µs delay expires,  $\overline{\text{CE}}\text{OUT}$  goes high and stays high regardless of any subsequent transitions on  $\overline{\text{CE}}\text{IN}$  during the reset event. When  $\overline{\text{CE}}\text{OUT}$  is disconnected from  $\overline{\text{CE}}\text{IN}$ ,  $\overline{\text{CE}}\text{OUT}$  is actively pulled up to OUT.

The propagation delay through the CE circuitry depends on both the source impedance of the drive to CEIN and the capacitive loading at CEOUT. Minimize the capacitive load at CEOUT to minimize the propagation delay, and use a low output-impedance driver.

#### Low-Line Output (LL)

The low-line comparator monitors VCC with a threshold voltage typically 2.5% higher than the reset threshold (see Table 2).  $\overline{LL}$  asserts prior to a reset condition during a brownout condition. On power-up,  $\overline{LL}$  deasserts after the reset output.  $\overline{LL}$  can be used to provide a nonmaskable interrupt (NMI) to the  $\mu P$  when the voltage begins to fall to initiate an orderly software shutdown routine.

#### Manual Reset Input

Many  $\mu P$ -based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. For the MAX16016/MAX16020/MAX16021, a logic-low on  $\overline{MR}$  asserts RESET/RESET. RESET/RESET remains asserted while  $\overline{MR}$  is low. When  $\overline{MR}$  goes high RESET/RESET deasserts after a minimum of 145ms (tRP).  $\overline{MR}$  has an internal 30k $\Omega$  pullup resistor to VCC.  $\overline{MR}$  can be driven with TTL/CMOS logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from  $\overline{MR}$  to GND to create a manual reset function; external debounce circuitry is not required. If  $\overline{MR}$  is driven from a long cable or the device is used in a noisy environment, connect a 0.1 $\mu F$  capacitor from  $\overline{MR}$  to GND to provide additional noise immunity.

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#### **Watchdog Timer**

#### Watchdog Input

The watchdog monitors µP activity through the input WDI. If the µP becomes inactive, either the reset output is asserted in pulses (MAX16016) or the watchdog output goes low (MAX16020/MAX16021). To use the watchdog function, connect WDI to a bus line or µP I/O line. If WDI remains high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and RESET asserts for the reset timeout period (MAX16016) or WDO goes low (MAX16020/MAX16021). The internal watchdog timer clears whenever the reset output asserts or the WDI sees a rising or falling edge within the watchdog timeout period. The WDI input is designed for a threestated output device with a 10µA maximum leakage current and the capability of driving a maximum capacitive load of 200pF. The three-state device must be able to source and sink at least 200µA when active. Disable the watchdog timer by leaving WDI unconnected or by three-stating the driver connected to WDI. The watchdog timer periodically attempts to pulse WDI to the opposite logic-level through a  $25k\Omega$  resistor for  $40\mu$ s to determine whether WDI is either unconnected or latched to a logic state. The watchdog function is also disabled when in battery-backup mode.

#### Watchdog Output

WDO remains high if there is a transition or pulse at WDI during the watchdog-timeout period. WDO goes low if no transition occurs at WDI during the watchdog timeout period and remains low until the next transition at WDI or when a reset is asserted. Connect WDO to MR to generate a system reset on every watchdog fault. When a

watchdog fault occurs in this mode, WDO goes low, which pulls MR low, causing a reset pulse to be issued. As soon as the reset output is asserted, the watchdog timer clears and WDO returns high. With WDO connected to MR, a continuous high or low on WDI causes 145ms (min) reset pulses to be issued every 1.235s.

# Battery Testing Function/BATTOK Indicator (MAX16020/MAX16021)

The MAX16020/MAX16021 feature a battery testing function that works in conjunction with the BATTOK output. The battery voltage is tested for 1.235s after VCC is applied and once every 24 hours thereafter. During this test, an internal  $100 k\Omega$  resistor is connected from BATT to ground and the battery is monitored to ensure that the battery voltage is above 2.6V. If the battery voltage is below 2.6V, the BATTOK output deasserts low to indicate a weak battery condition. The MAX16020 has a BATT\_TEST output that pulses high during the battery voltage test. Connect a resistor and FET as shown in Figure 6 to provide an additional load during the battery test. In battery-backup mode, the battery testing function is disabled and BATTOK goes low.

#### **Battery Freshness Seal Mode**

The MAX16016/MAX16020/MAX16021 battery freshness seal disconnects the backup battery from internal circuitry and OUT until VCC is applied. This ensures the backup battery connected to BATT is fresh when the final product is used for the first time.

The internal freshness seal latch prevents BATT from powering OUT until  $V_{CC}$  has come up for the first time, setting the latch. When  $V_{CC}$  subsequently turns off, BATT begins to power OUT.

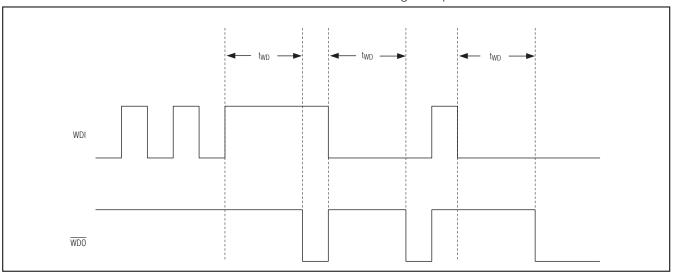


Figure 1. Watchdog Timing (MAX16016/MAX16020)

To reenable the freshness seal:

- 1) Connect a battery to BATT.
- 2) Bring VCC to 0V.
- 3) Drive  $\overline{MR}$  higher than  $V_{BATT}$  + 1.2V for at least 3µs.
- 4) Pull OUT to 0V.

#### **Reset Output**

A  $\mu P$ 's reset input starts the  $\mu P$  in a known state. The  $\mu P$  supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. Reset output is guaranteed to be a logic-low or logic-high depending on the device chosen. RESET or RESET asserts when  $V_{CC}$  is below the reset threshold and remains asserted for at least 145ms (tRP) after  $V_{CC}$  rises above the reset threshold. RESET or RESET also asserts when  $\overline{MR}$  is low. The MAX16016 watchdog function causes  $\overline{RESET}$  to assert in pulses following a watchdog timeout. The reset output is available in both push-pull and open-drain configurations.

#### **Power-Fail Comparator**

The MAX16016/MAX16020/MAX16021 offer an undervoltage comparator that the output PFO goes low when the voltage at PFI falls below its VPFT threshold.

Common uses for the power-fail comparator include monitoring the power supply (such as a battery) before any voltage regulation to provide an early power-fail warning, so software can conduct an orderly system shutdown. The power-fail comparator has a typical input hysteresis of VPFT-HYS and is powered from OUT, making it independent of the reset circuit. Connect the PFI input to GND if not used.

### Applications Information

#### **Monitoring an Additional Supply**

The MAX16016/MAX16020/MAX16021  $\mu P$  supervisors can monitor either positive or negative supplies using a resistive voltage-divider to PFI.  $\overline{PFO}$  can be used to generate an interrupt to the  $\mu P$  or to trigger a reset (Figures 2 and 3). To monitor a negative supply, connect the top of the resistive divider to VCC. Connect the bottom of the resistive divider to the negative voltage to be monitored.

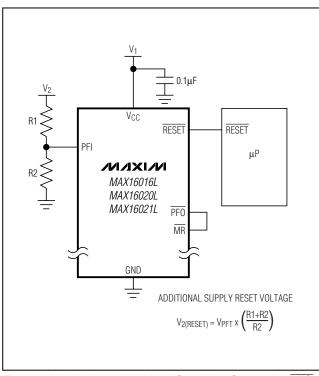


Figure 2. Monitoring an Additional Supply by Connecting  $\overline{PFO}$  to  $\overline{MR}$ 

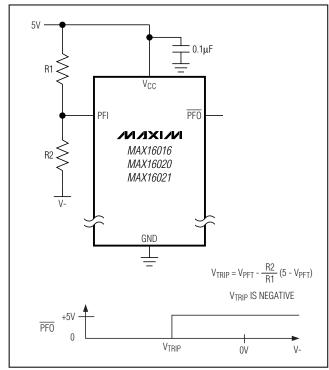


Figure 3. Monitoring a Negative Supply

#### **Adding Hysteresis to PFI**

The power-fail comparators have a typical input hysteresis of VPFT-HYS. This is sufficient for most applications where a power-supply line is being monitored through an external voltage-divider (see the *Monitoring an Additional Supply* section). Figure 4 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 so that PFI sees VPFT when VIN falls to the desired trip point (VTRIP). Resistor R3 adds hysteresis. R3 is typically an order of magnitude greater than R1 or R2. R3 should be larger than 50k $\Omega$  to prevent it from loading down  $\overline{\text{PFO}}$ . Capacitor C1 adds additional noise rejection.

#### **Battery-On Indicator (Push-Pull Version)**

BATTON goes high when in battery-backup mode. Use BATTON to indicate battery-switchover status or to supply base drive to an external pass transistor for higher current applications (Figure 5).

**Operation Without a Backup Power Source** The MAX16016/MAX16020/MAX16021 provide a battery-backup function. If a backup power source is not used, connect BATT to GND and OUT to  $V_{CC}$ .

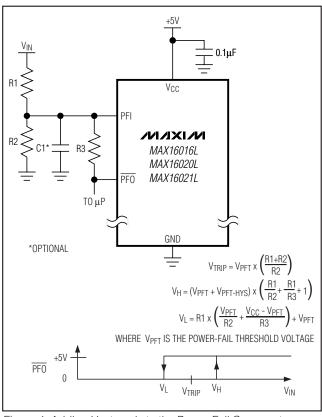


Figure 4. Adding Hysteresis to the Power-Fail Comparator

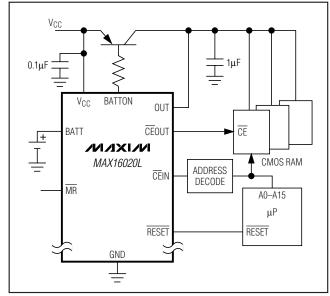


Figure 5. BATTON Driving an External Pass Transistor

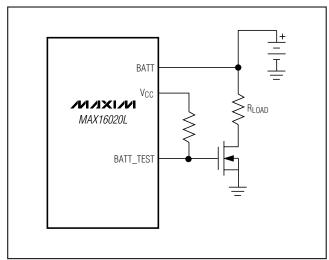


Figure 6. Adjustable BATT\_TEST Load

#### Replacing the Backup Battery

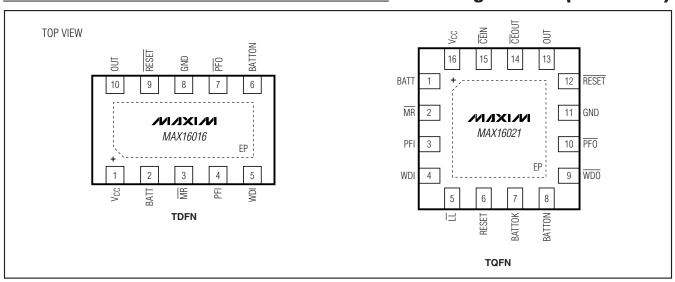
When  $V_{CC}$  is above  $V_{TH}$ , the backup power source can be removed without danger of triggering a reset pulse. The device does not enter battery-backup mode when  $V_{CC}$  stays above the reset threshold voltage.

#### **Negative-Going Vcc Transients**

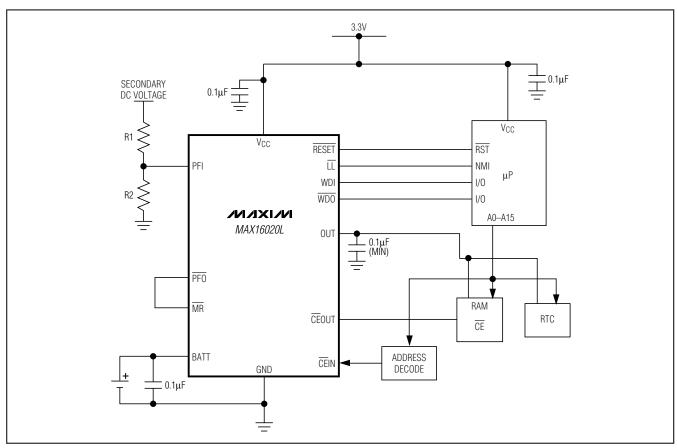
The MAX16016/MAX16020/MAX16021 are relatively immune to short duration, negative going V<sub>CC</sub> transients. Resetting the  $\mu$ P when V<sub>CC</sub> experiences only small glitches is usually not desirable. A 0.1 $\mu$ F bypass capacitor mounted close to V<sub>CC</sub> provides additional transient immunity.

18 \_\_\_\_\_\_ **/V**|/X|/M

### Pin Configurations (continued)



### **Typical Application Circuit**



#### **Selector Guide**

PART	ALL LOGIC OUTPUTS (EXCEPT BATT_TEST)	MR	POWER-FAIL COMPARATOR	WATCHDOG TIMER	BATTON	LOW- LINE OUTPUT	BATTOK/ BATT_TEST/ RESET	CHIP- ENABLE
MAX16016LTB_	Push-pull	$\checkmark$	$\sqrt{}$	WDI	√	_	_	_
MAX16016PTB_	Open-drain	$\sqrt{}$	$\checkmark$	WDI	$\checkmark$	_	_	_
MAX16020LTE_	Push-pull	~	<b>V</b>	WDI/WDO	<b>V</b>	V	BATTOK/ BATT_TEST	<b>V</b>
MAX16020PTE_	Open-drain	<b>√</b>	<b>V</b>	WDI/WDO	<b>V</b>	V	BATTOK/ BATT_TEST	<b>√</b>
MAX16021LTE_	Push-pull	<b>√</b>	<b>V</b>	WDI/WDO	<b>V</b>	V	BATTOK/ RESET	<b>√</b>
MAX16021PTE_	Open-drain	<b>√</b>	V	WDI/WDO	√	$\sqrt{}$	BATTOK/ RESET	<b>√</b>

### Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	
MAX16020_TE_+T	-40°C to +85°C	16 TQFN-EP*	
MAX16021_TE_+T	-40°C to +85°C	16 TQFN-EP*	

The first placeholder "\_" designates all output options. Letter "L" indicates push-pull outputs and letter "P" indicates opendrain outputs. The last placeholder "\_" designates the reset threshold (see Table 1).

T = Tape and reel.

### Chip Information

PROCESS: BICMOS

### \_Package Information

For the latest package outline information and land patterns (footprints), go to <a href="https://www.maxim-ic.com/packages">www.maxim-ic.com/packages</a>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 TDFN-EP	T1033+1	<u>21-0137</u>	90-0093
16 TQFN-EP	T1644+4	<u>21-0139</u>	<u>90-0070</u>

<sup>+</sup>Denotes a lead(Pb)-free/RoHS-compliant package.

<sup>\*</sup>EP = Exposed pad.

#### **Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED	
0	5/08	Initial release		
1	7/08	Released the MAX16016. Updated <i>Ordering Information, Electrical Characteristics</i> , Tables 1 and 2, <i>Pin Description</i> , and <i>Detailed Description</i> .	1, 3, 4, 5, 9, 10, 12, 13, 15, 16, 19, 20	
2	10/08	Released the MAX16021.	20	
3	12/08	Updated <i>Electrical Characteristics</i> , <i>Pin Description</i> , Table 3, and the <i>Power-Fail Comparator</i> section.	3, 9, 10, 11, 14, 16	
4	1/10	Updated Electrical Characteristics.	4	
5	4/11	Updated Pin Description.	9, 10	
6	11/11	Updated Pin Description.	9, 10	

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