300mA Low Voltage Buck-Boost Converter with PowerPath and 1.6µA Quiescent Current

FEATURES

- **Dual Input Buck-Boost with Integrated PowerPath™ Manager**
- **Ultralow Start-Up Voltages: 850mV Start with No Backup Source, 300mV with a Backup Source**
- **Compatible with Primary or Rechargeable Backup Batteries**
- **Digitally Selectable V_{OUT} and V_{STORE}**
- **Maximum Power Point Control**
- **Ultralow Quiescent Current: 1.6µA**
- Regulated Output with V_{IN} or V_{STORE} Above, Below or Equal to the Output
- Optional Backup Battery Trickle Charger
- Shelf Mode Disconnect Function to Preserve Battery Shelf Life
- Burst Mode® Operation
- Accurate RUN Pin Threshold
- Power Good Output Voltage Indicator
- Selectable Peak Current Limit: 90mA/650mA
- Available in Thermally Enhanced 3mm × 4mm 16-Pin QFN and 20-Pin TSSOP Packages

APPLICATIONS

- Wireless Sensor Networks
- Home or Office Building Automation
- Energy Harvesting
- Remote Sensors

DESCRIPTION

The LTC®3106 is a highly integrated, ultralow voltage buck-boost DC/DC converter with automatic PowerPath management optimized for multisource, low power systems. At no load, the LTC3106 draws only 1.6µA while creating an output voltage up to 5V from either input source.

If the primary power source is unavailable, the LTC3106 seamlessly switches to the backup power source. The LTC3106 is compatible with either rechargeable or primary cell batteries and can trickle charge a backup battery whenever there is an energy surplus available. Optional maximum power point control ensures power transfer is optimized between power source and load. The output voltage and backup voltage, V_{STORE}, are programmed digitally, reducing the required number of external components. Zero power Shelf Mode ensures that the backup battery will remain charged if left connected to the LTC3106 for an extended time.

Additional features include an accurate turn-on voltage, a power good indicator for V_{OUT}, a user selectable 100mA peak current limit setting for lower power applications, thermal shutdown as well as user selectable backup power and output voltages.

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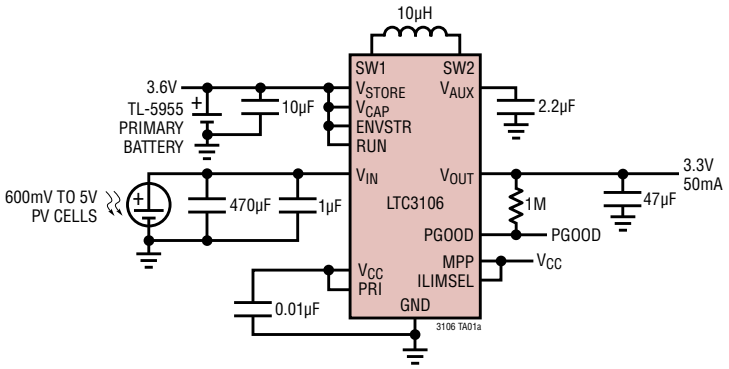
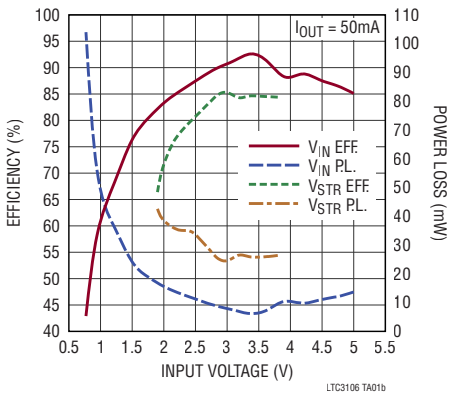
TYPICAL APPLICATION

Solar Cell Input with Primary Battery Backup



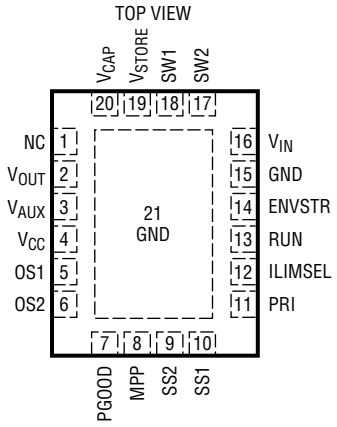
Efficiency vs Input Voltage



ABSOLUTE MAXIMUM RATINGS (Notes 1, 6)

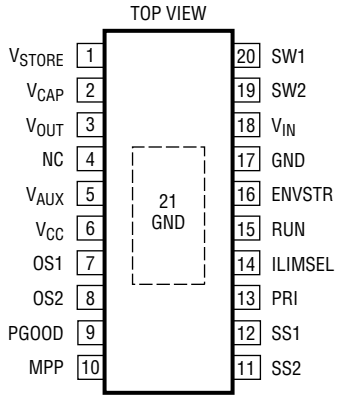
Supply Voltages
V_{IN}, V_{STORE}, V_{OUT}, V_{CAP} ..... –0.3V to 6V
All Other Pins ..... –0.3V to 6V
Operating Junction Temperature Range
(Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
FE Package ..... 300°C

PIN CONFIGURATION



UDC PACKAGE
20-LEAD (3mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 52°C/W, θ_{JC} = 7°C/W (Note 5)
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 48.6°C/W, θ_{JC} = 8.6°C/W (Note 5)
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3106EUDC#PBF	LTC3106EUDC#TRPBF	LGQH	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3106IUDC#PBF	LTC3106IUDC#TRPBF	LGQH	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3106EFE#PBF	LTC3106EFE#TRPBF	LTC3106FE	20-Lead Plastic TSSOP	–40°C to 125°C
LTC3106IFE#PBF	LTC3106IFE#TRPBF	LTC3106FE	20-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 1.5V, V_{OUT} = 3.3V, V_{STORE} = 3.6V and V_{AUX} in regulation unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Start-Up Voltage	Start-Up from V_{IN}, V_{OUT} = V_{AUX} = V_{STORE} = 0V, RUN = V_{IN}	●		0.85	1.2	V
V_{IN} Maximum Operating Voltage					5.1	V
V_{IN} Minimum Operating Voltage	V_{STORE} in Operating Voltage Limits, RUN > 0.613V, ENVSTR Pin > 0.8V (Minimum Voltage Is Load Dependent)	●	0.25	0.3	0.35	V
V_{IN} Minimum No-Load Start-Up Power	Start-Up from V_{IN}, RUN = V_{IN}, V_{OUT} = V_{AUX} = V_{STORE} = 0V			12		µW
V_{IN} Undervoltage Quiescent Current	Start-Up from V_{IN}, RUN = V_{IN}, V_{OUT} = V_{AUX} = V_{STORE} = 0V	●		1	2	µA
Shutdown Current – V_{IN}	V_{STORE} = 0V, RUN = 0 T_J = –40°C to 85°C (Note 4)	●		300 300	750 450	nA nA
Quiescent Current – V_{IN}	Switching Enabled, V_{OUT} in Regulation, Non-Switching	●		0.1	1	µA
	Switching Enabled, V_{OUT} in Regulation, Non-Switching, T_J = –40°C to 85°C (Note 4)			0.1	0.3	µA
V_{STORE} Maximum Operating Voltage	PRI = V_{CC}, ENVSTR = V_{STORE}	●			4.3	V
V_{STORE} Minimum Operating Voltage	V_{OUT} in Regulation, V_{CAP} Shorted to V_{STORE}, PRI = V_{CC}, ENVSTR = V_{STORE}		2.1			V
V_{STORE} Under Voltage Lockout	PRI = V_{CC}, ENVSTR = V_{STORE}	●	1.730	1.778	1.826	V
V_{STORE} Operating Voltage (Note 7)	SS1 = 0V, SS2 = 0V OV UV	● ●	3.90 2.70	4.00 2.78	4.10 2.86	V V
	SS1 = 0V, SS2 = V_{CC} OV UV	● ●	2.81 1.85	2.90 1.90	2.99 1.95	V V
	SS1 = V_{CC}, SS2 = 0V OV UV	● ●	2.91 2.08	3.00 2.15	3.08 2.21	V V
	SS1 = V_{CC}, SS2 = V_{CC} OV UV	● ●	3.90 2.91	4.00 3.00	4.10 3.08	V V
Output Regulation Voltage	1.8V V_{OUT} Selected	●	1.75	1.8	1.85	V
	T_J = –40°C to 85°C (Note 4)		1.755	1.8	1.845	V
	2.2V V_{OUT} Selected	●	2.14	2.2	2.25	V
	T_J = –40°C to 85°C (Note 4)		2.145	2.2	2.245	V
	3.3V V_{OUT} Selected	●	3.22	3.3	3.40	V
	T_J = –40°C to 85°C (Note 4)		3.23	3.3	3.38	V
	5V V_{OUT} Selected	●	4.90	5.0	5.10	V
	T_J = –40°C to 85°C (Note 4)		4.92	5.0	5.08	V
Quiescent Current – V_{AUX}	Enabled, V_{OUT} in Regulation, Non-Switching, T_J = –40°C to 85°C (Note 4)	●		1.6 1.6	3 2.5	µA µA
Quiescent Current – V_{OUT}	Enabled, V_{OUT} in Regulation, Non-Switching, T_J = –40°C to 85°C (Note 4)	●		0.1 0.1	1 0.3	µA µA
Quiescent Current – V_{STORE}	Enabled, V_{OUT} in Regulation, Non-Switching, V_{CAP} Shorted to V_{STORE} T_J = –40°C to 85°C (Note 4)	●		0.1 0.1	1 0.3	µA µA
Shutdown Current – V_{STORE}	V_{IN} = 0V, V_{CAP} Shorted to V_{STORE}, ENVSTR = 0V T_J = –40°C to 85°C (Note 4)	●		0.1 0.1	0.7 0.3	µA µA
Shelf Mode V_{STORE} Leakage Current	Isolated V_{STORE}, ENVSTR = 0V			0.1	25	nA
N-Channel MOSFETs – Leakage Current	B and C Switches			0.1	1	µA
P-Channel MOSFETs – Leakage Current	A1, A2, D1 and D2 Switches			0.1	1	µA
N-Channel MOSFET B and C Switch $R_{DS(ON)}$	V_{IN} = 5V			0.5		Ω
P-Channel MOSFET A1 $R_{DS(ON)}$	V_{IN} = 5V			0.5		Ω
P-Channel MOSFET A2 $R_{DS(ON)}$	V_{STORE} = V_{CAP} = 4.2V			1.9		Ω
P-Channel MOSFET D1 $R_{DS(ON)}$	V_{OUT} = 3.3V			0.9		Ω
P-Channel MOSFET D2 $R_{DS(ON)}$	V_{STORE} = V_{CAP} = 4.2V			2.9		Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 1.5V, V_{OUT} = 3.3V, V_{STORE} = 3.6V and V_{AUX} in regulation unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
P-Channel MOSFET AUXSW $R_{DS(ON)}$	V_{AUX} = 5.4V			3		Ω
P-Channel V_{STORE} Isolation MOSFET $R_{DS(ON)}$	V_{STORE} = 4.2V			2		Ω
Peak Current Limit (V_{OUT})	V_{OUT} Powered from V_{IN}, ILIMSEL > 0.8V V_{OUT} Powered from V_{IN}, ILIMSEL = 0V V_{OUT} Powered from V_{STORE}, ILIMSEL > 0.8V V_{OUT} Powered from V_{STORE}, ILIMSEL = 0V	● ● ● ●	530 60 140 60	725 100 200 100		mA mA mA mA
VALLEY Current Limit	V_{OUT} Powered from V_{IN}, ILIMSEL > 0.8V V_{OUT} Powered from V_{IN}, ILIMSEL = 0V V_{OUT} Powered from V_{STORE}, ILIMSEL > 0.8V V_{OUT} Powered from V_{STORE}, ILIMSEL = 0V	● ● ● ●	300 10 30 10	400 44 70 44		mA mA mA mA
Peak Current Limit (V_{STORE} Charging)	V_{STORE} Powered from V_{IN}	●	60	100		mA
PGOOD Threshold	V_{OUT} Falling, Percentage Below V_{OUT}		–11	–9	–7	%
PGOOD Hysteresis	Percentage of V_{OUT}			3		%
PGOOD Voltage Low	I_{PGOOD} = 100µA			0.2		V
PGOOD Leakage Current	V_{PGOOD} = 5V			0.1	10	nA
V_{IH} Digital Input High Logic Level	Pins: OS[1:2], SS[1:2], ILIMSEL, ENVSTR, PRI	●	0.8			V
V_{IL} Digital Input Low Logic Level	Pins: OS[1:2], SS[1:2], ILIMSEL, ENVSTR, PRI	●			0.3	V
Digital Input Leakage Current	Pin Voltage = 5.2V, Pins: OS[1:2], SS[1:2], ILIMSEL, PRI			0.1	10	nA
ENVSTR Input Leakage Current		●		44	80	nA
Auxiliary Voltage Threshold	V_{AUX} Rising			5.2		V
Auxiliary Voltage Hysteresis	V_{AUX} Falling, Restart V_{AUX} Charging			50		mV
MPP Pin Output Current	V_{MPP} = 0.6V	●	1.21	1.5	1.72	µA
MPP Pin Shutdown Current	V_{MPP} = V_{CC}			0.1	10	nA
MPP Disable Threshold	Voltage Below V_{CC}		–1	–0.8		V
RUN Threshold - Enable Reference		●	0.15	0.4	0.55	V
Accurate RUN Threshold - Enable Switching from V_{IN}	RUN Pin Voltage Increasing T_J = –40°C to 85°C (Note 4)	●	0.585 0.591	0.6 0.6	0.615 0.609	V V
Accurate RUN Hysteresis				100		mV
RUN Input Current				0.1	10	nA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3106 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3106E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3106I is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D)according to the formula:

$$T_J = T_A + (P_D)(\theta_{JA}°C/W)$$

where θ_{JA} is the package thermal impedance. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: Specification is guaranteed by design and not 100% tested in production.

Note 5: Failure to solder exposed backside of the package to the PC board will result in a higher thermal resistance

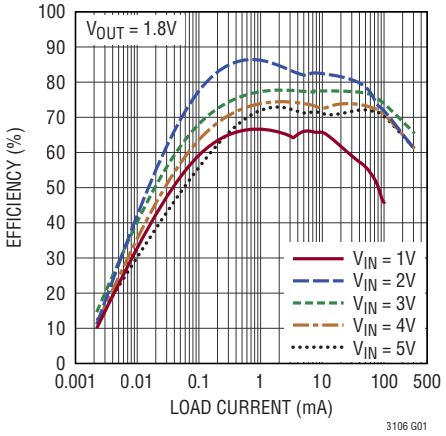
Note 6: Voltage transients on the switch pins beyond the DC limits specified in Absolute Maximum Ratings are non-disruptive to normal operation when using good layout practices as described elsewhere in the data sheet and as seen on the demo board.

Note 7: If PRI = GND, then charging is enabled on V_{STORE} whenever surplus energy is available from V_{IN}. The OV and UV thresholds are the maximum charge and discharge levels controlled by the LTC3106.

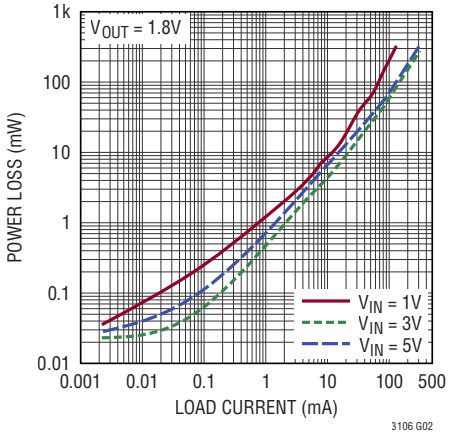
Note 8: Some of the IC electrical characteristics are measured in an open-loop test configuration that may differ from the typical operating conditions. These differences are not critical for the accuracy of the parameter and will not impact operation.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

V_{IN} Efficiency vs Load Current



V_{IN} Power Loss vs Load Current



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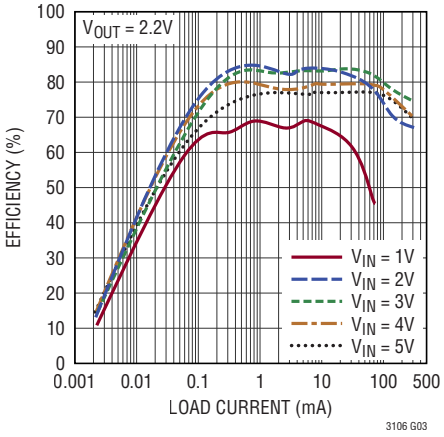

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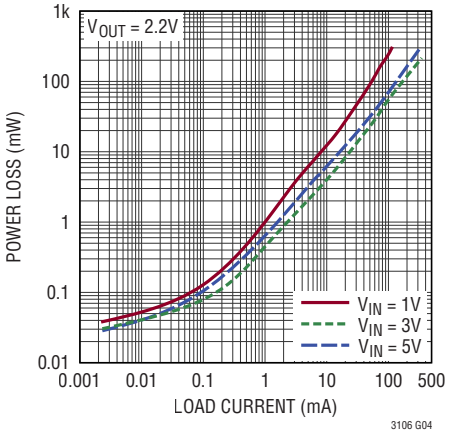

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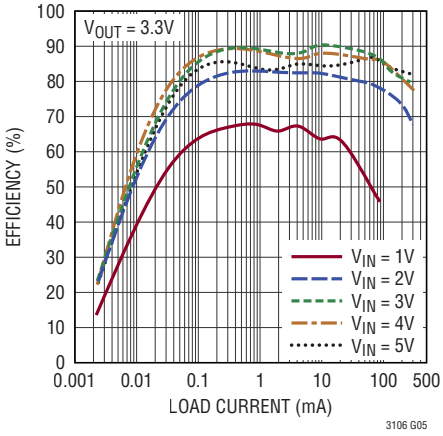

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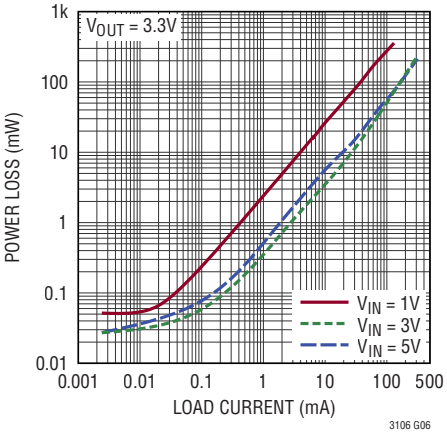
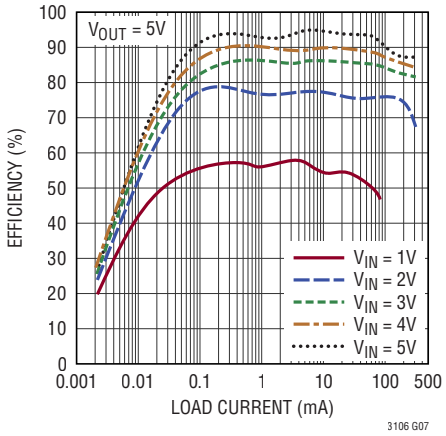
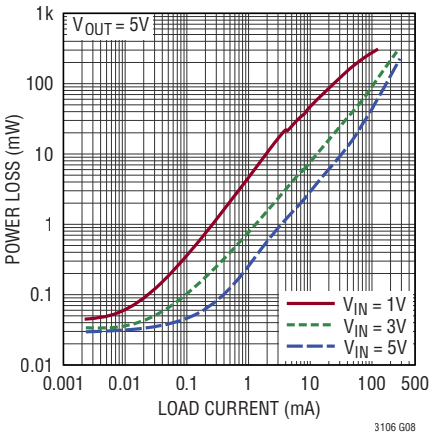


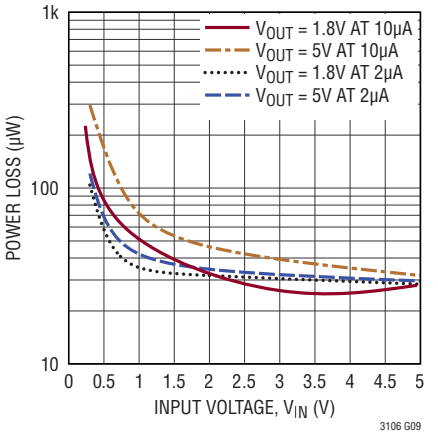
V_{IN} Efficiency vs Load Current



V_{IN} Power Loss vs Load Current

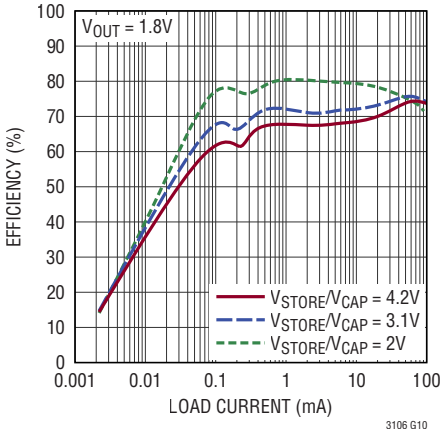


Light Load Power Loss vs Input Voltage (V_{IN})

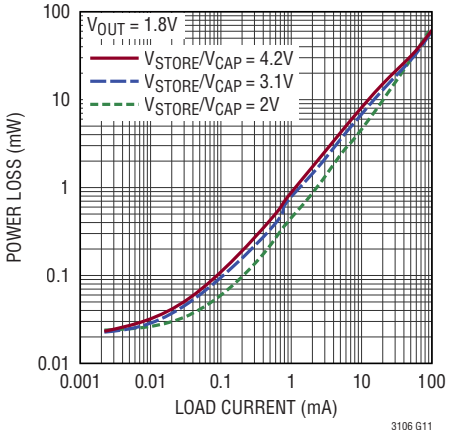


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

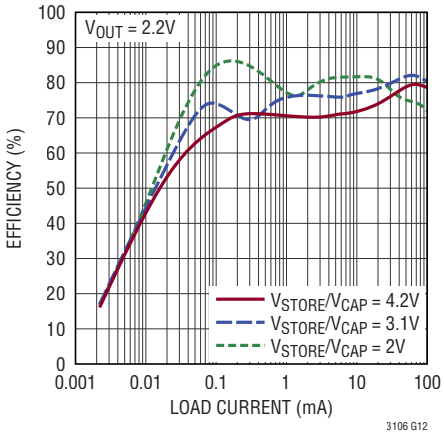
V_{STORE}/V_{CAP} Efficiency vs Load Current



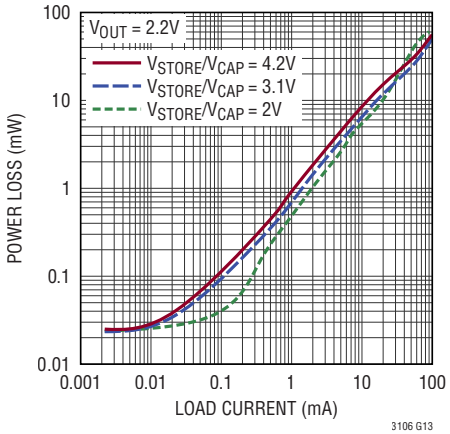
V_{STORE}/V_{CAP} Power Loss vs Load Current



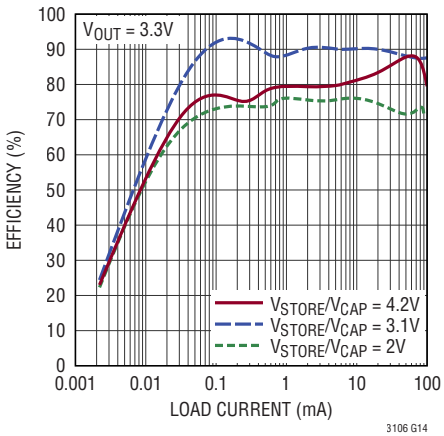
V_{STORE}/V_{CAP} Efficiency vs Load Current



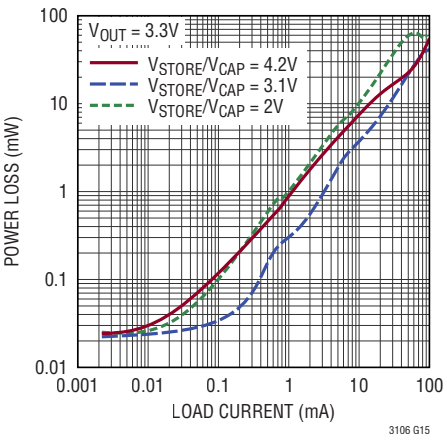
V_{STORE}/V_{CAP} Power Loss vs Load Current



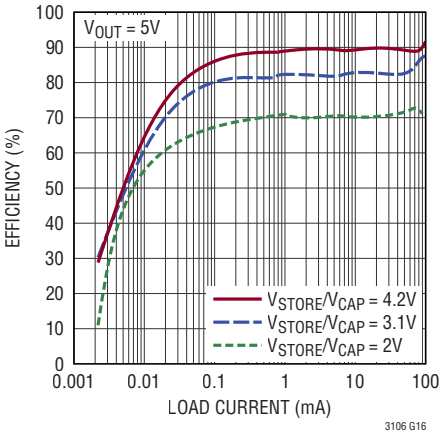
V_{STORE}/V_{CAP} Efficiency vs Load Current



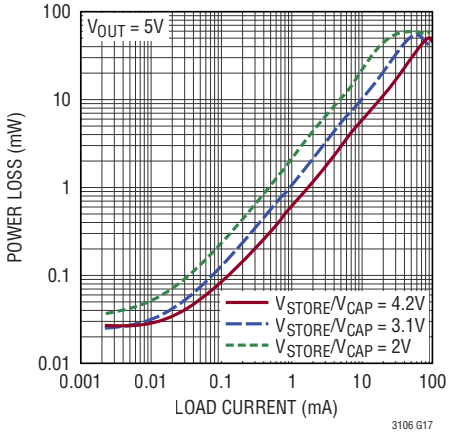
V_{STORE}/V_{CAP} Power Loss vs Load Current



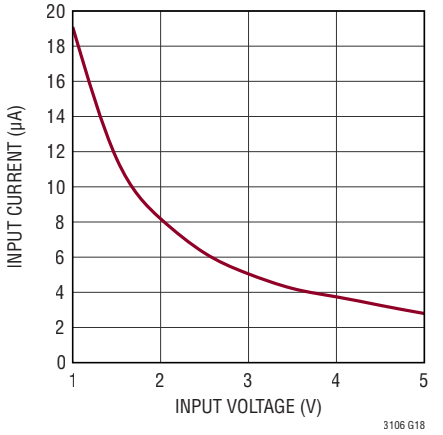
V_{STORE}/V_{CAP} Efficiency vs Load Current



V_{STORE}/V_{CAP} Power Loss vs Load Current

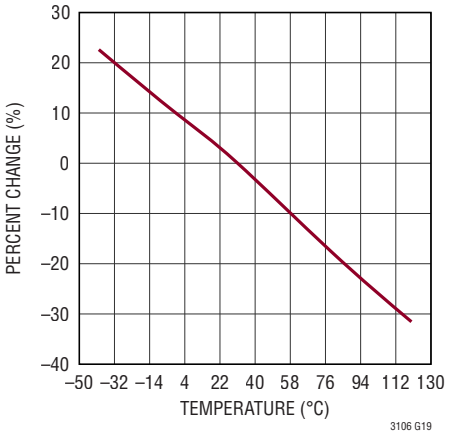


No Load Input Current vs Input Voltage

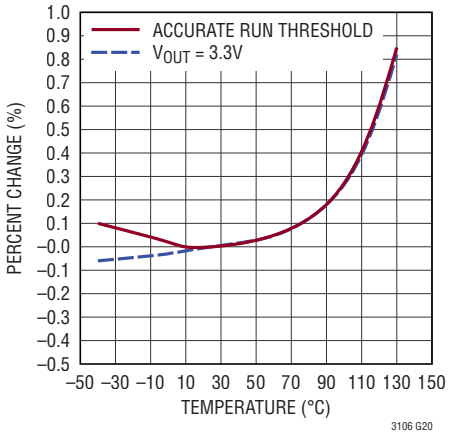


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

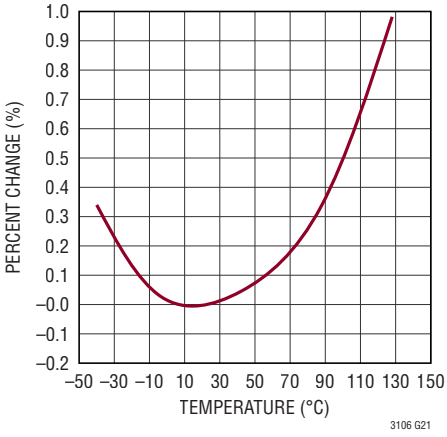
Normalized RUN Threshold vs Temperature



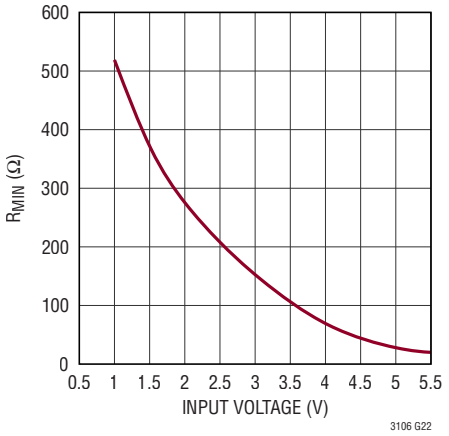
Normalized V_{OUT}, Accurate RUN_{TH} vs Temperature



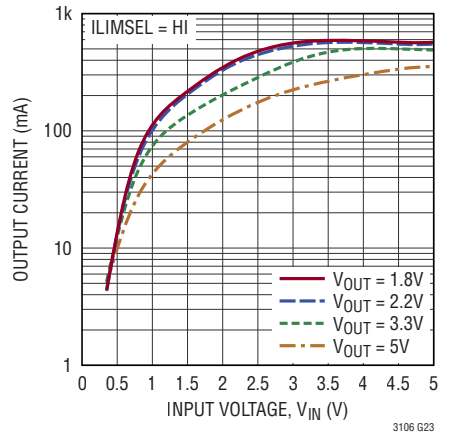
Normalized Input Voltage UVLO vs Temperature



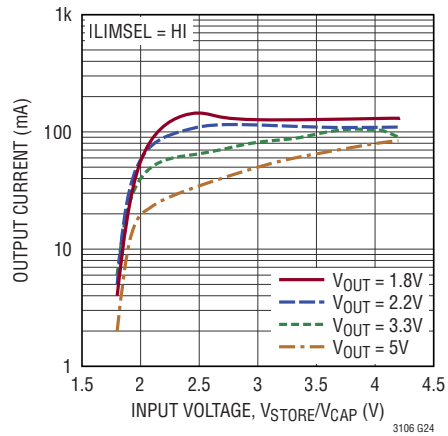
Start-Up Into Resistive Load L = 10µH



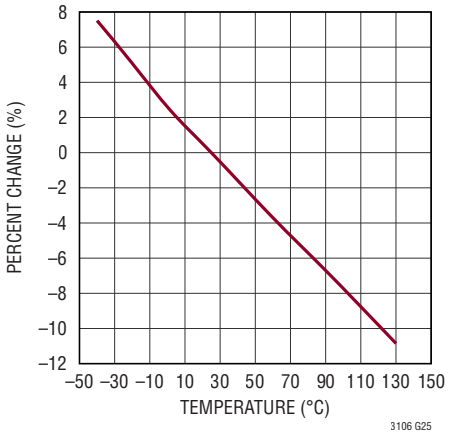
Maximum Output Current vs Input Voltage (V_{IN})



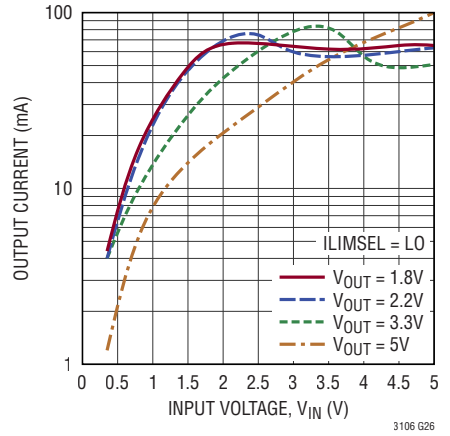
Maximum Output Current vs Input Voltage (V_{STORE}/V_{CAP})



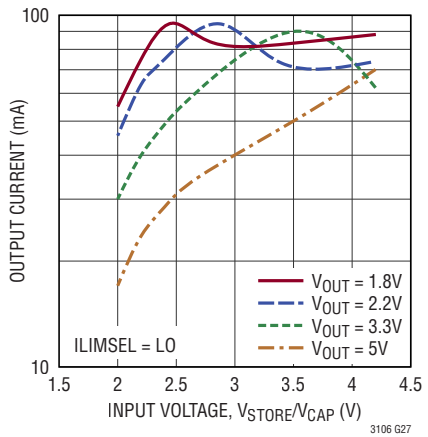
Normalized V_{IN} Start-Up Voltage vs Temperature



Maximum Output Current vs Input Voltage (V_{IN})

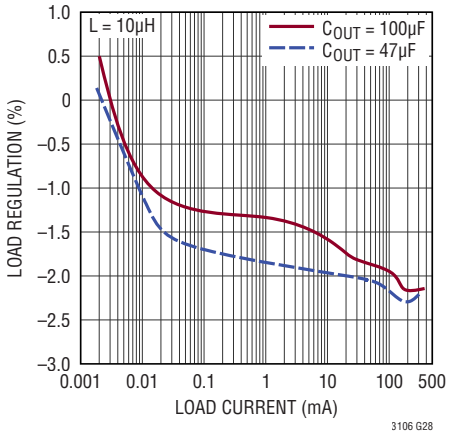


Maximum Output Current vs Input Voltage (V_{STORE}/V_{CAP})

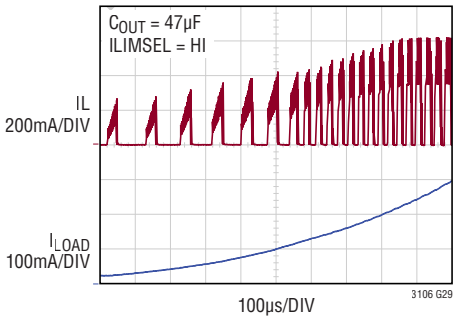


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

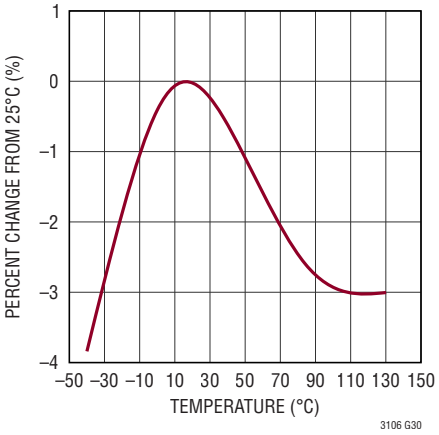
Normalized Output Voltage Regulation vs Load Current



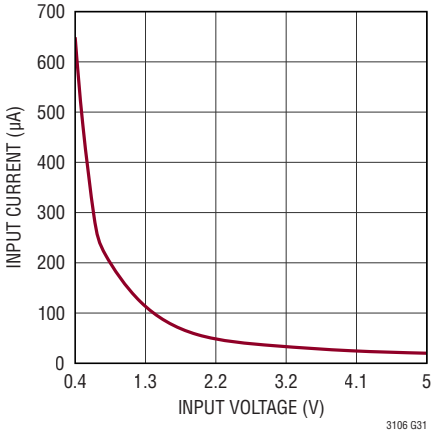
Inductor Current vs Load Current



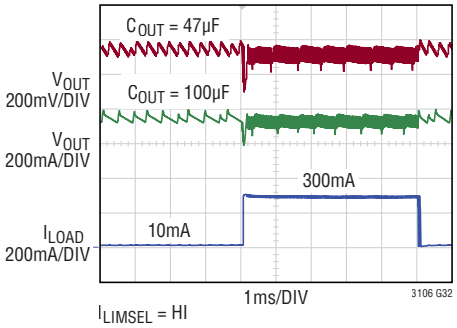
Normalized MPP Output vs Temperature



No Load Input Current vs Input Voltage, MPP Enabled

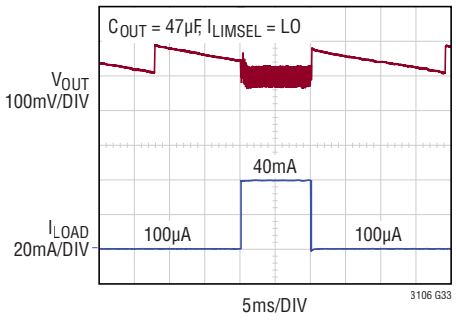


$5V_{IN}$ to $3.3V_{OUT}$ Load Step 10mA to 300mA

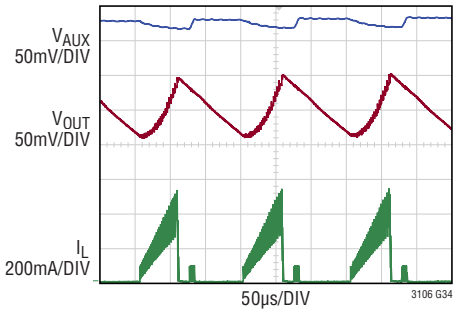


ILIMSEL = HI

$5V_{IN}$ to $3.3V_{OUT}$ Load Step 100µA to 40mA

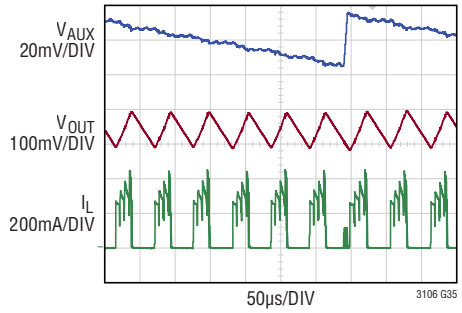


Boost Mode at V_{IN} = 1.5V V_{OUT} = 3.3V, 100mA



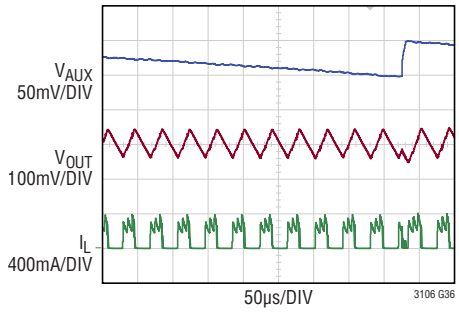
L = 10µH
C_{OUT} = 47µF
I_{LIMSEL} = HI

Buck-Boost Mode at V_{IN} = 3.5V V_{OUT} = 3.3V 100mA



L = 10µH
C_{OUT} = 47µF
I_{LIMSEL} = HI

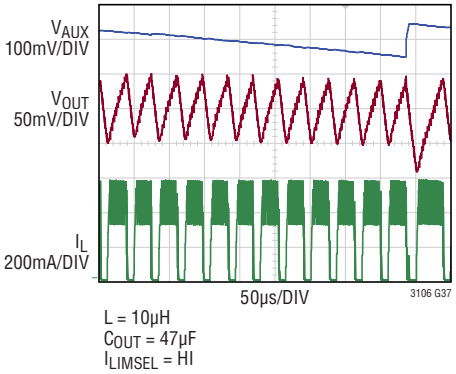
Buck Mode at V_{IN} = 4.3V V_{OUT} = 3.3V, 100mA



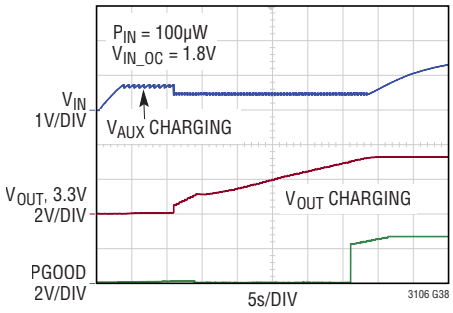
L = 10µH
C_{OUT} = 47µF
I_{LIMSEL} = HI

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

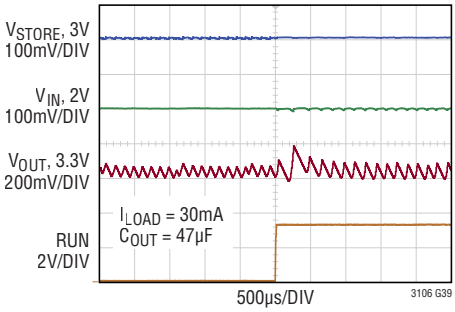
Buck Mode at V_{IN} = 5V V_{OUT} = 3.3V, 300mA



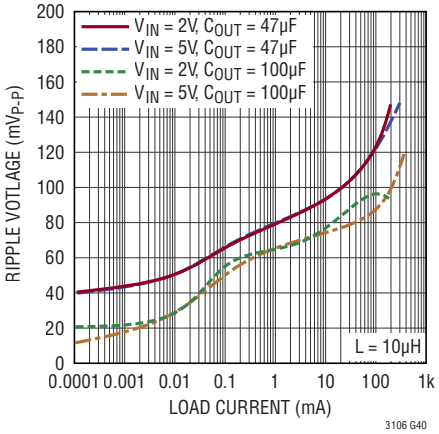
No-Load Start-Up from Low Power Source V_{STORE} = 0V, V_{IN} = RUN



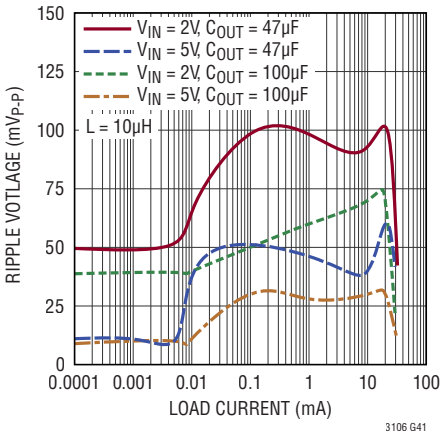
V_{STORE} to V_{IN} Switchover



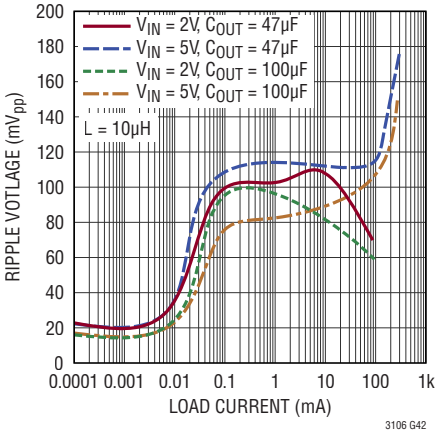
3.3V Output Voltage Ripple vs Load Current (ILIMSEL High)



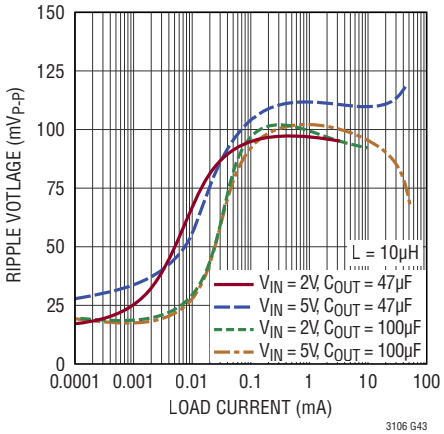
3.3V Output Voltage Ripple vs Load Current (ILIMSEL Low)



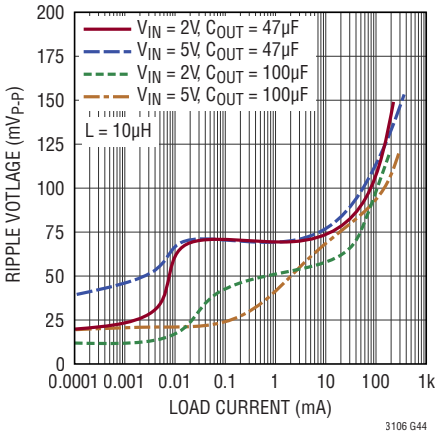
5V Output Voltage Ripple vs Load Current (ILIMSEL High)



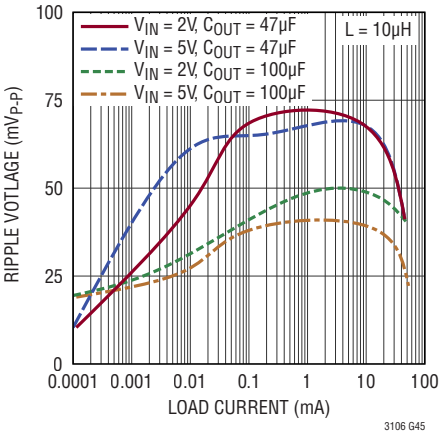
5V Output Voltage Ripple vs Load Current (ILIMSEL Low)



1.8V Output Voltage Ripple vs Load Current (ILIMSEL High)

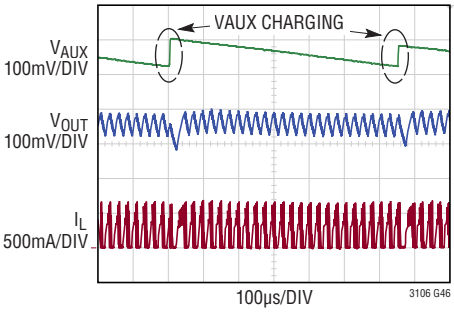


1.8V Output Voltage Ripple vs Load Current (ILIMSEL Low)



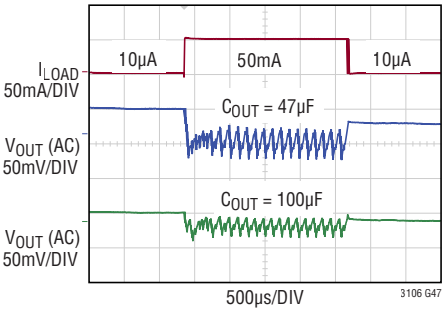
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

Output Voltage Ripple 5V V_{IN}, 3.3V V_{OUT} 200mA



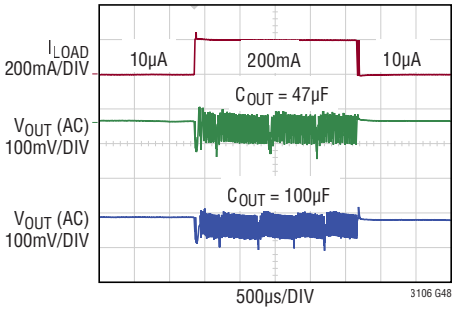
I_{LIMSEL} = HIGH
C_{OUT} = 100µF

5V V_{IN} to 1.8V V_{OUT} Load Step 10µA to 50mA



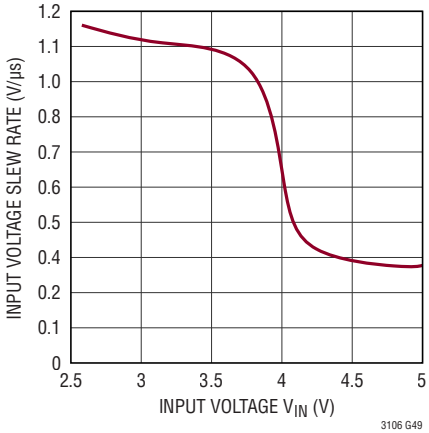
I_{LIMSEL} = LOW

5V V_{IN} to 1.8V V_{OUT} Load Step 10µA to 200mA

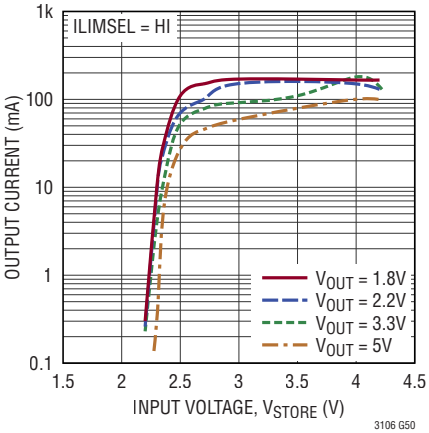


I_{LIMSEL} = HIGH

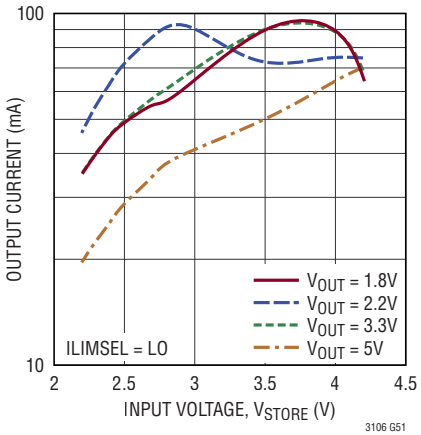
Maximum Slew Rate vs Input Voltage



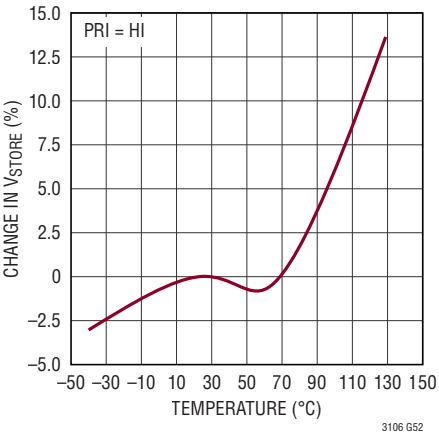
Maximum Output Current vs Input Voltage (V_{STORE} Shelf Mode)



Maximum Output Current vs Input Voltage (V_{STORE} Shelf Mode)



Normalized Average Minimum Operating V_{STORE} vs Temperature



PIN FUNCTIONS (QFN/TSSOP)

NC (Pin 1/Pin 4): No Connect. Not electrically connected internally. May be connected to PCB ground or left floating.

V_{OUT} (Pin 2/Pin 3): Programmable Output Voltage. Connect at least a 22µF low ESR capacitor to GND as close to the part as possible. Capacitor size may increase depending on output voltage ripple and load current requirements.

V_{AUX} (Pin 3/Pin 5): Auxiliary Voltage. This pin is a generated voltage rail used to power internal circuitry only. Connect a 2.2µF minimum ceramic capacitor to GND as close to the part as possible. Larger capacitors may also be used depending on the application start-up requirements. If larger capacitors are used maintain a minimum 10:1 V_{OUT} to V_{AUX} capacitor value ratio.

V_{CC} (Pin 4/Pin 6): Internal Supply Rail. Do not load. Used for powering internal circuitry and biasing the programming inputs only. Decouple with a 0.1µF ceramic capacitor placed as close to the part as possible.

OS1, OS2 (Pins 5, 6/Pins 7, 8): V_{OUT} Select Programming Inputs. Connect the pins to ground or V_{CC} to program the output voltage according to Table 1.

PGOOD (Pin 7/Pin 9): Power Good Indicator. Open-drain output that is pulled to ground if V_{OUT} falls 8% below its programmed voltage. The PGOOD pin is not actively pulled to ground in shutdown. If pulled high the PGOOD pin will float high and will not be valid until 3.5ms after the part is enabled.

MPP (Pin 8/Pin 10): Set Point Input for Maximum Power Point Control. Connect a resistor from MPP to GND to program the activation point for the MPP comparator. To disable the MPP circuit, connect MPP directly to the V_{CC} pin.

SS1, SS2 (Pins 10, 9/Pins 12, 11): V_{STORE} Select Programming Inputs. Connect the pins to ground or V_{CC} to program the V_{STORE} voltage range according to Table 2. Only valid if PRI is low. Tie both to ground if PRI is high.

PRI (Pin 11/Pin 13): Primary Battery Enable Input. Tie to V_{CC} to enable the use of a non-rechargeable primary battery and to disable V_{STORE} pin charge capability. SS[1:2] are ignored if PRI = V_{CC}. Tie to GND to use a secondary battery and enable charging.

ILIMSEL (Pin 12/Pin 14): Current Limit Input Select. Tie to GND to disable the automatic power adjust feature and operate at the lowest peak current or tie to V_{CC} to enable the power adjust feature for operation at higher peak inductor currents.

RUN (Pin 13/Pin 15): Input to enable the IC and to set custom V_{IN} undervoltage thresholds. There are two thresholds on the RUN pin. A voltage greater than 400mV (typ) will enable certain internal IC functions. The accurate RUN threshold is set at 600mV and enables V_{IN} as an input. Tie this pin to V_{IN} or connect to an external divider from V_{IN} to provide an accurate undervoltage threshold. Tie to >600mV to allow sub-600mV operation from V_{IN}. The accurate RUN pin threshold has 50mV of hysteresis provided internally.

ENVSTR (Pin 14/Pin 16): Enable V_{STORE} Input. Tie to V_{STORE} to enable V_{STORE} as a backup input. Grounding this pin disables the use of V_{STORE} as a backup input source.

GND (Pin 15/Pin 17 and Pin 21 Exposed Pad): Connect to PCB ground for internal electrical ground connection and for rated thermal performance.

V_{IN} (Pin 16/Pin 18): Main Supply Input. Decouple with minimum 10µF capacitor. Input capacitor value may be significantly larger (>100µF) depending on source impedance and load requirements. If larger capacitors are used a 1µF min ceramic capacitor should be also placed as close to the V_{IN} pin as possible.

SW1, SW2 (Pins 18, 17/Pins 20, 19): Buck-Boost Converter Switch Pins. Connect inductor between SW1 and SW2 pins.

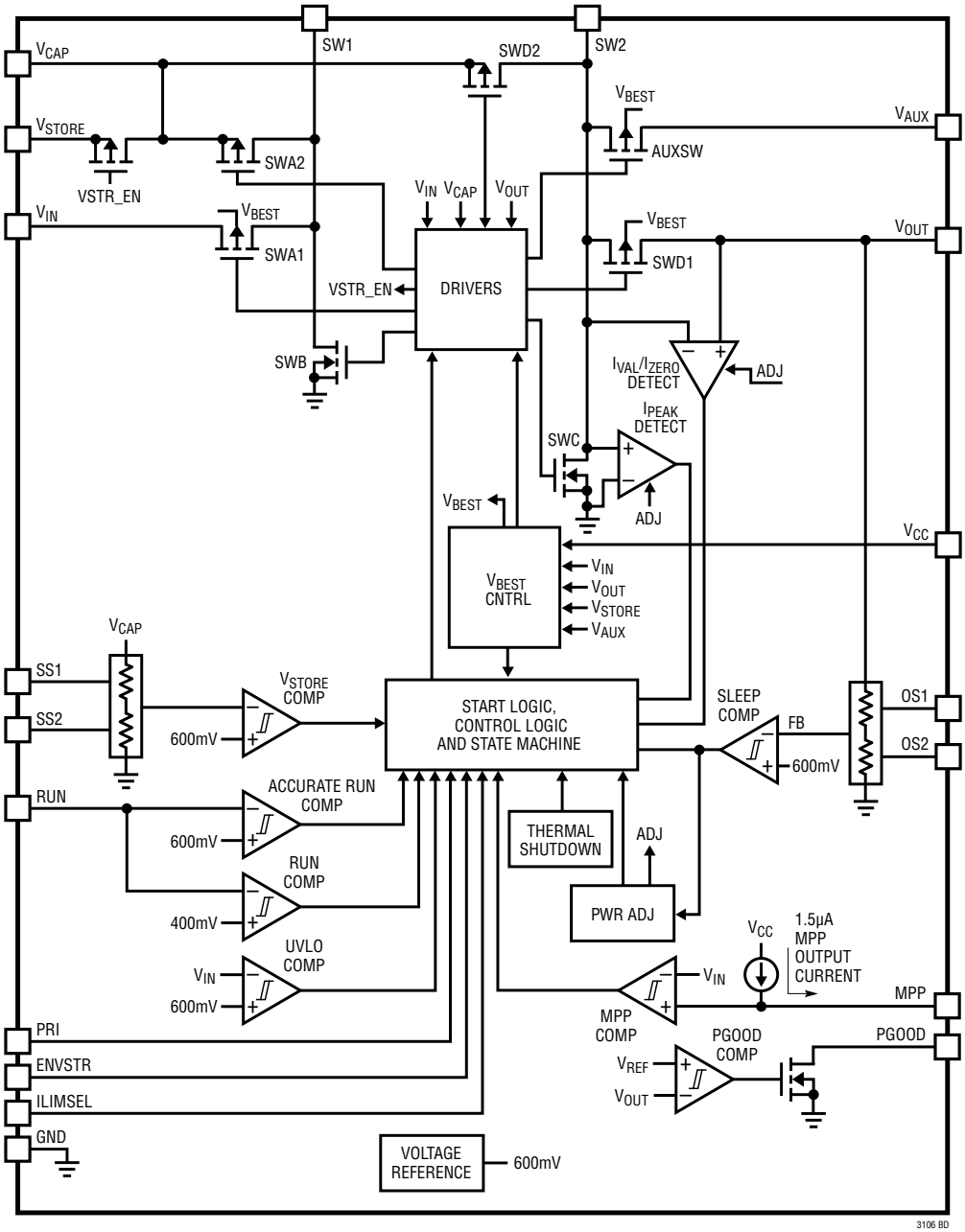
V_{STORE} (Pin 19/Pin 1): Secondary Supply Input. A primary or secondary rechargeable battery may be connected from this pin to GND to power the system in the event the input voltage is lost. When PRI pin is low, current will be sourced from this pin to trickle charge the storage element up to the maximum selected storage voltage. When PRI is high no charging will occur. Tie this pin to V_{CAP} for primary

PIN FUNCTIONS (QFN/TSSOP)

or high capacity secondary battery applications. For low capacity sources only tie V_{STORE} directly to the battery. Tie to GND if unused.

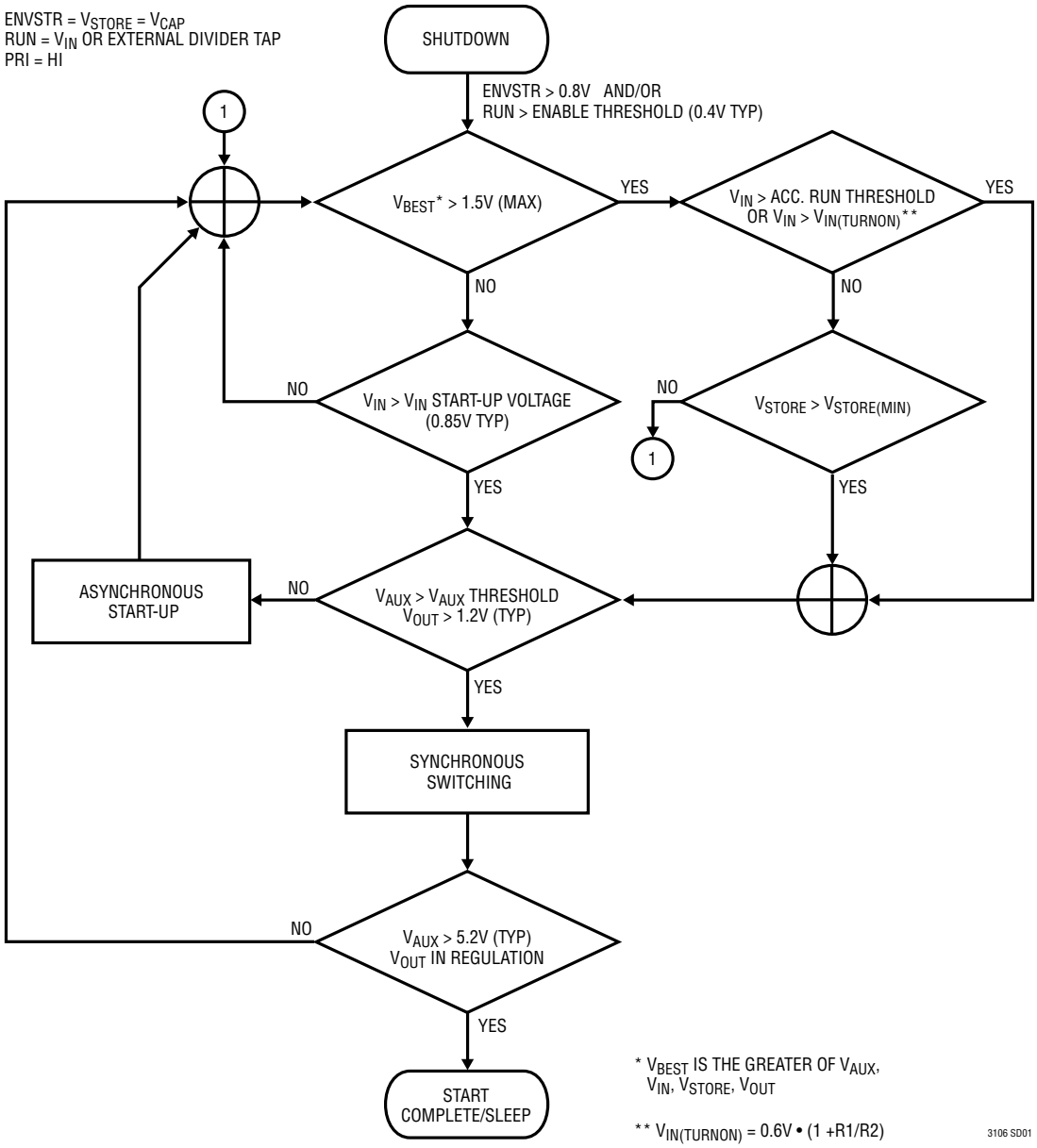
V_{CAP} (Pin 20/Pin 2): V_{STORE} Isolation Pin. Isolates V_{STORE} from the decoupling capacitor for low capacity backup batteries. Tie to V_{STORE} for primary or high capacity secondary battery applications. Decouple to GND with a capacitor large enough to handle the peak load current from V_{STORE}. Tie to GND if unused.

BLOCK DIAGRAM



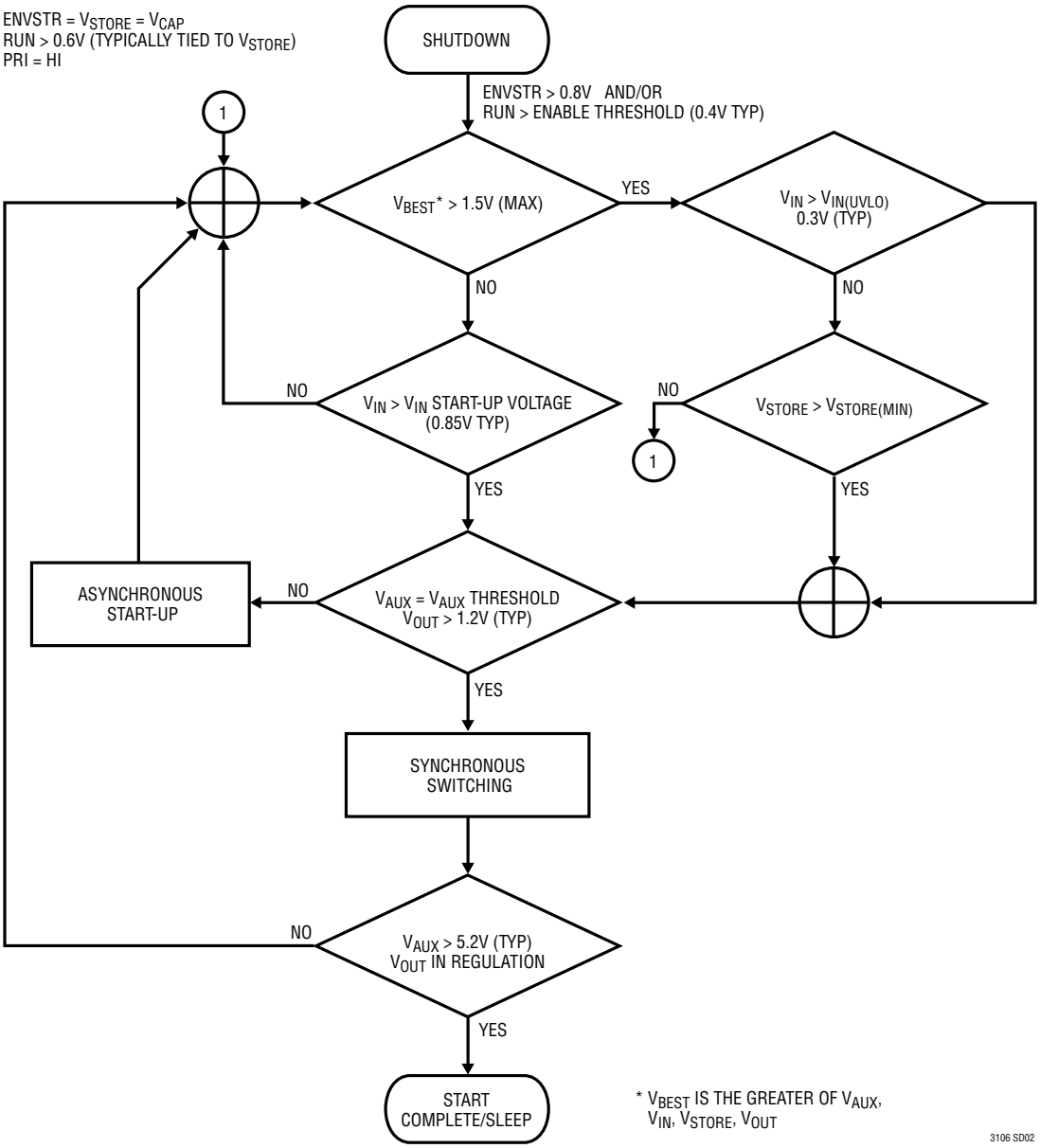
OPERATION

Simplified Operational Flow Chart Using Accurate RUN with Primary Battery Backup



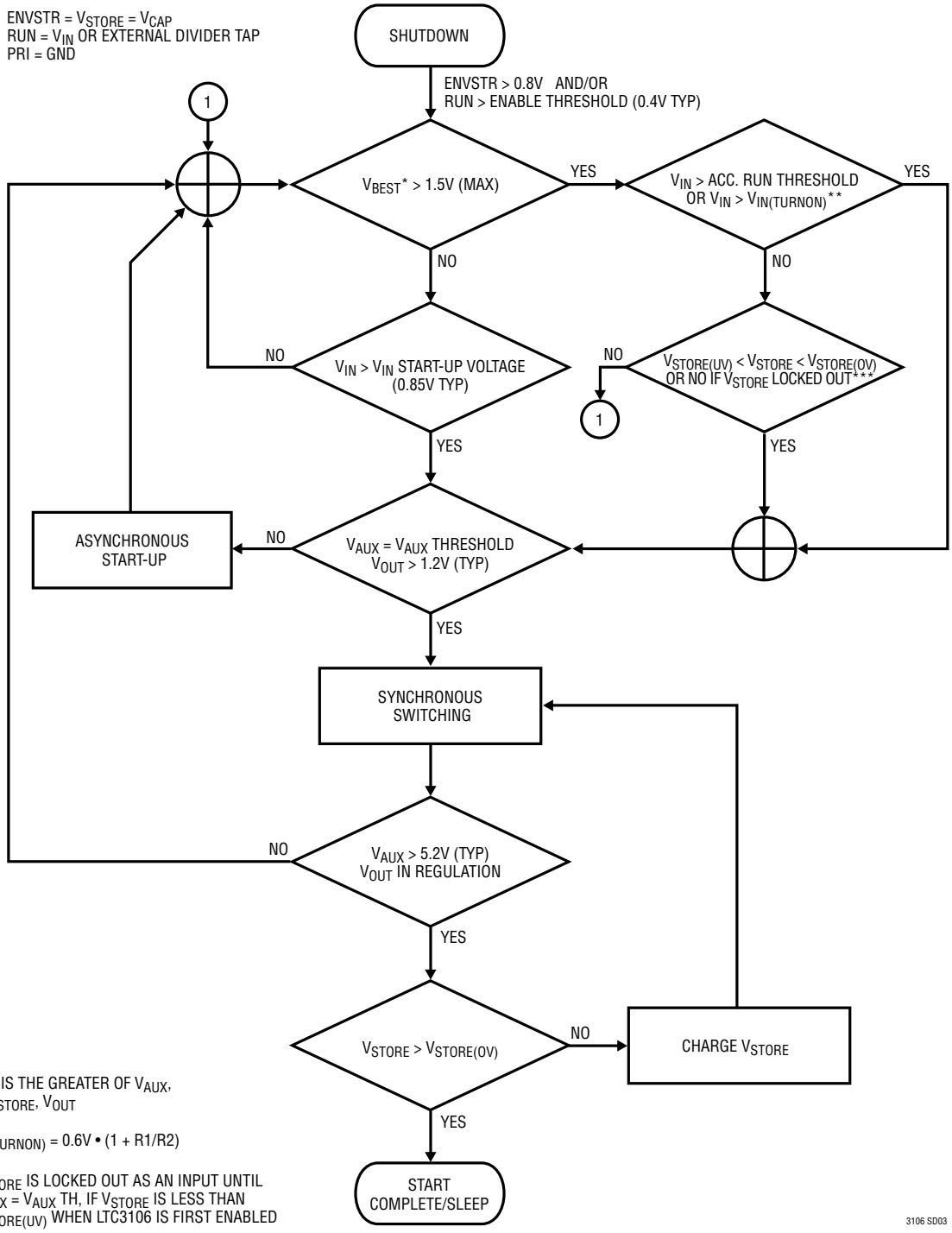
OPERATION

Simplified Operational Flow Chart Using V_{IN} UVLO with Primary Battery Backup



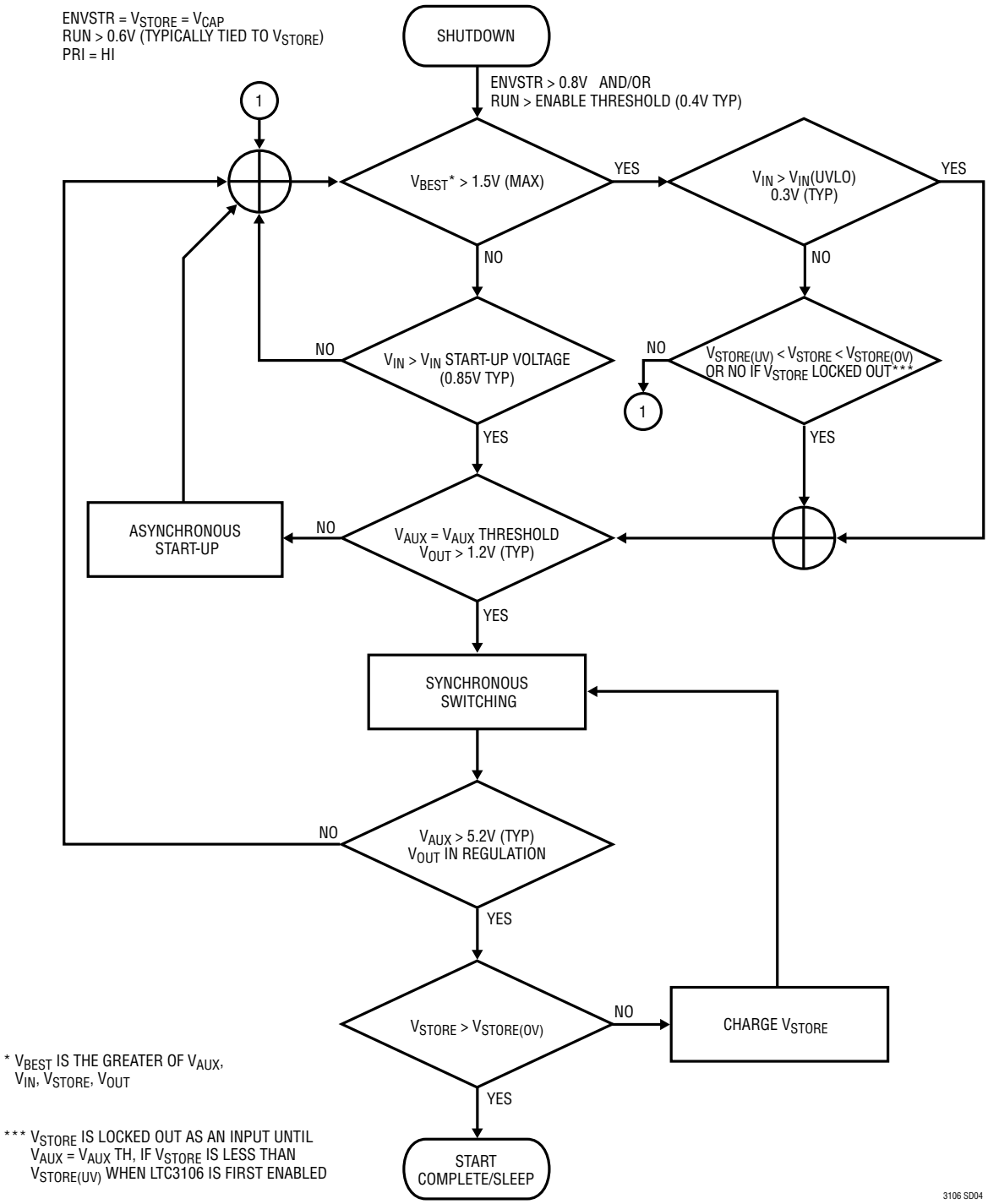
OPERATION

Simplified Operational Flow Chart Using Accurate RUN with Rechargeable Battery Backup



OPERATION

Simplified Operational Flow Chart Using V_{IN} UVLO with Rechargeable Battery Backup



OPERATION

Introduction

The LTC3106 is a high performance two input, synchronous buck-boost converter with low quiescent current over a wide input voltage range (refer to graph G18). The PowerPath control architecture allows the use of a single inductor to generate a user selectable fixed regulated output voltage through seamless transition between either of the two power inputs. If input power is available (V_{IN}) or the backup battery is present (V_{STORE}), the buck-boost regulator will operate from V_{IN} providing up to 300mA to the load. Should the V_{IN} source become unavailable the regulator will select V_{STORE}/V_{CAP} as its input delivering up to 90mA to the load. If a rechargeable battery is used as the backup source, a low current recharge power path is also provided allowing use of excess input energy to charge the backup source if the output voltage is in regulation. User selectable upper and lower thresholds are available to handle multiple battery chemistries and to protect the battery from overcharge/deep discharge. Charging can be externally disabled using the PRI pin for use of a primary battery as the backup source.

V_{IN}

The main input voltage, V_{IN}, can be configured to operate over an extended voltage range to accommodate multiple power source types including but not limited to high impedance sources. An accurate RUN pin allows predictable regulator turn-on at a specified input voltage. Optional maximum power point control (MPPC) capability is also integrated into the LTC3106. Either can be used to ensure maximum power extraction from non-ideal power sources.

V_{STORE}/V_{CAP}

A backup source can be tied to V_{STORE}. As shown in the Block Diagram, V_{STORE} can be isolated from V_{CAP} by the isolation switch for near zero current draw requirements and lower output current levels. When using the isolation feature the ILIMSEL pin should be tied to ground due to the increased series resistance the isolation switch adds.

For typical secondary and primary battery backup applications isolation is not needed, V_{STORE} and V_{CAP} should be shorted together. In this configuration the ILIMSEL feature can be used to increase output current to higher. Both configurations are shown in Figure 1. In either configuration, V_{CAP} is always enabled at start-up if ENVSTR is high to determine if V_{CAP} is within the programmed voltage range. If V_{CAP} is below the lower threshold it is latched off during start-up to minimize quiescent current draw from V_{CAP}. Since the voltage on V_{CAP} is continually monitored a very small 100nA typical quiescent current will persist with V_{CAP} in shutdown (ENVSTR tied to GND).

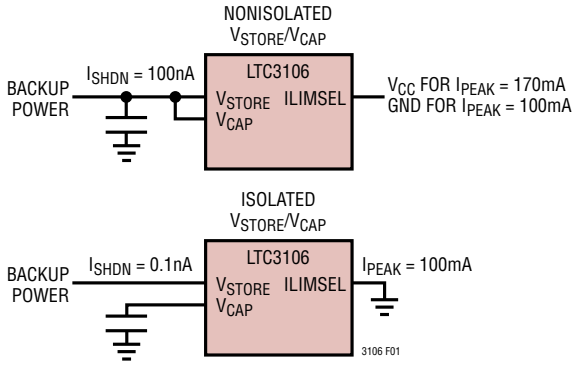


Figure 1. V_{STORE}/V_{CAP} Configurations

Shutdown

Either input source can be enabled independently or together. Bring ENVSTR below the worst-case logic threshold of 0.3V to disable V_{STORE}/V_{CAP} as input or output if charging is enabled (PRI low). Bringing ENVSTR below 0.3V will also turn off the isolation switch if the LTC3106 is configured to isolate V_{STORE} from V_{CAP}.

A low voltage logic input on the RUN pin enables some circuit functions at 400mV typical while an accurate comparator enables V_{IN} as an input. To disable V_{IN} as an input, RUN must be below the accurate RUN threshold of 600mV (typ). To put the LTC3106 in shutdown mode the ENVSTR pin must be below 0.3V and the RUN pin must be brought below the worst-case low level logic threshold of 150mV.

Accurate RUN Pin

If RUN is brought below the 500mV accurate comparator falling threshold, the buck-boost converter will inhibit switching from V_{IN}. Certain control circuits will remain powered unless RUN is brought below its low level logic threshold of 400mV. A small amount of current draw on V_{IN} will still remain in this mode.

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With the addition of an optional resistor divider as shown in Figure 2, the RUN pin can be used to establish a user programmable turn-on and turn-off threshold. This feature can be utilized to set an application specific V_{IN} undervoltage threshold or to operate the converter from V_{IN} in a hiccup mode from very low power sources. If V_{STORE}/V_{CAP} is available as a backup power source, V_{IN} input power priority over V_{STORE}/V_{CAP} is only given if the RUN pin is above the accurate threshold.

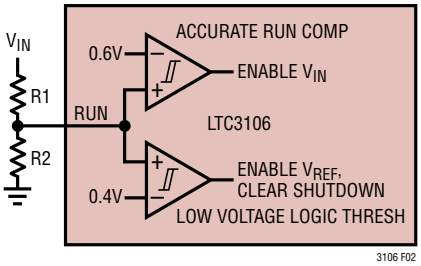

Figure 2. Accurate RUN Pin Comparator

The V_{IN} input is enabled when the voltage on RUN exceeds 0.6V (nominal). Therefore, the turn-on voltage threshold on V_{IN} can be set externally and is given by:

$$V_{IN(TURNON)} = 0.6V \bullet \left(1 + \frac{R1}{R2}\right)$$

The RUN comparator includes a built-in hysteresis of approximately 100mV, so that the typical turn-off threshold will be;

$$V_{IN(TURNOFF)} = 0.5V \bullet \left(1 + \frac{R1}{R2}\right)$$

V_{AUX}

V_{AUX} is charged up during start-up and is also refreshed as necessary from V_{IN} or V_{STORE}/V_{CAP} during normal operation. Once V_{AUX} is fully charged or greater than either input voltage source it will power the LTC3106 active circuitry. The V_{AUX} pin should be bypassed with a minimum 2.2µF capacitor. Once V_{AUX} reaches 5.2V (typ), V_{OUT} is allowed to start charging. Although minimized by design techniques the single inductor architecture allows some parasitic asynchronous charging of V_{AUX}. An internal shunt regulator limits the maximum voltage on V_{AUX} to 5.5V typical and shunts any excess current to V_{OUT}. When the V_{AUX} voltage drops to 5.1V typical, input power is briefly diverted to recharge V_{AUX}.

V_{OUT}

The main output voltage on V_{OUT} can be powered from either input power source and is user programmed to one of four regulated voltages using the voltage select pins OS1 and OS2, according to Table 1. It is recommended that OS1 and OS2 be tied to either ground or V_{CC}.

Table 1. Output Voltage Selection

OS1	OS2	OUTPUT VOLTAGE
0	0	1.8V
0	V_{CC}	2.2V
V_{CC}	0	3.3V
V_{CC}	V_{CC}	5V

V_{CC}

An internal decision circuit determines the voltage on the V_{CC} pin. V_{CC} is the highest voltage of either V_{IN}, V_{CAP}, V_{OUT} or V_{AUX}. Although the V_{CC} decision circuit is always active, when start-up is complete during normal operation V_{AUX} will equal V_{CC}. V_{CC} should be decoupled with a 0.1µF capacitor placed as close as possible to the V_{CC} pin. V_{CC} is not designed to source or sink current externally. V_{CC} may be used to terminate the LTC3106 logic inputs but should not otherwise be externally loaded.

High Capacity Secondary Battery Backup

Short V_{STORE} to V_{CAP} for high capacity (>5mAh) backup power sources such as rechargeable lithium coin cell batteries, or primary batteries as shown in Figure 3. To accommodate a variety of battery chemistries and maximum voltages the V_{STORE}/V_{CAP} over and undervoltage thresholds are user programmed to one of four voltage ranges using the V_{STORE}/V_{CAP} select pins SS1 and SS2, according to Table 2.

Table 2. V_{STORE} Voltage Selection

PRI	SS1	SS2	V_{STORE}/V_{CAP} OV	V_{STORE}/V_{CAP} UV	BATTERY TYPE
0	0	0	4V	2.78V	Li Carbon
0	0	V_{CC}	2.9V	1.9V	2x Rechargeable NiMH
0	V_{CC}	0	3V	2.15V	Rechargeable Li Coin Cell
0	V_{CC}	V_{CC}	4V	3V	Li Polymer/Graphite
V_{CC}	0	0	4.2V	2.1V	Primary, Non-Rechargeable

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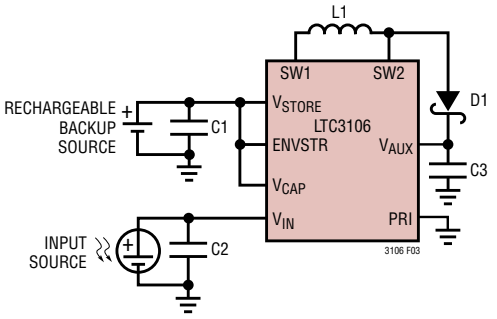

Figure 3. High Capacity Battery Configuration (Shown with V_{STORE} Enabled)

If secondary battery charging is enabled (PRI = GND) with both the output and V_{AUX} voltages in regulation, available input power will be diverted to V_{STORE}/V_{CAP} to trickle charge the backup power source with a 30mA typical current limit. Overcharging of the input source is prevented by the upper limit threshold setting.

Figures 3 and 4 show an additional Schottky diode (D1) from SW2 to V_{AUX}. When charging is enabled (PRI = GND) the addition of a Schottky diode from SW2 to V_{AUX} is necessary to prevent a V_{OUT} regulation error caused by the small parasitic output current resulting from the LTC3106 charging the secondary battery on V_{STORE}/V_{CAP}. The additional diode allows for some inrush current to the V_{AUX} capacitor C3 from either input source that would have otherwise been blocked by the AUXSW. Figure 5 shows an alternate Schottky diode configuration with two additional external components, Q1 and C4, that will still eliminate the V_{OUT} regulation error but will also significantly reduce the inrush current.

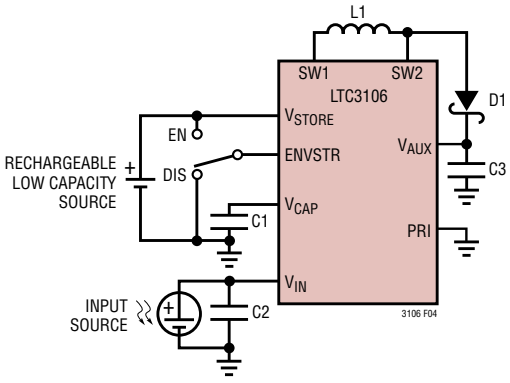

Figure 4. Low Capacity Battery Configuration (Shown with V_{STORE} Disabled, ENVSTR Tied to Ground)

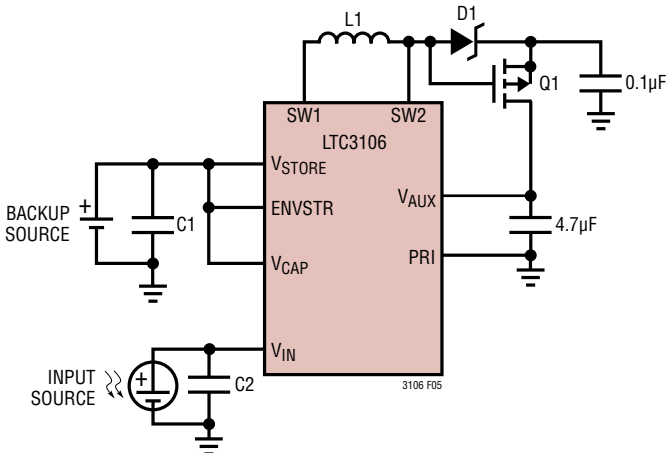

Figure 5. Rechargeable Battery Configuration with Inrush Current Limiting

Low Capacity Secondary Battery and True Isolation

For very low capacity batteries an isolation switch between V_{STORE} and V_{CAP} provides for true input source isolation and near zero current draw (<1nA) on V_{STORE}. As shown in Figure 4, simply connect V_{CAP} to a bulk capacitor and V_{STORE} to the isolated source. Tie ENVSTR to ground to isolate V_{STORE}. Although adequate for most low capacity sources such as solid state or small Li-Ion Polymer batteries, the current available to the output from V_{STORE} in this configuration will be reduced. To enable V_{STORE} as an input and prevent a significant increase in the quiescent current, it is recommended that ENVSTR terminate to V_{STORE} or to a voltage greater than V_{STORE}.

Primary Battery

The LTC3106 PRI input allows the user to disable secondary battery features such as trickle charging on V_{STORE} so that a primary battery may be used in the absence of sufficient power from the harvested source on V_{IN}. The SW2 to V_{AUX} Schottky diode is NOT required or recommended with the primary function enabled. With PRI tied to V_{CC}, the V_{STORE} input voltage range ignores the state of the SS1 and SS2 pins and operates over the wide voltage range of 2.1V to 4.3V. To use the highest peak current capability V_{STORE} should be tied to V_{CAP} in this configuration. To start the LTC3106 from V_{STORE}/V_{CAP}, V_{STORE}/V_{CAP} must be greater than 2.1V nominally. During an output short (V_{OUT} < 1.1V) a small V_{STORE} reverse current of 20µA (typical) will be

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present. If an extended duration output short is expected, protection for the primary battery should be considered.

Start-Up

The LTC3106 will start up from either input voltage source but gives priority to V_{IN}. The AUX output is initially charged with the synchronous rectifiers disabled. Once V_{AUX} has reached its terminal voltage the output voltage is then also charged asynchronously until V_{OUT} reaches approximately 1.2V. The converter then leaves the asynchronous mode in favor of a more efficient synchronous start-up mode until V_{OUT} is in regulation and the part enters normal operation.

It is normal for the output voltage to rise as V_{AUX} is charging. The AUXSW switch and the SWDI switch are in parallel so even when switched off there is still some asynchronous body diode conduction to the output. The rate at which this occurs is related to the V_{AUX}/V_{OUT} output capacitor ratio and operating conditions at start-up (i.e., any static load on V_{OUT}). A minimum 10:1 ratio of V_{OUT} to V_{AUX} cap is recommended to allow for proper start-up.

Starting from Very Low Current Input Sources

Many solar cells that are optimized for indoor use have very low available power at low light levels and therefore very low output current, often less than 100µA at 200Lux. If the LTC3106 is to start up using only a weak source on V_{IN} and with no back up battery on V_{STORE} the input capacitance must be sized larger than that for normal operation. Although dependent on the specific operating conditions for the application, in general, starting from low current sources on V_{IN} at low light levels alone will require larger input capacitances than those calculated using the C_{VIN} equation in the V_{IN} and V_{OUT} Capacitor Selection section. For example if the LTC3106 application in Figure 14 needs to start from the AM-1454 solar cell without the benefit of a battery on V_{STORE}, the required input capacitance increases from 470µF to 2.2mF minimum.

If a battery is connected to V_{STORE} but is disabled by bringing ENVSTR low and is therefore not used to start the LTC3106, the input source on V_{IN} needs to have an output current equal to or greater than 100µA (typ) regardless of the input capacitor size for the internal V_{CC} decision circuit to run properly during start up. If the input source has less than a 100µA capability, startup could stall until more input current is available from the source or until the V_{STORE} battery is enabled. The 100µA limitation also applies where the LTC3106's output is used to charge a battery or a large super capacitor. For typical applications where the input capacitance is greater than the output capacitance the 100µA limitation does not apply.

Operating from a Low Power V_{IN}

Controlling the minimum input voltage is essential when using high impedance or intermittent input sources. The LTC3106 has several options for V_{IN} voltage control during start-up and during normal operation.

If a valid V_{STORE} voltage exists or if V_{AUX} is in regulation, there are several LTC3106 configurations allowing accurate control at lower input voltages on V_{IN}. The accurate RUN comparator can be used to control the V_{IN} turn-on threshold at any arbitrary voltage equal to or above 600mV as discussed in the Accurate RUN Pin section of this data sheet. The 300mV UVLO on V_{IN} could also be used to maintain V_{IN} but is fixed at the 300mV threshold. If a higher sleep current can be tolerated, the MPP pin can be used to control V_{IN} at any arbitrary threshold above 300mV. These latter two methods of controlling V_{IN} are discussed in later sections of the data sheet.

Even if no other input source is present (V_{STORE}/V_{CAP} disabled, not used or too low), a crude V_{IN} comparator will control V_{IN} during start-up. If the RUN pin is tied to V_{IN} or held above the RUN enable threshold (>0.4V typ) the LTC3106 has a typical start-up voltage of 0.85V with input currents as low as 15µA or ~12µW of input power. If the source impedance is high enough to cause V_{IN} to drop below the V_{IN} comparator threshold, start-up is terminated until the input capacitance is again charged to approximately 0.85V. Operation continues in this manner until start-up is complete. Input source impedance due to the source itself or due to the input source's expected environmental conditions determine the required size of the input capacitance on V_{IN} to facilitate a successful start-up. Recommendations are presented in the Input Capacitor Selection and Typical Applications sections of this document.

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Normal Operation

When V_{AUX} is in regulation (~5.2V) and V_{OUT} is greater than 1.2V typical, the converter will enter normal operation.

Always prioritizing V_{IN} over V_{CAP}, the integrated PowerPath control circuitry provides seamless transition between input sources as needed to maintain regulation of the output voltage and to periodically recharge V_{AUX}.

An accurate comparator is used to monitor the output voltage as it continues to charge to one of the user selected fixed output voltage values. If V_{OUT} is above this voltage value no switching occurs and only quiescent current is drawn from the power source (sleep mode). When V_{OUT} drops below the fixed output voltage the LTC3106 "wakes up", switching commences, and the output capacitor is again charged. The value of the output capacitor, the load current, input source and the output voltage comparator hysteresis (~1%) all determine the number of current pulses required to pump up the output capacitor before the part returns to sleep. Normalized input and output voltages in the various modes as well as typical inductor current waveforms are shown in Figure 6. Only V_{IN} is shown but the V_{STORE}/V_{CAP} power path have the same architecture. Regions of the current waveforms where switches A and D are on provide the highest efficiency since energy is transferred directly from the input source to the output.

Boost Mode

When $V_{IN} < V_{OUT} – 300mV$, the LTC3106 operates in boost or step-up mode. Referring to Figure 6 when V_{OUT} falls below the programmed regulation voltage, switches A and C are turned on (V_{IN} is applied across the inductor) and current is ramped until I_{PEAK} is detected. When this occurs, C is turned off, D is turned on and current is delivered to the output capacitor ($V_{IN} – V_{OUT}$ is applied across the inductor). Inductor current falls when D is on, until an I_{VALLEY} is detected. Terminating at I_{VALLEY} results in an increased load current capability for a given peak current. This AC then AD switch sequence is repeated until the output is pumped above the programmed regulation voltage, a final I_{VALLEY} is detected, and the part returns to sleep mode.

Buck Mode

When $V_{IN} > V_{OUT} + 700mV$, the LTC3106 operates in buck or step-down mode. At the beginning of a buck mode cycle (Figure 6 right side) switches A and D are turned on ($V_{IN} – V_{OUT}$ is applied across the inductor), current is delivered to the output and ramped up until I_{PEAK} is detected. When this occurs, A is turned off, B is turned on and inductor current falls ($–V_{OUT}$ across the inductor) until an I_{VALLEY} is detected. This AD then BD switch sequence is repeated

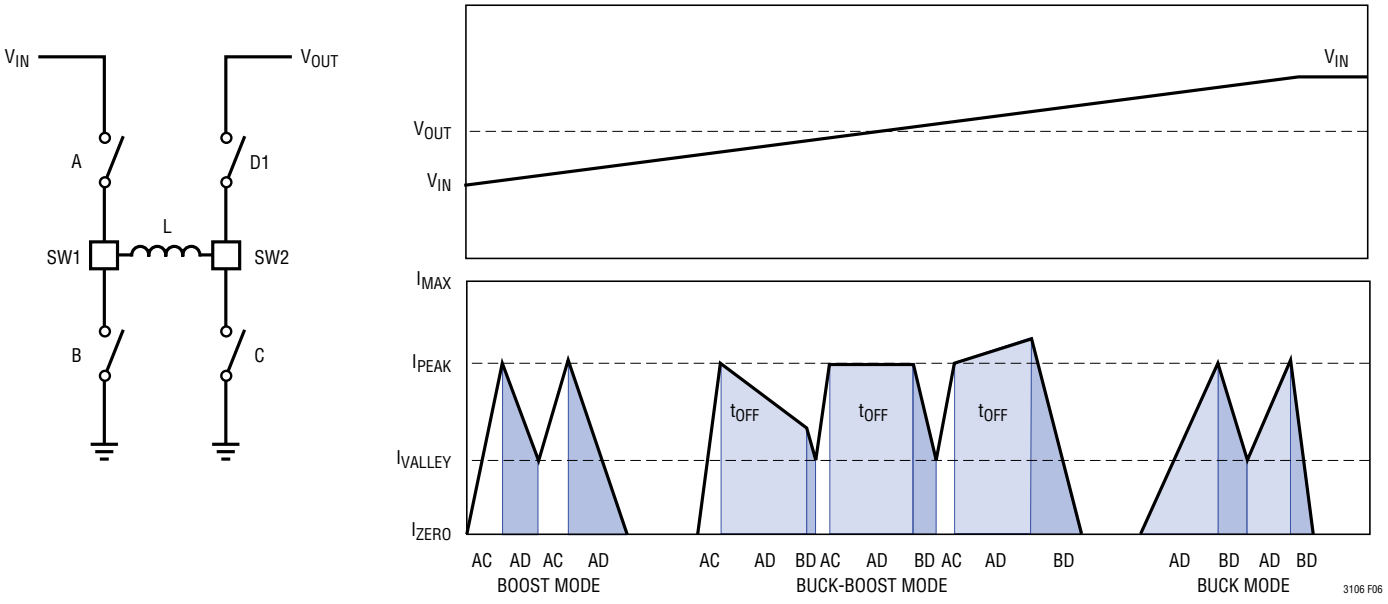

Figure 6. Operating Voltage and Current Waveforms

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until the output is pumped above its regulation voltage, a final I_{VALLEY} is detected, and the part returns to sleep mode.

Buck-Boost Mode

If (V_{OUT} – 700mV) < V_{IN} < (V_{OUT} + 300mV), the LTC3106 operates in 4-switch step-up/step-down mode. Returning to Figure 6 (center) when V_{OUT} falls below its regulation voltage, switches A and C are turned on and current is ramped until I_{PEAK} is detected. As with boost mode operation, C is then turned off, D is turned on and current is delivered to the output. When A and D are on, the inductor current slope is dependent on the relationship between V_{IN}, V_{OUT}, and the $R_{DS(ON)}$ of the switches. In 4-switch mode, a t_{OFF} timer is used to terminate the AD pulse. Once the t_{OFF} timer expires, switch A is turned off, B is turned on, inductor current is ramped down and V_{OUT} is applied across the inductor until I_{VALLEY} is detected. This sequence is repeated until the output is regulated, BD switches are turned on, and a final I_{VALLEY} is detected. Anti-cross conduction circuitry in all modes ensures the P-channel MOSFET and N-channel MOSFET switch pairs (A and B or D and C) are never turned on simultaneously.

Note all three operational modes function the same if powering from V_{STORE}/V_{CAP} when V_{IN} is not available. Simply consider V_{IN} in the preceding paragraphs as V_{STORE}/V_{CAP}.

Undervoltage Lockout (UVLO) and Very Low V_{IN} Operation

There is an undervoltage lockout (UVLO) circuit within the LTC3106 to allow very low voltage V_{IN} operation. If the LTC3106 is configured so that the RUN pin is externally driven to a voltage greater than the 600mV accurate RUN threshold, the V_{IN} UVLO function allows the input voltage to remain viable as an input source down to ~250mV. Below this threshold V_{IN} is disabled and the input source will transition to V_{STORE}/V_{CAP}, assuming V_{STORE}/V_{CAP} is within its programmed range, until V_{IN} rises above ~300mV, where input power again transitions to V_{IN}. The V_{IN} input is always given priority over the V_{STORE}/V_{CAP} input if V_{IN} is viable.

Maximum Power Point Operation

As an alternative to using an external divider on the RUN pin (or for maximum power point thresholds below the 600mV RUN pin threshold) the maximum power point control circuit allows the user to set the optimal input voltage operating point for a given power source. The MPP circuit hysteretically regulates the average V_{IN} voltage to the MPP threshold. When V_{IN} is greater than the MPP voltage, input power is taken from V_{IN} to supply the load. If the V_{IN} power source does not have enough power for the load it will decrease. When V_{IN} is less than the MPP threshold voltage the input transitions to V_{STORE}/V_{CAP} if available. V_{IN} power may then recharge the input capacitor voltage and as it rises above the MPP threshold the process repeats. V_{IN} MPP regulation is then maintained using this "burst" technique. If V_{STORE} is disabled or in undervoltage, no switching occurs until V_{IN} again rises above the MPP threshold and only quiescent current is drawn from the power source (same as sleep mode).

To set the MPP threshold a 1.5µA (typical) source current is provided at the MPP pin. An external resistor to ground allows an arbitrary MPP threshold voltage setting. See Figure 7.

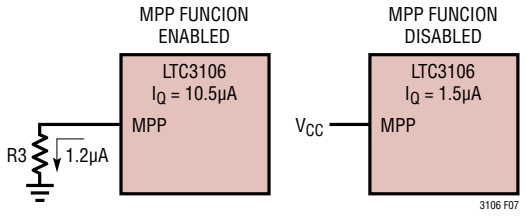

Figure 7. MPP Configurations

Note that when the MPP function is used the nominal quiescent current increases from 1.5µA (typical) to 10.5µA (typical). To disable the MPP feature and eliminate the additional I_Q, simply tie MPP to V_{CC}.

PGOOD Comparator

The LTC3106 provides an open-drain PGOOD output that pulls low if V_{OUT} falls more than 10% (typical) below its programmed value. When V_{OUT} rises to within 8% (typical) of its programmed value, the internal PGOOD pull-down

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will turn off and PGOOD will go high if an external pull-up resistor has been provided. An internal deglitch filter prevents nuisance trips of PGOOD due to short transients (<15µs typically) on V_{OUT}. Note that PGOOD can be pulled up to any voltage, as long as the absolute maximum rating of 6V is not exceeded, and as long as the maximum sink current rating is not exceeded when PGOOD is low. The PGOOD pin is not actively pulled low in shutdown. If pulled high the PGOOD pin will float high and will not be valid until 3.5ms after the part is enabled.

Power Adjust Feature

The LTC3106 ILIMSEL option enables a feature that maximizes efficiency at light load while providing increased power capability at heavy load by adjusting the peak and valley of the inductor current as a function of load. Lowering the peak inductor current for either input source at light load optimizes efficiency by reducing conduction losses in the internal MOSFET switches. As the load increases, the peak inductor current is automatically increased to a maximum of 650mA for V_{IN} and 150mA for V_{STORE}/V_{CAP}. At intermediate loads, the peak inductor current may vary from 90mA to 650mA. Figure 8 shows an example of how the inductor current changes as the load increases.

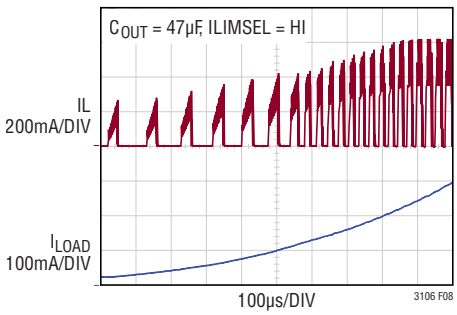

Figure 8. Inductor Current Changing as a Function of Load

The V_{OUT} capacitor should be a minimum of 47µF. A larger output capacitor can be used if lower peak to peak output voltage ripple is desired. A larger output capacitor will also improve load regulation on V_{OUT} but will result in higher peak currents than necessary at light load lowering the light load efficiency.

The valley of the inductor current is automatically adjusted as well to maintain a relatively constant inductor ripple current. This keeps the switching frequency relatively constant with load. The "burst" frequency (how often the LTC3106 delivers a burst of current pulses to the load) is determined by the internal hysteresis (output voltage ripple), the load current and the amount of output capacitance. All Burst Mode operation, or hysteretic converters, will enter the audible frequency range when the load is light enough. However, due to the low peak inductor current at light load, circuits using the LTC3106 do not typically generate any audible noise. Note that the power adjust feature is overridden by the MPP function.

To maximize efficiency for very high impedance input sources, low frequency pulsed load or low load current applications, the power adjust feature may be disabled using the ILIMSEL pin keeping the peak currents limited to 90mA. See Table 3 for ILIMSEL configurations.

Table 3. Current Limit Adjustment

ILIMSEL	V_{IN} PEAK I_{LIMIT} (mA)	V_{STORE} PEAK I_{LIMIT} (mA)
0	100	100
V_{CC}	650	170

Energy Storage

Harvested energy can be stored on the input capacitor, the output capacitor or if enabled, on the backup storage element on V_{STORE}. The wide input voltage range takes advantage of the fact that energy storage on the input capacitor is proportional to the square of the capacitor voltage. After the output voltage is brought into regulation any excess energy is stored on the input capacitor and its voltage increases. If V_{STORE} charging is enabled (PRI pin grounded) excess energy will first be used to recharge the backup power source before storing energy on the input capacitor.

APPLICATIONS INFORMATION

A standard application circuit for the LTC3106 is shown on the front page of this data sheet, although the LTC3106 can be configured to work from a variety of alternative energy and backup battery sources. The appropriate selection of external components is dependent upon the required performance of the IC in each particular application. This section of the data sheet provides some basic guidelines and considerations to aid in the selection of external components and the design of the applications circuit, as well as a few other application circuit examples.

V_{STORE}/V_{CAP} Capacitor Selection

If there is insufficient power on V_{IN}, the V_{STORE}/V_{CAP} input carries the full inductor current and provides power to internal control circuits in the IC. To minimize V_{STORE} voltage ripple and ensure proper operation of the IC, a low ESR bypass capacitor with a value of at least 4.7µF should be located as close to the V_{CAP} pin as possible. The traces connecting this capacitor to V_{CAP} and the ground plane should be made as short as possible. In cases where the series resistance of the battery is high or the LTC3106 is powered by long traces or leads, a larger value bulk input capacitor may be required and is generally recommended. In such applications a 47µF to 100µF low ESR electrolytic capacitor in parallel with a 1µF ceramic capacitor generally yields a high performance, low cost solution. Note that if there is sufficient power on V_{IN} only capacitor leakage current and shutdown current will be drawn from the V_{STORE}/V_{CAP} source. When using the Shelf Mode feature, the V_{STORE} pin should be isolated from the V_{CAP} pin and no capacitor is needed on the V_{STORE} pin. Instead the bypass capacitor should be located only on the V_{CAP} pin.

V_{IN} and V_{OUT} Capacitor Selection

The LTC3106 has no maximum capacitance limitation on V_{IN} or V_{OUT} but there is a slew rate limitation on V_{IN} that drives the need for a minimum input capacitance. Refer to the plot of Maximum Slew Rate vs Input Voltage in the Typical Performance Characteristics section. For general applications where the input source has a low impedance and relatively high output power, a minimum 22µF ceramic capacitor is recommended between V_{IN} and GND. In applications where the input has a high impedance and may be intermittent, such as in energy harvesting applications, the total V_{IN} capacitor value will be selected to optimize the use of the harvested source and will typically be greater than 100µF.

In energy harvesting applications the V_{IN} and V_{OUT} capacitors should be selected to optimize the use of the harvested source. Input capacitor selection is highly important if the LTC3106 must start from a, high source resistance system on V_{IN}. When using bulk input capacitors that have high ESR, a small valued parallel ceramic capacitor should be placed between V_{IN} and GND as close to the converter pins as possible. After V_{AUX} and the output voltage are brought into regulation any excess energy is stored on the input capacitor and its voltage will increase. Care should be taken to ensure the open-circuit voltage of the harvested source does not exceed or is appropriately clamped to the maximum operating voltage V_{IN} and that the input capacitor is rated for that voltage.

For pulsed load applications, even low power pulsed load applications such as Eterna® BLE, ZigBee as well as other proprietary low power RF protocols, the input capacitor should be sized to store enough energy to provide output power for the duration of the load profile. If enough energy is stored so that V_{IN} does not reach the chosen falling threshold during a load transient then the V_{STORE}/V_{CAP} current will be minimized thereby maximizing battery life. Spacing load transients so that the average power required to service the application is less than or equal to the power available from the energy harvesting source will also greatly extend the life of the battery. The following equation can be used to size the input capacitor to meet the power requirements of the output for the desired duration:

$$C_{VIN} = \frac{\left(2/\eta \bullet V_{OUT} \bullet \Sigma I_n T_n\right)}{\left(V_{INOV}{}^2 - V_{INUV}{}^2\right)} (\mu F)$$

Here η is the average efficiency of the converter over the input voltage range and V_{IN} is the input voltage when the converter begins to switch. Typically $V_{IN(OV)}$ will be the selected input voltage rising threshold. $V_{IN(UV)}$ is the $V_{IN(OV)}$ minus the hysteresis voltage. $\Sigma I_n T_n$ is the area under each of the load pulses for given load profile. This equation may overestimate the input capacitor necessary. It may be

APPLICATIONS INFORMATION

acceptable to allow the load current to deplete the output capacitor all the way to the lower PGOOD threshold. The equation also assumes that the input source charging has a negligible effect during this time. Example uses of this equation to size input capacitors are included in the design examples later in this section.

The duration for which the regulator sleeps depends on the load current and the size of the V_{OUT} capacitor. The sleep time decreases as the load current increases and/or as the output capacitor decreases. The V_{OUT} capacitor should be a minimum of 47µF. A larger output capacitor can be used if lower peak-to-peak output voltage ripple is desired. A larger output capacitor will also improve load regulation on V_{OUT}. Multilayer ceramic or low ESR electrolytic capacitors are both excellent options.

Proper sizing of the input capacitor to optimize energy storage at the input utilizes the potential for higher input voltages and higher efficiency. Ultimately the output current is limited by what the converter can supply from its input. If a larger peak transient load needs to be serviced, the output capacitor should be sized to support the larger current for the duration of the load transient by the following:

$$C_{OUT} \geq I_{LOAD} \bullet \frac{t_{PULSE}}{V_{DROOP}}$$

C_{OUT} is the output capacitor value (µF) required, I_{LOAD} is the peak transient load current (mA), t_{PULSE} is the duration of that transient (ms) and V_{DROOP} is the amount of voltage droop the circuit can tolerate (both in V).

For many of the LTC3106 applications, the input capacitor values can be quite large (>1mF). A list of high value storage capacitor manufacture's is listed in Table 4. For larger bulk output capacitors an additional low effective series resistance (ESR) output capacitor of 10µF should be added and connected as close to the IC pin as possible.

Regardless of its value, the selected output capacitor must be rated higher than the voltage selected for V_{OUT} by OS1 and OS2. Likewise the selected input capacitor must be rated higher than the open-circuit voltage of the V_{IN} source.

Table 4. Recommended Bulk Storage Capacitor Vendors

VENDOR	PART
AVX	BestCap Series TAJ, TPS Series Tantalum
Vishay	595D Series (Tantalum) 153 CRV (Aluminum, Low Leakage) 150 CRZ (Aluminum, Low Leakage) 196 DLC (Double Layer Aluminum)
Illinois Capacitor	RKR Series (Aluminum, Low Leakage) DCN Series
Cooper Bussman	KR Series KW Series PA, PB, PM, PH Series
Cap-XX	G Series (Dual Cell) H Series (Dual Cell)

V_{CC} Capacitor Selection

The V_{CC} output of the LTC3106 is generated from the greatest of V_{IN}, V_{CAP}, V_{AUX} or V_{OUT}. A low ESR 0.1µF capacitor should be used. The capacitor should be located close to the V_{CC} pin and through the shortest ground traces possible.

V_{AUX} Capacitor Selection

A minimum 2.2µF low ESR capacitor must be used to decouple V_{AUX} although 4.7µF is more typical for many applications. Smaller capacitor sizes help reduce V_{OUT} ripple especially at high load currents while larger capacitor sizes improve start-up at low output voltages. The capacitor should be located as close to the V_{AUX} pin as possible.

As mentioned in the operations section the AUX D switch and the V_{OUT} D switch are in parallel. Asynchronous diode conduction will occur when either V_{AUX} or V_{OUT} is being serviced by the buck/boost circuitry. For this reason it is recommended to keep a 10:1 ratio of V_{OUT} to V_{AUX} capacitor to ensure a proper start-up with low voltage, high impedance sources. Under most load conditions the output voltage will be maintained normally although under true zero load conditions (<500nA) the parasitic current from V_{AUX} to V_{OUT} could force V_{OUT} to regulate up to 5% higher than typical.

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Use of Ceramic Capacitors

To minimize losses in low power systems all capacitors should have low leakage current. Ceramic capacitors are recommended for use in LTC3106 applications due to their small size, low ESR and low leakage currents. However, many ceramic capacitors intended for power applications experience a significant loss in capacitance from their rated value as the DC bias voltage on the capacitor increases. It is not uncommon for a small surface mount capacitor to lose more than 50% of its rated capacitance when operated at even half of its maximum rated voltage. This effect is generally reduced as the case size is increased for the same nominal value capacitor. As a result, it is often necessary to use a larger value capacitance or a higher voltage rated capacitor than would ordinarily be required to actually realize the intended capacitance at the operating voltage of the application. X5R and X7R dielectric types are recommended as they exhibit the best performance over the wide operating range and temperature of the LTC3106. To verify that the intended capacitance is achieved in the application circuit, be sure to consult the capacitor vendor's curve of capacitance versus DC bias voltage.

PGOOD Output

The PGOOD output can also help with power management. PGOOD transitions high the first time the output reaches regulation and stays high until the output falls to 92% of the regulation point. PGOOD can be used to trigger a system load. For example, a current burst could begin when PGOOD goes high and would continuously deplete the output capacitor until PGOOD went low. Note the PGOOD pin will remain high if the output is still within 92% of the regulation point, even if the input falls below the lower UVLO threshold.

Inductor Selection

Low DCR power inductors with values between 4.7µH and 10µH are suitable for use with the LTC3106. Inductor vendor information can be found in Table 5. For most applications, a 10µH inductor is recommended. In applications where the input voltage is very low, a larger value inductor can provide higher efficiency and a lower start-up voltage.

In applications where the input voltage is relatively high (V_{IN} > 0.8V), smaller inductors may be used to provide a smaller overall footprint. In all cases, the inductor must have a low DCR and a saturation current rating greater than the highest typical peak current limit setting as listed in the Electrical Characteristics table. If the DC resistance of the inductor is too high, efficiency will be reduced and the minimum operating voltage will increase. Note the inductor value will have a direct effect on the switching frequency.

Table 5. Inductor Vendor Information

VENDOR	PART
Coilcraft www.coilcraft.com	EPL2014, EPL3012, EPL3015, LPS3015, LPS3314, XFL3012
Coiltronics www.cooperindustries.com	SDH3812, SD3814, SD3114, SD3118
Murata www.murata.com	LQH3NP, LQH32P, LQH44P
Sumida www.sumida.com	CDRH2D16, CDRH2D18, CDRH3D14, CDRH3D16
Taiyo-Yuden www.t-yuden.com	NR3012T, NR3015T, NRS4012T, BRC2518
TDK www.tdk.com	VLS3012, VLS3015, VLF302510MT, VLF302512MT
Toko www.tokoam.com	DP3015C, DB3018C, DB3020C, DP418C, DP420C, DEM2815C, DFE322512C, DFE252012C
Würth www.we-online.com	WE-TPC 2813, WE-TPC 3816, WE-TPC 2828

Maximum Power Point Threshold Configuration

There are two methods for maintaining the maximum power point of an input source on V_{IN}. Already discussed in this data sheet is a resistive divider on the RUN pin monitoring V_{IN}. This is useful for >600mV MPP set points. The LTC3106 also has a dedicated MPP function that can be used over the full input voltage range as well as input voltages between the UVLO and RUN pin thresholds. Note that the LTC3106 I_Q increases from 1.6µA (typ) to 10.6µA (typ) if the MPPC pin functionality is enabled.

The MPP circuit hysteretically controls V_{IN} by setting a lower voltage threshold on the MPP pin. If V_{IN} drops below the MPP threshold the converter will stop drawing power from V_{IN} and force a sleep signal. If V_{STORE} is within the proper operating range, the output power will then be taken from V_{STORE}. If however there is not a valid

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backup source or if the ENVSTR is low the LTC3106 will go to sleep and no power will be available to V_{OUT} until V_{IN} charges the input capacitor voltage above the MPP threshold. If more power is available at V_{IN} than is needed to supply V_{OUT}, V_{IN} could rise above the MPP threshold to the open-circuit voltage of source. This is normal as long as the open-circuit voltage is below the maximum allowed input voltage. The MPP pin voltage is set by connecting a resistor between the MPP pin and GND, as shown in Figure 4. The MPP voltage is determined by the equation:

$$V_{MPP} = 1.5\mu A \bullet R_{MPP}\ (M\Omega)$$

Disable the MPP function by tying the MPP pin to V_{CC}.

Design Example 1: Photovoltaic or Solar Energy Harvesting with Primary Battery Backup

In traditional battery hyp. only wireless nodes the main control unit (MCU) is connected directly to the battery. Several factors contribute to reduced battery capacity in these applications. Typically these wireless systems poll the node at a very low frequency with long low power inactive periods and occasional high current bursts when communicating with the node. The peak current during the pulsed load is much greater than the nominal drain current given by the battery manufacturer reducing capacity beyond that specified at the typical static drain current. Further, the usable input voltages for most MCUs (2V min typ) limit the usable capacity.

The application circuit in Figure 9 shows the LTC3106 interfaced with the AM-1816 solar cell supplemented with a CR2032 primary battery configured to deliver power to a pulsed load output. Though an energy harvesting system can eliminate the need for batteries, it also serves to supplement and increase battery life. When enough ambient energy is available the battery is unloaded and is only used when the ambient source is inadequate, not only extending battery life but improving reliability. Even when battery use is necessary, the PRI pin configures the V_{STORE} input for use of a primary battery, here the CR2032, extending the input voltage range, thereby increasing use of the available capacity than would be possible with a direct battery-MCU connection.

The main input voltage, V_{IN}, of the LTC3106 is designed to accommodate high impedance solar cells over a wide voltage range. Solar cells are classified according to their output power level, material employed (crystal silicon, amorphous silicon, compound semiconductor) and application space (indoor or outdoor lighting). Sanyo Electric's Amorton product line (a subsidiary of Panasonic) offers a variety of solar cells for various light conditions (For typical light conditions see Table 6) and power levels as well the ability to customize cells for specific application size and shapes. An additional list of companies that manufacture small solar cells (also referred to as modules or solar panels) suitable for use with the LTC3106 is provided in Table 7.

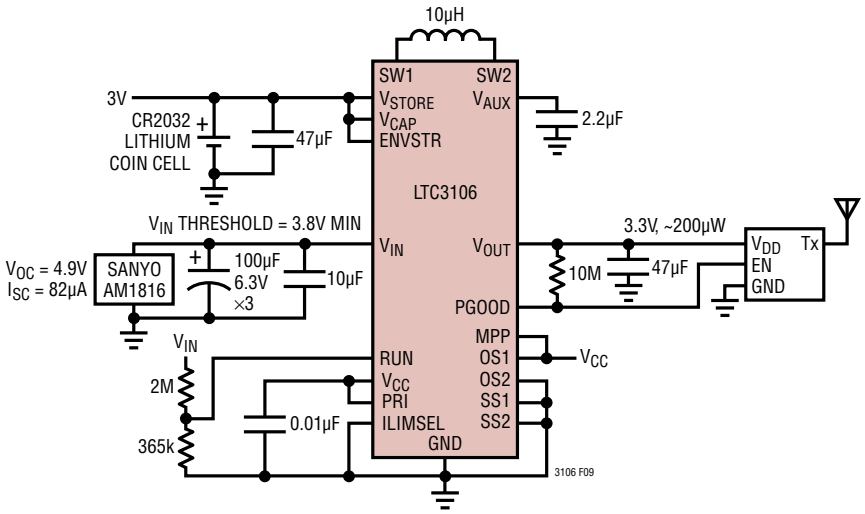

Figure 9. Solar Harvester with Primary Battery Backup

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Table 6. Typical Light Conditions

LOCATION	ILLUM. (Lux)
Meeting Room	200
Corridor	200
Office Desk	400 to 700
Lab	500 to 1000
Outdoors (Overcast)	1000 to 2000
Outdoors (Clear)	>2000

Table 7. Small Photovoltaic Panel Manufacturers

Sanyo	http://panasonic.net/energy/amorton/en/
PowerFilm	http://www.powerfilmsolar.com/
G24 Power	http://www.gcell.com/
SolarPrint	http://www.solarprint.ie/
Alta Devices	http://www.altadevices.com

The I-V and P-V curve for the AM-1816 panel is shown in Figure 10. The maximum power from the cell (PMAX) changes with light level but the voltage at PMAX changes only slightly. The V_{IN} threshold voltage in this application example is set to equal the voltage at PMAX using the resistive divider on the RUN pin. 4.2V is chosen for the $V_{IN(OV)}$ set point so that it is slightly below. With internal hysteresis the V_{INUV} is then 3.8V so the average V_{IN} voltage of ~4V is at the maximum power point from the manufacturer I-V and P-V data on the AM-1816 solar cell.

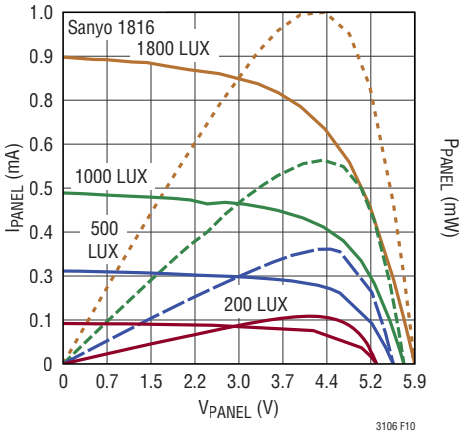

Figure 10. Measured I-V and P-V Curves Under Variable Light Conditions

Note the RUN pin resistive divider will add a V_{IN} dependent load on the input source. The divider current would be equal to:

$$I_{INDIV(STATIC)} \frac{4V}{(2.21M+432k)} = 1.6\mu A$$

In this application the load is a low power proprietary RF profile (Figure 11). The regions of operation are described, output and power losses are tabulated and the peak levels for each are given in Table 8. The total average output power needed in this application can be calculated to be 191µW.

Table 8. Application Load Profile Power Budget for Figure 11

INTERVAL	MCU FUNCTION	PEAK CURRENT I_n (mA)	INTERVAL T_n (ms)	CHARGE I_nT_n (µC)	REGION DUTY CYCLE (%)	INTERVAL OUTPUT POWER (mW)	AVERAGE OUTPUT POWER (µW)	LTC3106 POWER LOSS (FROM CURVES) (mW)	LTC3106 AVERAGE POWER LOSS (µW)
Region 1	Wake	0.3	1	0.3	0.1	1.0	1	0.2	0.2
Region 2	Pre-Processing	8	0.6	4.8	0.1	26.4	16	3	1.8
Region 3	Rx/Tx	20	1	20	0.1	66.0	66	5	5.0
Region 4	Processing	8	0.5	4	0.0	26.4	13	3	1.5
Region 5	Rx/Tx	20	1	20	0.1	66.0	66	5	5.0
Region 6	Sleep/Idle	0.001	1000	1	99.5	0.003	3	0.02	19.9
		Total Period: 1004ms				**Total Avg Power: 165µW**		**Total Avg. Power Loss: 37µW**	

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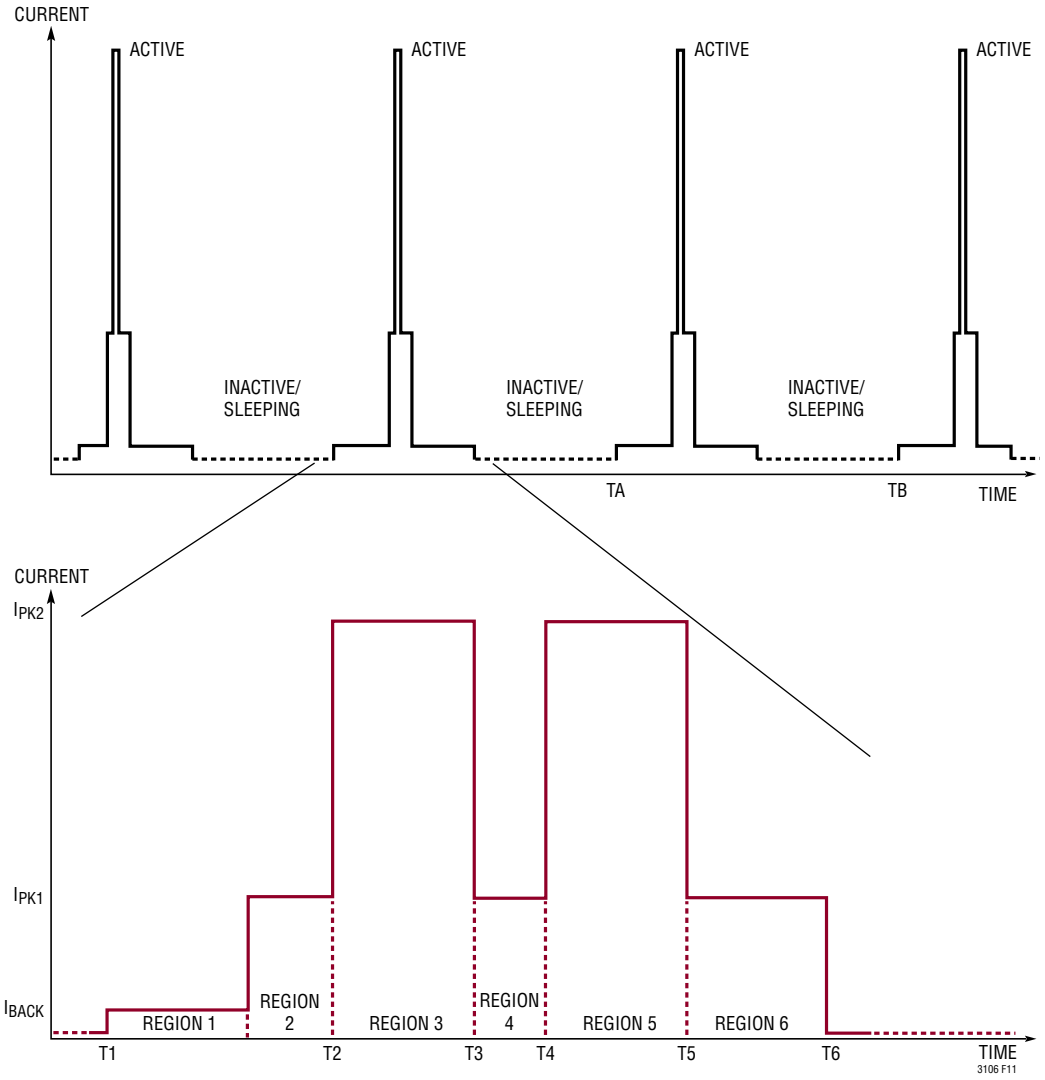

Figure 11. Application Load Profile for Schematic in Figure 8

The total average LTC3106 power loss over the same regions of operation for the load profile is 37µW. The divider load adds an additional 5µW of input power loss for a total input power requirement of 207µW. The calculated average efficiency, including the resistive divider is then η = 165µW/207µW which is 80%. The available power from the AM-1816 at 200lux is about 400µW. With a converter efficiency of about 80% the 400µW will power the total 207µW average load with some margin. If the light conditions become less favorable the available input power may drop below that needed to maintain the output voltage. The LTC3106 configuration in Figure 9 will operate with V_{IN} in "hiccup" mode turning on as V_{IN} increases above 4.2V and turning off if V_{IN} droops below 3.8V. With V_{IN} off, power is then taken from V_{STORE} until V_{IN} recovers and increases above the 4.2V threshold.

If the light conditions become more favorable V_{IN} will rise to the open-circuit voltage of the harvested source. Note if the open-circuit voltage of the harvested source will exceed the maximum voltage rating, an appropriate clamp should be added to prevent damage to the LTC3106. Figure 10 shows the open-circuit voltage of the AM-1816 can be greater than 5V. If full light is expected, a low reverse leakage current Zener diode is recommended to clamp V_{IN}. The DZ23, AZ23 and GDZ series with a Zener voltage of 4.7V or 5.1V are a good choice.

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To optimize use of the harvested source and increase the battery life of the backup source it is important to size the input capacitor to handle the average power load for the load profile at the lowest light level. Referring again to Table 8 to sum the required charge for the load and using the input capacitor sizing equation:

$$C_{VIN} = \frac{\left(2/\eta \bullet V_{OUT} \bullet \Sigma I_n T_n\right)}{\left(V_{IN(OV)}{}^2 - V_{IN(UV)}{}^2\right)} (\mu F)$$

The average efficiency (η) with V_{IN} = 4.2V and V_{OUT} = 3.3V is 0.8. The $V_{IN(OV)}$ and $V_{IN(UV)}$ thresholds are already determined and $\Sigma I_n T_n$ can be found in the load profile table. C_{VIN} is found to be 184µF. A single 220µF low leakage Tantalum chip capacitor could be used. For the lowest leakage solution and to add design margin 2× 100µF, 6.3V, ±10% ceramic capacitors are selected.

If the V_{IN} source is unavailable the primary battery on V_{STORE} will continue to supply the load. To offload the peak current load from the battery and minimize the effect of high peak currents degrading the rated battery capacity the lowest peak current setting on the LTC3106 is chosen. In addition, the V_{STORE} capacitor design should follow that of the V_{IN} capacitor. Using the same method but replacing the OV and UV thresholds with the max and min V_{STORE} input voltages the value of the V_{STORE} capacitor is calculated to be 38µF. For design margin a low ESR 10V, 47µF ceramic capacitor is used.

Design Example 2: Thermoelectric Harvesting from Peltier cell (TEG) with Rechargeable Battery Backup

A Peltier cell (also known as a thermoelectric cooler) is made up of a large number of series-connected P-N junctions, sandwiched between two parallel ceramic plates. Although Peltier cells are often used as coolers by applying a DC voltage to their inputs, they will also generate a DC output voltage, using the Seebeck effect, when the two plates are at different temperatures. The polarity of the output voltage will depend on the polarity of the temperature differential between the plates. The magnitude of the output voltage is proportional to the magnitude of the temperature differential between the plates. In this manner, a Peltier cell is referred to as a thermoelectric generator (TEG).

Peltier cells are available in a wide range of sizes and power capabilities, from less than 10mm square to over 50mm square. They are typically 2mm to 5mm in height. A list of Peltier cell manufacturers is given in Table 9.

Table 9. Peltier Cell Manufacturers

Micropelt www.micropelt.com
CUI, Inc www.cui.com (Distributor)
Fujitaka www.fujitaka.com/pub/peltier/english/thermoelectric_power.html
Ferrotec www.ferrotec.com/products/thermal/modules
Kryotherm www.kryothermusa.com
Laird Technologies www.lairdtech.com
Marlow Industries www.marlow.com
Nextreme www.nextreme.com
TE Technology www.tetech.com/Peltier-Thermoelectirc-Cooler-Modules.html
Tellurex www.tellurex.com

The low voltage capability of the LTC3106 design allows it to operate from a TEG with temperature differentials as low as 20°C, making it ideal for harvesting energy in many industrial applications in which a temperature difference exists between two surfaces or between a surface and the ambient environment.

The application circuit in Figure 12 shows the LTC3106 interfaced with a TEG supplemented with a Li-ion rechargeable (secondary) battery, both configured to deliver power to a low power pulsed load output. With the RUN pin connected to V_{STORE}, the application circuit is configured to take advantage of the 300mV input voltage UVLO. In this configuration V_{IN} will operate in "hiccup" mode turning on as V_{IN} increases above 0.3V and turning off if V_{IN} droops 50mV below 0.3V to maintain an average power to the output without allowing the input to fall to zero. Assuming a good battery voltage the output power will be supplied by the battery when the input voltage drops below the UVLO threshold and transition back to the input when the input charges up above the UVLO threshold.

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In addition to providing power to the output when the harvested power is not adequate, the secondary battery also provides a reservoir for excess harvested energy. If the output is in regulation harvested power is diverted to charge the secondary battery. The maximum charge voltage and low battery threshold are programmed by the SS1 and SS2 pins. In Figure 12 SS1 and SS2 are configured to provide a worst-case upper threshold of 4.16V and a worst-case low battery threshold of 2.88V (refer to Table 2). Charging of the secondary battery will terminate at the upper threshold to prevent excessive battery voltage. Since the ENVSTR pin is held high in this application, a prolonged absence of harvested power results in the output being maintained solely by the battery.

With V_{CAP} and V_{STORE} connected together, the battery will be disconnected from the internal power path at the low battery threshold to protect Li-Ion batteries from permanent damage due to deep discharge. A low ESR 10µF capacitor is used to decouple the V_{STORE}/V_{CAP} pin.

Similar to the previous design example the load profile is another low power proprietary RF profile (Figure 13). The RxTx rate of this load pulse is 2 seconds. The regions of operation are described, output and power losses are tabulated and the peak levels for each are given in Table 10. The total average output power needed in this application can be calculated to be 42µW.

The total average LTC3106 power loss over the same regions of operation for the load profile is 31µW. The total input power requirement is 73µW. The calculated average efficiency, including the resistive divider is then η = 42µW/73µW which is 0.58. Although this may seem low it is important to realize the load current is quite low (2µA) a majority of the time (sleep/idle region) where the average power loss from the LTC3106 is only 20µW.

To minimize use of the secondary battery and prolonging its long term lifetime, it is important to optimize the use of the harvested source by dimensioning the input capacitor to handle the average power load for the load profile at the lowest temperature differential. Referring again to

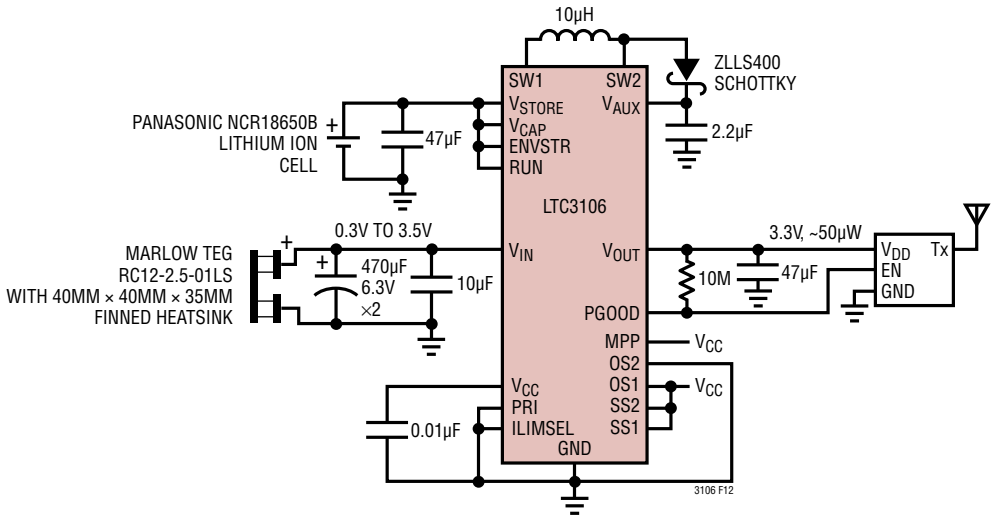

Figure 12. TEG Harvester with Secondary Battery Backup

APPLICATIONS INFORMATION

Table 11 to sum the required charge for the load and using the input capacitor sizing equation:

$$C_{VIN} = \frac{\left(2/\eta \bullet V_{OUT} \bullet \Sigma I_n T_n\right)}{\left(V_{INOV}{}^2 - V_{INUV}{}^2\right)}$$

Table 11. Low Capacity Li-Ion and Thin Film Battery Manufacturers

VENDOR	PART
CYMBET	EnerChip CBC Series
Infinite Power Solutions	THINERGY MEC2000 and MEC100 Series
GM Battery	GMB and LiPo Series

The average efficiency (η) with $V_{IN(OV)}$ = 0.3V and $V_{IN(UV)}$ = 0.25V, the input UVLO upper and lower thresholds respectively, and a V_{OUT} of 3.3V is the already calculated η = 0.58. The $\Sigma I_n T_n$ can be found in the load profile table. C_{VIN} is then found to be 973µF. At such low harvested power levels, the input capacitor values can be quite large.

Large value storage capacitor manufactures are listed in Table 4. The application in Figure 12 uses 2× 470µF Tantalum chip capacitors.

The chosen capacitor should be rated for a voltage greater than the maximum open-circuit voltage of the harvested source and/or clamped to an appropriate voltage. If the open circuit TEG voltage is expected to be greater than the maximum rating of the input pin, it is recommended that a low reverse leakage current 4.7V or 5.1V Zener diode be used to clamp V_{IN}.

The available power from the TEG at the lowest temperature differential (dt = 20°C) is about 200µW, enough to power the total 42µW average load with some margin.

If the conditions become less favorable the available input power may drop below that is needed at the output, V_{IN} will drop below the UVLO threshold turning off V_{IN}. With V_{IN} off, power is then taken from V_{STORE} until V_{IN} recovers and increases above the UVLO threshold.

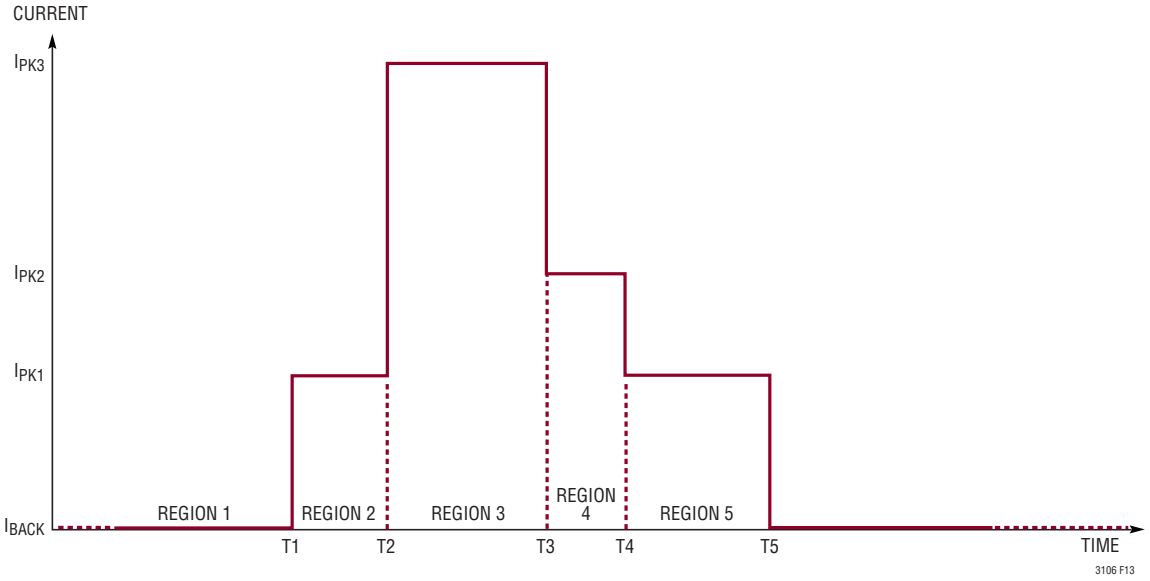

Figure 13. Application Load Profile

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If conditions become more favorable the input capacitor will charge to a higher voltage terminating at the open-circuit voltage of the harvested source. When the output is idle under these conditions, excess energy is used to maintain the charge on the V_{STORE} battery. Any remaining excess energy will be stored on the input capacitor and V_{IN} will rise to the open-circuit voltage of the harvested source. As already mentioned, if the open-circuit voltage of the harvested source will exceed the maximum voltage rating of the pin an appropriate clamp should be added to prevent damage to the LTC3106.

Most MCUs, even low power wireless specific MCUs, still load the LTC3106 output with a small current. If, however, the load current will be less than 400nA the output regulation error can increase to 5% of the nominal output voltage depending on sleep period and the size of the output capacitor.

Table 10. Application Load Profile Power Budget for Figure 11

INTERVAL	MCU FUNCTION	PEAK CURRENT I_n (mA)	INTERVAL T_n (ms)	CHARGE I_nT_n (µC)	REGION DUTY CYCLE (%)	INTERVAL OUTPUT POWER (mW)	AVERAGE OUTPUT POWER (µW)	LTC3106 POWER LOSS (FROM CURVES) (mW)	LTC3106 AVERAGE POWER LOSS (µW)
Region 1	Sleep/Idle	0.002	2000	4	99.85	0.007	7	0.2	20.0
Region 2	Pre-Processing	1.7	0.6	1.02	0.03	56	2	3	0.9
Region 3	Tx	17	1	17	0.05	53.1	28	5	7.5
Region 4	Rx	4	0.5	2	0.02	13.2	3	3	1.2
Region 5	Post-Processing	1.7	1	1.7	0.05	5.6	3	5	1.5
		Total Period: 2003ms				**Total Avg Power: 42.37µW**		**Total Avg. Power Loss: 31µW**	

TYPICAL APPLICATIONS

The circuit in Figure 14 is a practical example of simple energy harvesting. The LTC3106 is powered from the USB bus power when the USB interface is connected for data transfer to a host. When the USB power is available V_{STORE} is disabled as an input, output power will come from V_{IN} and charging of the battery will occur when V_{OUT} and V_{AUX} are in regulation. The battery may also be charged from ambient light on the Sanyo AM-1454 solar cell when the device used to collect data remotely, extending battery life and the time required between USB connections. Note that the D01 output from the monitor goes high and dials the LTC3106 peak current limit higher when USB power is available.

Figure 15 shows the LTC3106 as a simple dual input, 2.2V buck-boost converter. One input is from a 5V wall adaptor and the other from a 3V rechargeable lithium coin cell. Figure 15 also shows an example of the optional external inrush current limiting circuit to V_{AUX}.

To take advantage of the very low discharge rate and long shelf life of low capacity thin film batteries the application in Figure 16 shows use of the Shelf mode functionality. An external switch allows the V_{STORE} pin to be disconnected from the external bypass capacitor on V_{CAP} as well the internal power path and threshold detection circuitry thereby reducing battery discharge to V_{STORE} pin leakage plus the self-discharge of the battery itself. A factory "pre-charged" battery could then be assembled into the harvester node and stored with a full charge for some time. When enabled the battery will supplement the harvested source and will be recharged with any surplus harvested energy. A list of thin-film battery manufacturers is listed in Table 11.

The circuit in Figure 17 shows the LTC3106 configured to harvest solar energy when possible to prolong the time before battery service is necessary. The resistive divider on RUN sets the optimal minimum operating point for the solar cell on V_{IN}. When available, harvested power on V_{IN} supplements the power available from the primary battery extending the life of the battery.

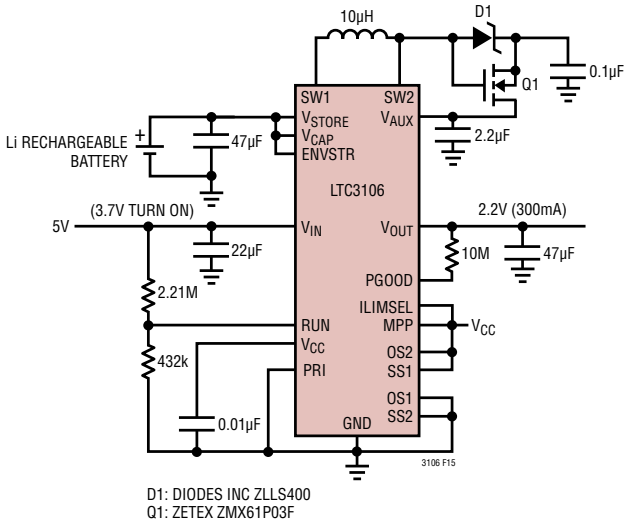


Figure 15. 5V to 2.2V Converter with Rechargeable Battery Backup and Inrush Current Limiting

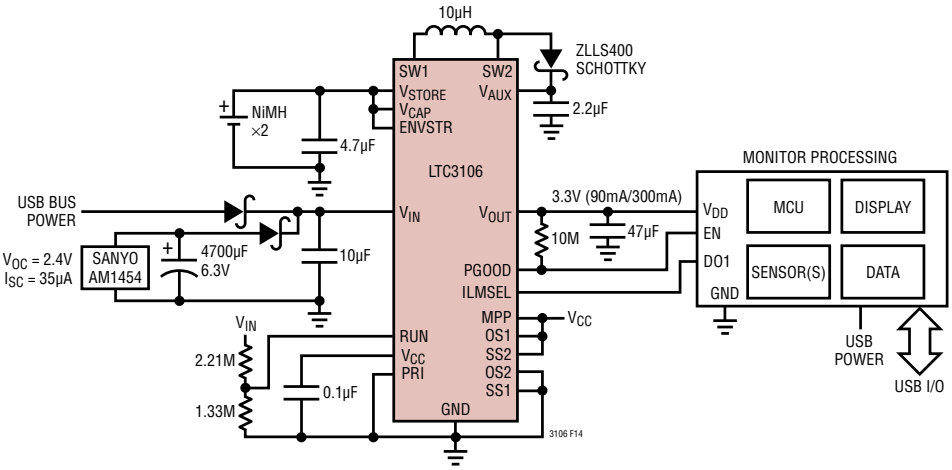


Figure 14. Portable Medical Device with Ambient Light Harvester or USB Powered Charging

TYPICAL APPLICATIONS

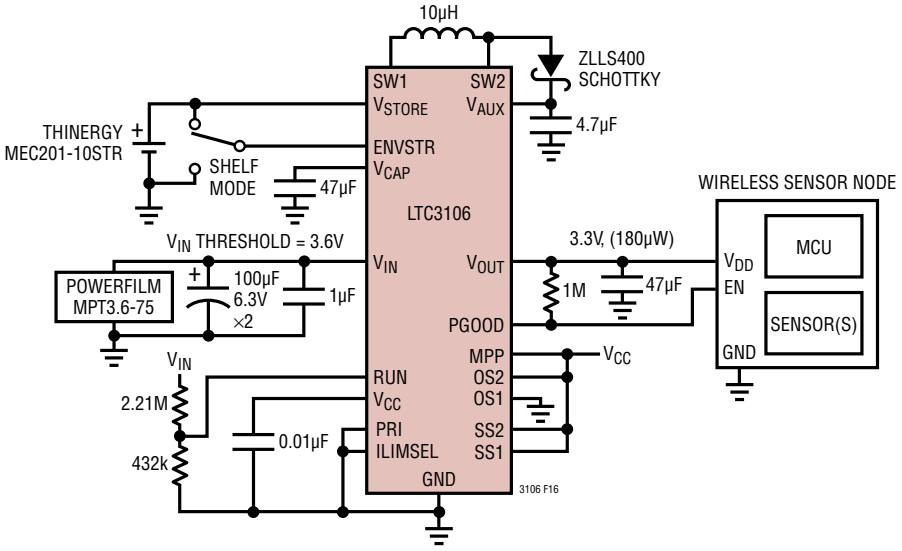


Figure 16. Remote Outdoor Solar Powered Harvester with Thin Film Battery Backup

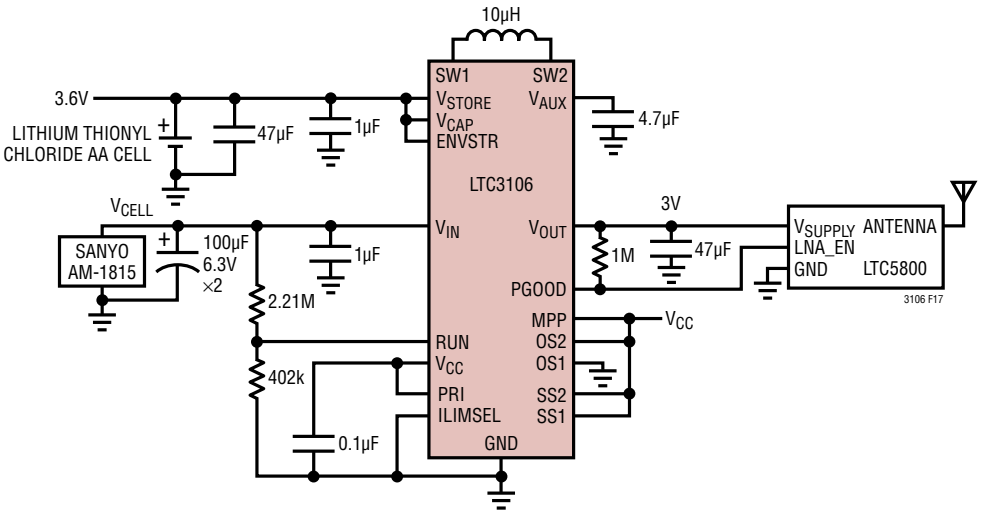
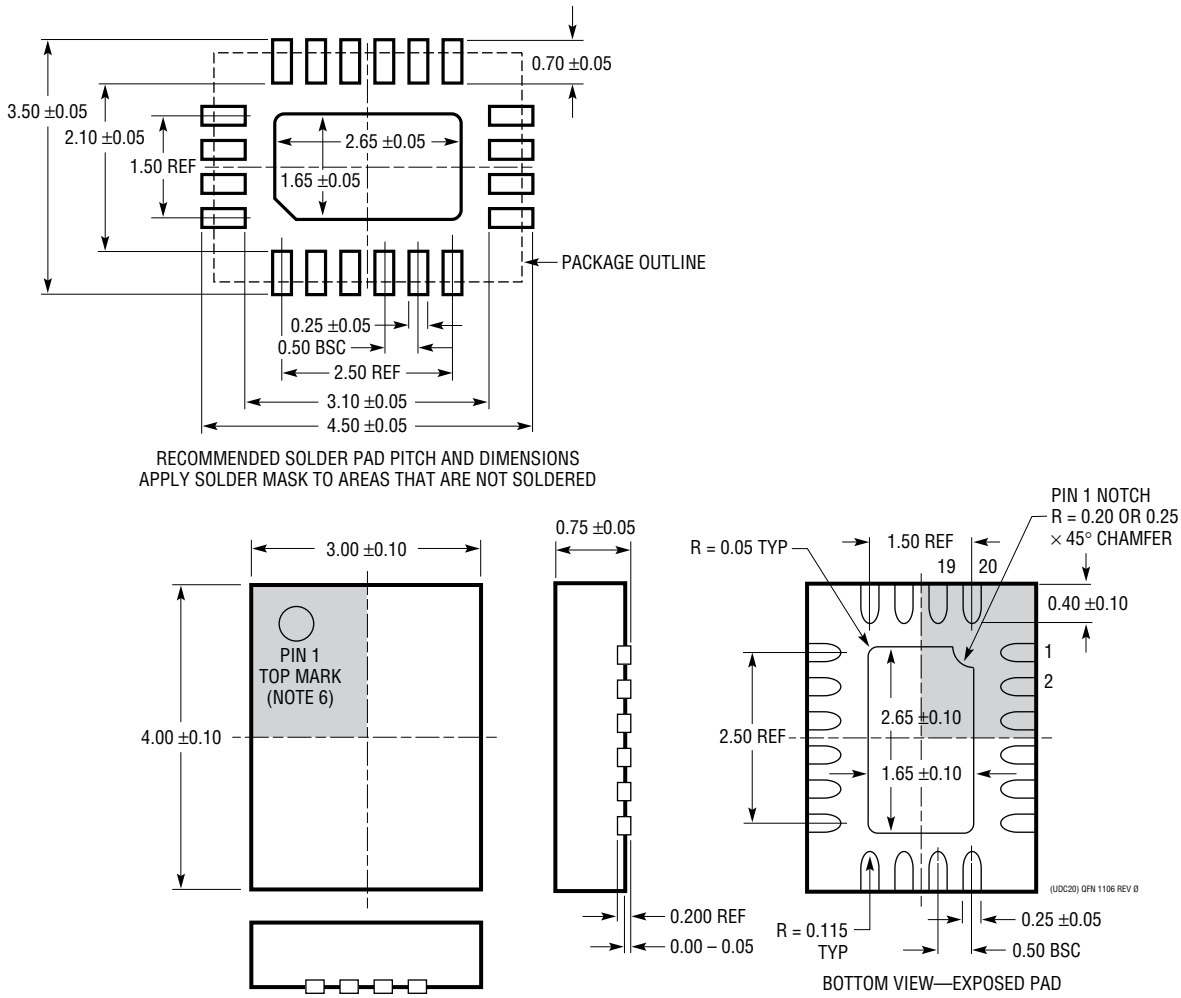


Figure 17. Extended Life Battery Powered Mote for Wireless Mesh Network

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3106#packaging for the most recent package drawings.

UDC Package
20-Lead Plastic QFN (3mm × 4mm)
(Reference LTC DWG # 05-08-1742 Rev Ø)

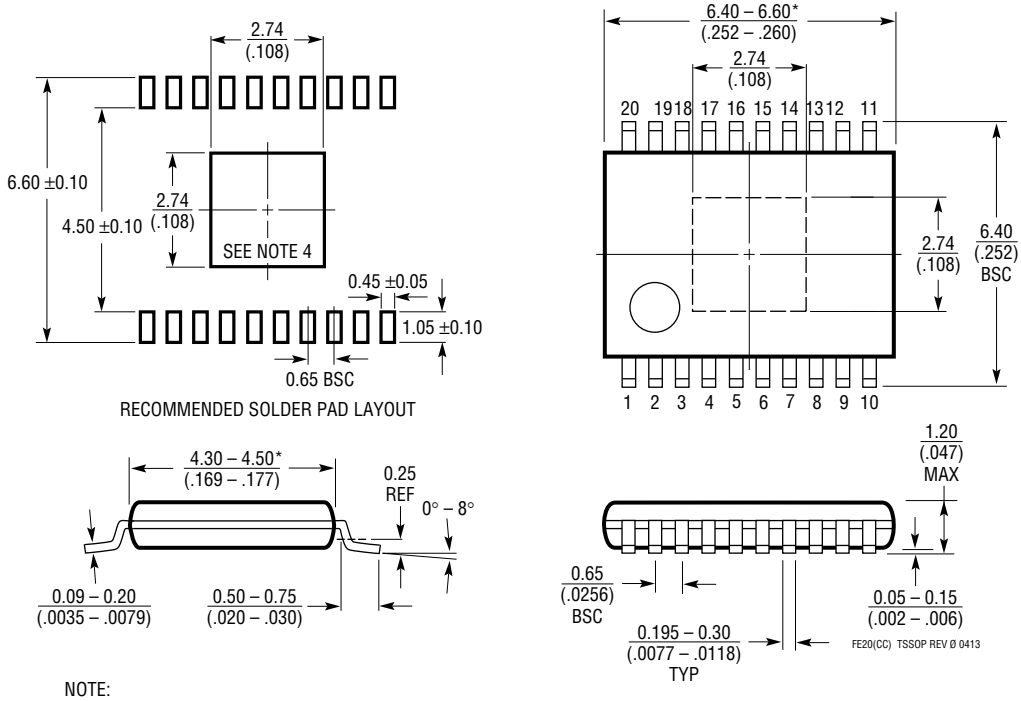


NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3106#packaging for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1950 Rev Ø)
Exposed Pad Variation CC

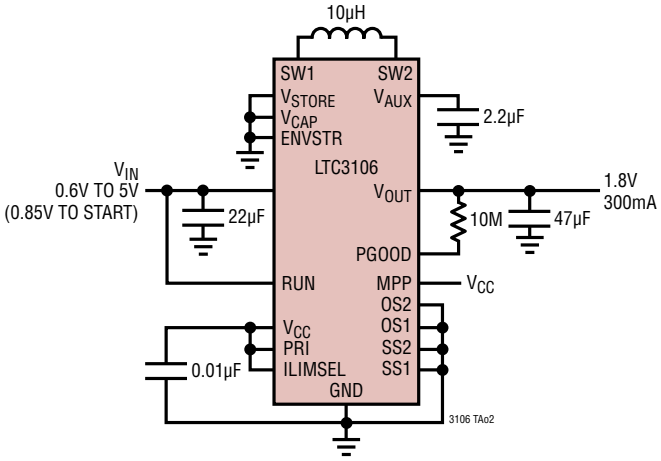


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Simple Wide Input Voltage Buck-Boost Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3103	15V, 300mA Synchronous Step-Down DC/DC Converter with Ultralow Quiescent Current	V_{IN}: 2.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 1.8µA, I_{SD} = 1µA 3mm × 3mm DFN-10, MSOP-10
LTC3105	400mA Step-Up DC/DC Converter with Maximum Power Point Control and 250mV Start-Up	V_{IN}: 0.225V to 5V, $V_{OUT(MIN)}$ Adj. 1.5V to 5V, I_Q = 24µA, I_{SD} < 1µA, 3mm × 3mm DFN-12, MSOP-12
LTC3107	Ultralow Voltage Energy Harvester and Primary Battery Life Extender	V_{IN} = 0.02V to 1V, V_{OUT} Tracks V_{BAT}, V_{BAT} = 2V to 4V, I_Q = 80nA, V_{LDO} = 2.2V, 3mm × 3mm DFN-10
LTC3108/LTC3108-1	Ultralow Voltage Step-Up Converter and Power Managers	V_{IN}: 0.02V to 1V, $V_{OUT(MIN)}$ Fixed 2.35V to 5V, I_Q = 6µA, I_{SD} < 1µA, 3mm × 4mm DFN-12, SSOP-16
LTC3109	Auto-Polarity, Ultralow Voltage Step-Up Converter and Power Manager	V_{IN}: 0.03V to 1V, $V_{OUT(MIN)}$ Fixed 2.35V to 5V, I_Q = 7µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, SSOP-20
LTC4070	Li-Ion/Polymer Shunt Battery Charger System	450nA I_Q, 1% Float Voltage Accuracy, 50mA Shunt Current 4.0V/4.1V/4.2V
LTC4071	Li-Ion/Polymer Shunt Battery Charger System with Low Battery Disconnect	550nA I_Q, 1% Float Voltage Accuracy, <10nA Low Battery Disconnect, 4.0V/4.1V/4.2V, 8-Lead 2mm × 3mm DFN and MSOP Packages
LTC3129/LTC3129-1	Micropower 200mA Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.42V to 15V, V_{OUT}: 1.4V to 15V, I_Q = 1.3µA, I_{SD} = 10nA, MSOP-16E, 3mm × 3mm QFN-16 Packages
LTC3330/LTC3331	Nanopower Buck-Boost DC/DC with Energy Harvesting Battery Life Extender	V_{IN}: 2.7V to 20V, V_{OUT}: 1.2V to 5.0V, Enable and Standby Pins, I_Q = 750nA, 5mm × 5mm QFN-32 Package
LTC3388-1/LTC3388-3	20V High Efficiency Nanopower Step-Down Regulator	V_{IN}: 2.7V to 20V, V_{OUT}: 1.2V to 5.0V, Enable and Standby Pins, I_Q = 720nA, I_{SD} = 400nA, 3mm × 3mm DFN-10, MSOP-10
LTC3588-1	Nanopower Energy Harvesting Power Supply	950nA I_Q in Sleep, V_{OUT}: 1.8V, 2.5V, 3.3V, 3.6V, Integrated Bridge Rectifier, MSE-10 and 3mm × 3mm QFN-10 Packages
LTC3588-2	Nanopower Energy Harvesting Power Supply	<1µA I_Q in Regulation, UVLO Rising = 16V, UVLO Falling = 14V, V_{OUT} = 3.45V, 4.1V, 4.5V 5.0, MSE-10 and 3mm × 3mm QFN-10 Packages
LTC5800-IPMA	IP Wireless Mote-On-Chip	Ultralow Power Mote, 72-Lead, 10mm × 10mm QFN

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