



# Dual N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}$ ( $\Omega$ )	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)			
60	1.4 at V <sub>GS</sub> = 10 V	0.37	0.47			
00	$3.0 \text{ at V}_{GS} = 4.5 \text{ V}$	0.25	0.47			

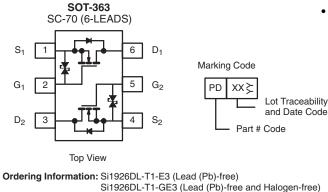
### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R<sub>g</sub> Tested
- ESD Protected: 1800 V
- Compliant to RoHS Directive 2002/95/EC

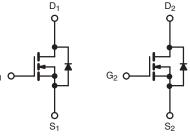


### **APPLICATIONS**

· Low Power Load Switch







N-Channel MOSFET

N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATING</b>	<b>S</b> T <sub>A</sub> = 25 °C, unlo	ess otherwis	e noted	
Parameter		Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	<b> </b>
	T <sub>C</sub> = 25 °C		0.37	
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C	] .	0.30	
Continuous Diain Current (1) = 130 C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	0.34 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		0.27 <sup>b, c</sup>	Α
Pulsed Drain Current		I <sub>DM</sub>	0.65	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	1-	0.43	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	- I <sub>S</sub>	0.25 <sup>b, c</sup>	
	T <sub>C</sub> = 25 °C		0.51	
Maximum Dawar Dissipation	T <sub>C</sub> = 70 °C	P <sub>D</sub>	0.33	w
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	] 'D	0.30 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C	1	0.20 <sup>b, c</sup>	
Operating Junction and Storage Temperature R	T <sub>J</sub> , T <sub>stq</sub>	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 5 s	R <sub>thJA</sub>	360	415	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	300	350	] 0/00	

#### Notes:

- a. Based on  $T_C = 25$  °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. Maximum under steady state conditions is 400 °C/W.

# **Si1926DL**

# Vishay Siliconix



<b>SPECIFICATIONS</b> T <sub>J</sub> = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 A		56.7		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	l <sub>D</sub> = 250 μA		- 3		mv/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1		2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 10 \text{ V}$			± 150	nA	
Zoro Coto Voltago Drain Current	1	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$			10	μΑ	
On-State Drain Current <sup>a</sup>	-	$V_{DS} = \ge 10 \text{ V}, V_{GS} = 4.5 \text{ V}$	0.50			Α	
On-State Drain Current	I <sub>D(on)</sub>	$V_{DS} = \ge 7.5 \text{ V}, V_{GS} = 10 \text{ V}$	0.65				
Drain-Source On-State Resistance <sup>a</sup>	D	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.34 A			1.4		
Diain-Source On-State Resistance"	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 0.23 \text{ A}$			3	Ω	
Forward Transconductance	9 <sub>fs</sub>	$V_{DS} = 30 \text{ V}, I_D = 0.2 \text{ A}$		159		ms	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			18.5			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		7.5		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			4.2			
Tabel Oats Observe	Qg	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 0.34 \text{ A}$		0.9	1.4		
Total Gate Charge				0.5	0.75		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 0.34 \text{ A}$		0.2		nC	
Gate-Drain Charge	Q <sub>gd</sub>			0.15			
Gate Resistance	$R_g$	f = 1 MHz		160	240	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			6.5	10		
Rise Time	t <sub>r</sub>	$V_{DD} = 30 \text{ V}, R_{L} = 100 \Omega$		12	18		
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong 0.3 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		13	22	ns ns	
Fall Time	t <sub>f</sub>			14	21		
Drain-Source Body Diode Characterist	ics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			0.43	^	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				0.65	A	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 0.3 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			16.5	25	nC	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	1 0 6 4 41/44 400 4/		13	20		
Reverse Recovery Fall Time	ta	I <sub>F</sub> = 0.6 A, dI/dt = 100 A/μs		13.5			
Reverse Recovery Rise Time	t <sub>b</sub>			3		ns	

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

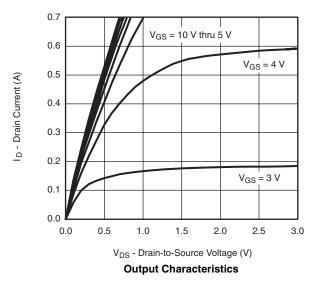
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

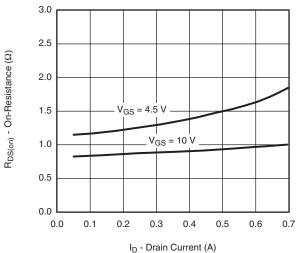




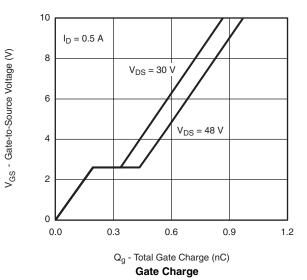


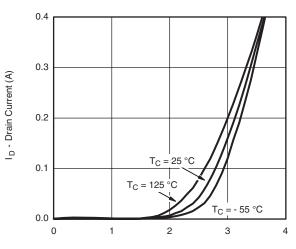
# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



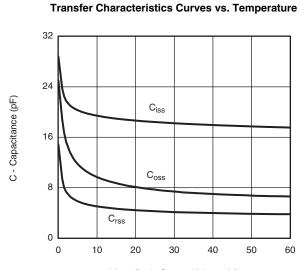


On-Resistance vs. Drain Current



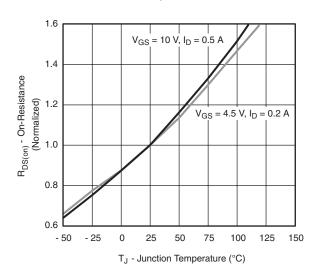


V<sub>GS</sub> - Gate-to-Source Voltage (V)



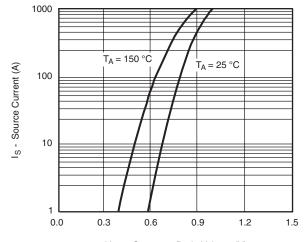
V<sub>DS</sub> - Drain-Source Voltage (V)

### Capacitance

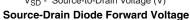


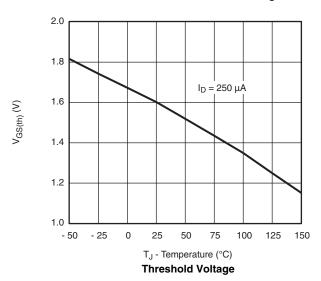
On-Resistance vs. Junction Temperature

# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

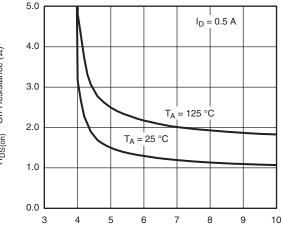


 $V_{SD}$  - Source-to-Drain Voltage (V)



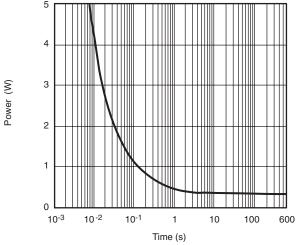


R<sub>DS(on)</sub> - On-Resistance (᠒)

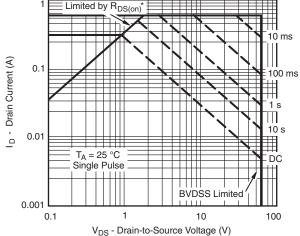


V<sub>GS</sub> - Gate-to-Source Voltage (V)

 $R_{DS(on)}$  vs.  $V_{GS}$  vs. Temperature



Single Pulse Power



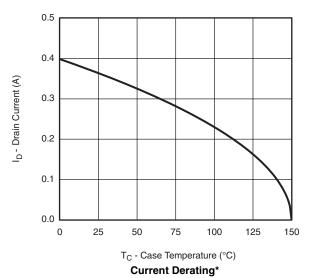
\*  $V_{GS} > minimum \ V_{GS}$  at which  $R_{DS(on)}$  is specified

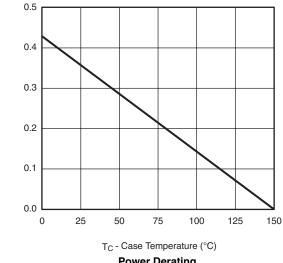
Safe Operating Area





# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





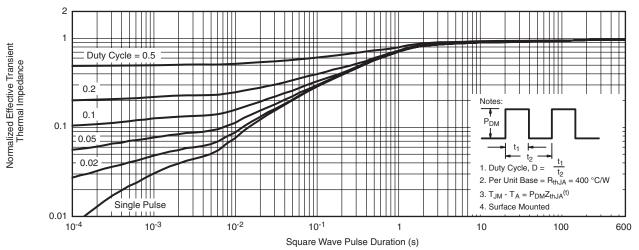
**Power Derating** 

Power Dissipation (W)

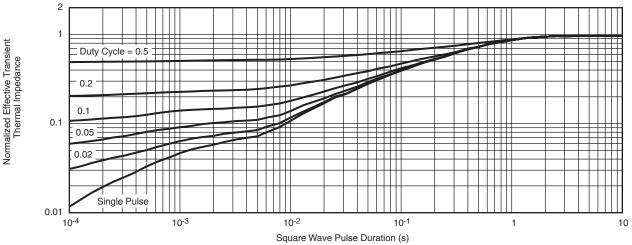
 $<sup>^*</sup>$  The power dissipation  $P_D$  is based on  $T_{J(max)}$  = 150  $^{\circ}$ C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package



### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



#### Normalized Thermal Transient Impedance, Junction-to-Ambient



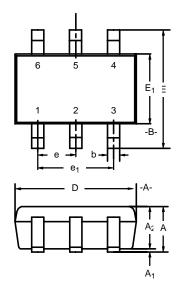
Normalized Thermal Transient Impedance, Junction-to-Foot

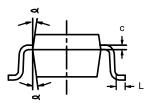
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?73684">www.vishay.com/ppg?73684</a>.





# SC-70: 6-LEADS





	MILLIMETERS			I	NCHE	S
Dim	Min	Nom	Max	Min	Nom	Max
Α	0.90	_	1.10	0.035	_	0.043
A <sub>1</sub>	-	_	0.10	-	_	0.004
A <sub>2</sub>	0.80	_	1.00	0.031	_	0.039
b	0.15	_	0.30	0.006	_	0.012
С	0.10	-	0.25	0.004	-	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
Ε	1.80	2.10	2.40	0.071	0.083	0.094
E <sub>1</sub>	1.15	1.25	1.35	0.045	0.049	0.053
е	0.65BSC			0.026BSC	;	
e <sub>1</sub>	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
کے	7°Nom				7°Nom	

DWG: 5550





# **Dual-Channel LITTLE FOOT® SC-70 6-Pin MOSFET Recommended Pad Pattern and Thermal Performance**

### **INTRODUCTION**

This technical note discusses the pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for dual-channel LITTLE FOOT power MOSFETs in the SC-70 package. These new Vishay Siliconix devices are intended for small-signal applications where a miniaturized package is needed and low levels of current (around 250 mA) need to be switched, either directly or by using a level shift configuration. Vishay provides these devices with a range of on-resistance specifications in 6-pin versions. The new 6-pin SC-70 package enables improved on-resistance values and enhanced thermal performance.

#### **PIN-OUT**

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration.

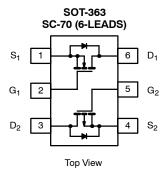


FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (http://www.vishay.com/doc?71154)

#### BASIC PAD PATTERNS

See Application Note 826, Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs, (http://www.vishay.com/doc?72286) for the 6-pin SC-70. This basic pad pattern is sufficient for the low-power applications for which this package is intended. For the 6-pin device, increasing the pad patterns yields a reduction in thermal resistance on the order of 20% when using a 1-inch square with full copper on both sides of the printed circuit board (PCB).

### **EVALUATION BOARDS FOR THE DUAL** SC70-6

The 6-pin SC-70 evaluation board (EVB) measures 0.6 inches by 0.5 inches. The copper pad traces are the same as described in the previous section, Basic Pad Patterns. The board allows interrogation from the outer pins to 6-pin DIP connections permitting test sockets to be used in evaluation testing.

The thermal performance of the dual SC-70 has been measured on the EVB with the results shown below. The minimum recommended footprint on the evaluation board was compared with the industry standard 1-inch square FR4 PCB with copper on both sides of the board.

#### THERMAL PERFORMANCE

### Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package measured as junction-to-foot thermal resistance is 300°C/W typical, 350°C/W maximum. The "foot" is the drain lead of the device as it connects with the body. Note that these numbers are somewhat higher than other LITTLE FOOT devices due to the limited thermal performance of the Alloy 42 lead-frame compared with a standard copper lead-frame.

### **Junction-to-Ambient Thermal Resistance** (dependent on PCB size)

The typical  $R\theta_{JA}$  for the dual 6-pin SC-70 is  $400^{\circ} C/W$  steady state. Maximum ratings are 460°C/W for the dual. All figures based on the 1-inch square FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at two different ambient temperatures.

Document Number: 71237 www.vishav.com 12-Dec-03



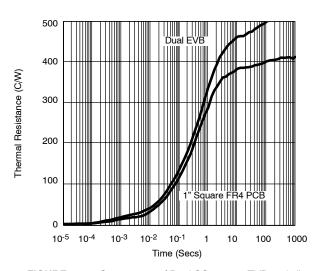
SC-70 (6-PIN)	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_{D} = \frac{T_{J(max)} - T_{A}}{R\theta_{JA}}$	$P_{D} = \frac{T_{J(max)} - T_{A}}{R\theta_{JA}}$
$P_{D} = \frac{150^{\circ}C - 25^{\circ}C}{400^{\circ}C/W}$	$P_{D} = \frac{150^{\circ}C - 60^{\circ}C}{400^{\circ}C/W}$
$P_D = 312 \text{mW}$	$P_D = 225 \text{ mW}$

NOTE: Although they are intended for low-power applications, devices in the 6-pin SC-70 will handle power dissipation in excess of 0.2 W.

### **Testing**

To aid comparison further, Figure 2 illustrates the dual-channel SC-70 thermal performance on two different board sizes and two different pad patterns. The results display the thermal performance out to steady state. The measured steady state values of  $R\theta_{JA}$  for the dual 6-pin SC-70 are as follows:

LITTLE FOOT SC-70 (6-PIN)			
Minimum recommended pad pattern (see Figure 2) on the EVB of 0.5 inches x 0.6 inches.	518°C/W		
2) Industry standard 1" square PCB with maximum copper both sides.	413°C/W		



Comparison of Dual SC70-6 on EVB and 1" FIGURE 2. Square FR4 PCB.

The results show that if the board area can be increased and maximum copper traces are added, the thermal resistance reduction is limited to 20%. This fact confirms that the power dissipation is restricted with the package size and the Alloy 42 leadframe.

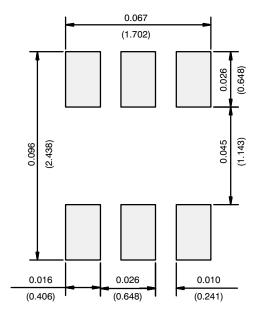
### **ASSOCIATED DOCUMENT**

Single-Channel LITTLE FOOT SC-70 6-Pin MOSFET Copper Leadframe Version, REcommended Pad Pattern and Thermal Performance, AN815, (http://www.vishay.com/doc?71334).

Document Number: 71237 www.vishay.com 12-Dec-03



### **RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



# **Legal Disclaimer Notice**

Vishay

# **Disclaimer**

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and/or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

# **Material Category Policy**

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

Revision: 02-Oct-12 Document Number: 91000

# **ПОСТАВКА** ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

# Данный компонент на территории Российской Федерации Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

## http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

## Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru\_6 moschip.ru\_4 moschip.ru\_9