19-1498; Rev 1; 12/99

EVALUATION KIT AVAILABLE

# +3.3V, 2.5Gbps, SDH/SONET 16:1 Serializer with Clock Synthesis and LVDS Inputs



## General Description

The MAX3890 serializer is ideal for converting 16-bit-wide, 155Mbps parallel data to 2.5Gbps serial data in ATM and SDH/SONET applications. Operating from a single +3.3V supply, this device accepts low-voltage differential-signal (LVDS) clock and data inputs for interfacing with high-speed digital circuitry, and delivers positive-referenced emitter-coupled logic (PECL) serial data and clock outputs. A fully integrated phase-locked loop (PLL) synthesizes an internal 2.5GHz serial clock from a 155.52MHz, 77.76MHz, 51.84MHz, or 38.88MHz reference clock. A loopback data output is provided to facilitate system diagnostic testing.

The MAX3890 is available in the extended temperature range (-40°C to +85°C) in a 64-pin TQFP exposed-pad (EP) package.

## Applications

2.5Gbps SDH/SONET Transmission Systems

2.5Gbps ATM/SONET Access Nodes

Add/Drop Multiplexers

Digital Cross-Connects

ATM Backplanes

## Features

- **Single +3.3V Supply**
- **495mW Power Consumption**
- **Exceeds ANSI, ITU, and Bellcore Specifications**
- **155Mbps (16-bit wide) Parallel to 2.5Gbps Serial Conversion**
- **Clock Synthesis for 2.5Gbps**
- **Multiple Clock Reference Frequencies (155.52MHz, 77.76MHz, 51.84MHz, 38.88MHz)**
- **LVDS Parallel Clock and Data Inputs**
- **Additional High-Speed Output for System Loopback Testing**

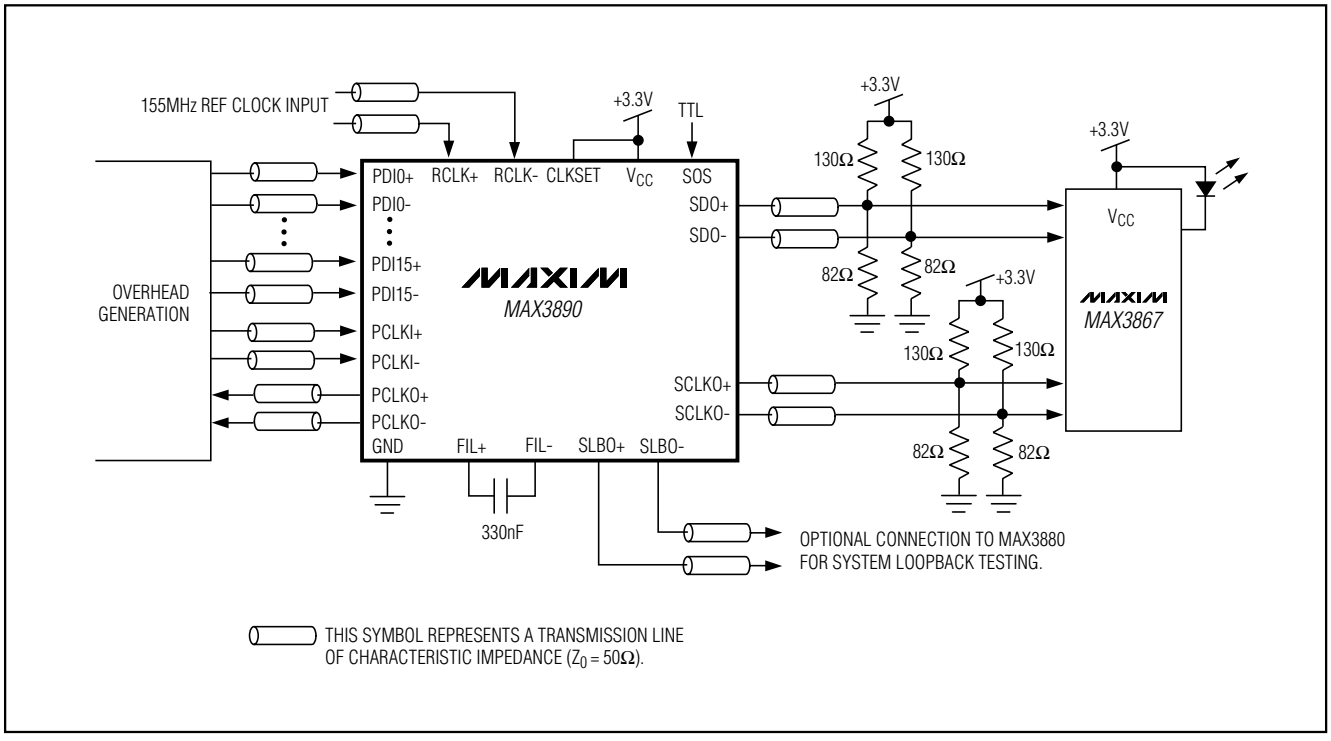
## Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE |
|---|---|---|
| MAX3890ECB | -40°C to +85°C | 64 TQFP-EP* |

**EP = Exposed pad*

***Pin Configuration appears at end of data sheet.***

## Typical Operating Circuit






*For free samples and the latest literature, visit www.maxim-ic.com or phone 1-800-998-8800. For small orders, phone 1-800-835-8769.*

# +3.3V, 2.5Gbps, SDH/SONET 16:1 Serializer with Clock Synthesis and LVDS Inputs

## ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- $V_{CC}$ .....-0.5V to +5V
- All Inputs, FIL+, FIL- .....-0.5V to ($V_{CC}$ + 0.5V)

Output Current
- LVDS Outputs (PCLKO±).....10mA
- PECL Outputs (SDO±, SCLKO±).....50mA
- CML Outputs (SLBO±).....15mA

Continuous Power Dissipation ($T_A$ = +85°C)
- TQFP-EP (derate 44.8mW/°C above +85°C) .....1W

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +3.0V to +3.6V, differential LVDS loads = 100Ω ±1%, PECL loads = 50Ω ±1% to ($V_{CC}$ - 2V), CML loads = 50Ω ±1% to $V_{CC}$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V, $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Current | $I_{CC}$ | PECL outputs unterminated, SOS = low | | 150 | 230 | mA |
| **PECL OUTPUTS** (SDO±, SCLKO±) | | | | | | |
| Output Voltage High | $V_{OH}$ | $T_A$ = 0°C to +85°C | $V_{CC}$ - 1.025 | | $V_{CC}$ - 0.88 | V |
| | | $T_A$ = -40°C | $V_{CC}$ - 1.085 | | $V_{CC}$ - 0.88 | |
| Output Voltage Low | $V_{OL}$ | $T_A$ = 0°C to +85°C | $V_{CC}$ - 1.81 | | $V_{CC}$ - 1.62 | V |
| | | $T_A$ = -40°C | $V_{CC}$ -1.83 | | $V_{CC}$ - 1.555 | |
| **LVDS INPUTS AND OUTPUTS** (PCLKO±, PDI_±, PCLKI±, RCLKI±) | | | | | | |
| Input Voltage Range | $V_I$ | Differential input voltage = 100mV | 0 | | 2.4 | V |
| Differential Input Threshold | $V_{IDTH}$ | | -100 | | 100 | mV |
| Threshold Hysteresis | $V_{HYST}$ | | | 60 | | mV |
| Differential Input Resistance | $R_{IN}$ | | 85 | 100 | 115 | Ω |
| Output Voltage High | $V_{OH}$ | | | | 1.475 | V |
| Output Voltage Low | $V_{OL}$ | | 0.925 | | | V |
| Differential Output Voltage | $\|V_{OD}\|$ | Figure 5 | 250 | | 400 | mV |
| Change in Magnitude of Differential Output Voltage for Complementary States | $\Delta\|V_{OD}\|$ | | | | ±25 | mV |
| Output Offset Voltage | $V_{OS}$ | | 1.125 | | 1.275 | V |
| Change in Magnitude of Output Offset Voltage for Complementary States | $\Delta V_{OS}$ | | | | ±25 | mV |
| Single-Ended Output Resistance | $R_O$ | | 40 | 95 | 140 | Ω |
| Change in Magnitude of Single-Ended Output Resistance for Complementary Outputs | $\Delta R_O$ | | | ±2.5 | ±10 | % |

## DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +3.0V to +3.6V, differential LVDS loads = 100Ω ±1%, PECL loads = 50Ω ±1% to ($V_{CC}$ - 2V), CML loads = 50Ω ±1% to $V_{CC}$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V, $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **PROGRAMMING INPUT** (CLKSET) | | | | | | |
| CLKSET Input Current | $I_{CLKSET}$ | CLKSET = 0 or $V_{CC}$ | | | ±500 | µA |
| **TTL INPUT** (SOS) | | | | | | |
| Input Voltage High | $V_{IH}$ | | 2.0 | | | V |
| Input Voltage Low | $V_{IL}$ | | | | 0.8 | V |
| Input Current High | $I_{IH}$ | | -10 | | 10 | µA |
| Input Current Low | $I_{IL}$ | | -10 | | 10 | µA |
| **CURRENT MODE LOGIC (CML) OUTPUTS** (SLBO±) | | | | | | |
| Differential Output Voltage | $\|V_{OD}\|$ | | 100 | | 400 | mV |
| Single-Ended Output Resistance | $R_O$ | | | 50 | | Ω |

## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +3.0V to +3.6V, differential LVDS load = 100Ω ±1%, PECL loads = 50Ω ±1% to ($V_{CC}$ - 2V), CML loads = 50Ω ±1% to $V_{CC}$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V, $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Serial Clock Rate | $f_{SCLK}$ | | | 2.488 | | GHz |
| Parallel Data Setup Time | $t_{SU}$ | (Note 2) | 300 | | | ps |
| Parallel Data-Hold Time | $t_H$ | (Note 2) | 700 | | | ps |
| PCLKO to PCLKI Skew | $t_{SKEW}$ | Figure 2 | 0 | | +4.0 | ns |
| Output Jitter Generation (SCLKO±) | $\Phi_0$ | Jitter bandwidth = 12kHz to 20MHz, RCLK amplitude > $\|V_{IDTH}\|$ (Note 3) | | | 3 | $ps_{RMS}$ |
| PECL Differential Output Rise/Fall Time | $t_R$, $t_F$ | 20% to 80% | | | 120 | ps |
| Parallel Input Clock Rate | $f_{PCLKI}$ | | | 155.52 | | MHz |
| Reference Clock Input (RCLKI) Rise/Fall Time | $t_R$, $t_F$ | 20% to 80%, f = 155.52MHz | | | 1.0 | ns |
| Parallel Clock Output (PCLKO) Rise/Fall Time | $t_R$, $t_F$ | 20% to 80% | | | 1.0 | ns |
| Serial Clock Output (SCLKO) to Serial-Data Output (SDO) Delay | $t_{SCLK-SD}$ | SCLKO rising edge to SDO edge | 110 | | 290 | ps |

**Note 1:** AC characteristics guaranteed by design and characterization.

**Note 2:** Setup and hold times are relative to the rising edge of PCLKI+, measured by applying a 155.52MHz differential parallel clock with rise/fall time = 1ns (20% to 80%). See Figure 2.

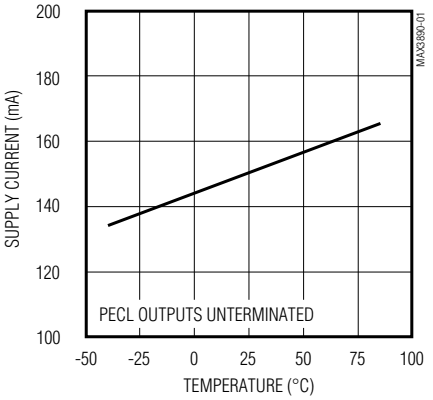
**Note 3:** For $f_{RCLK}$ = 38.88MHz, the minimum reference clock amplitude is ≥ 200mV.

# +3.3V, 2.5Gbps, SDH/SONET 16:1 Serializer with Clock Synthesis and LVDS Inputs

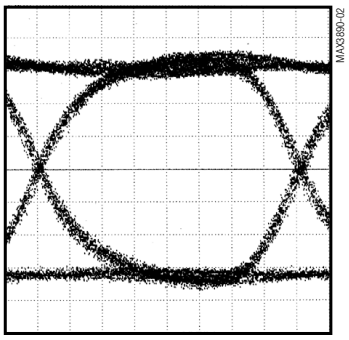
## Typical Operating Characteristics

($V_{CC}$ = +3.3V, PECL loads = 50Ω ±1%, $T_A$ = +25°C, unless otherwise noted.)

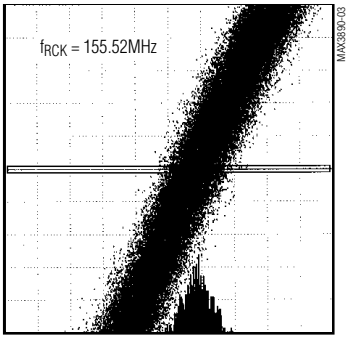
**SUPPLY CURRENT vs. TEMPERATURE**




**SERIAL-DATA OUTPUT EYE DIAGRAM**

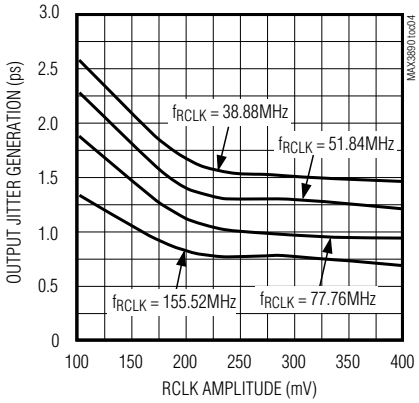



**SERIAL-DATA OUTPUT JITTER**




TOTAL WIDEBAND RMS JITTER = 2.155ps
PEAK-TO-PEAK JITTER = 15.7ps

**OUTPUT JITTER GENERATION vs. RCLK AMPLITUDE**



## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1, 17, 33, 48, 49, 63 | GND | Ground |
| 2, 5, 7, 10, 13, 14, 32, 56, 60, 64 | $V_{CC}$ | +3.3V Supply Voltage |
| 3 | SLBO- | System Loopback Inverting Output. Enabled when SOS is high. |
| 4 | SLBO+ | System Loopback Noninverting Output. Enabled when SOS is high. |
| 6 | SOS | System Loopback Output Select. System loopback disabled when low. |
| 8 | SCLKO- | Inverting PECL Serial Clock Output |
| 9 | SCLKO+ | Noninverting PECL Serial Clock Output |
| 11 | SDO- | Inverting PECL Serial-Data Output |
| 12 | SDO+ | Noninverting PECL Serial-Data Output |
| 15 | PCLKI+ | Noninverting LVDS Parallel Clock Input. Connect the incoming parallel-clock signal to the PCLKI inputs. Note that data is updated on the positive transition of the PCLKI signal. |
| 16 | PCLKI- | Inverting LVDS Parallel Clock Input. Connect the incoming parallel-clock signal to the PCLKI inputs. Note that data is updated on the positive transition of the PCLKI signal. |
| 18, 20, 22, 24, 26, 28, 30, 34, 36, 38, 40, 42, 44, 46, 50, 52 | PDI15+ to PDI0+ | Noninverting LVDS Parallel Data Inputs. Data is clocked on the PCLKI positive transition. |
| 19, 21, 23, 25, 27, 29, 31, 35, 37, 39, 41, 43, 45, 47, 51, 53 | PDI15- to PDI0- | Inverting LVDS Parallel Data Inputs. Data is clocked on the PCLKI positive transition. |
| 54 | PCLKO+ | Noninverting LVDS Parallel Clock Output. Use positive transition of PCLKO to clock the overhead management circuit. |
| 55 | PCLKO- | Inverting LVDS Parallel Clock Output. Use positive transition of PCLKO to clock the overhead management circuit. |
| 57 | RCLK+ | Noninverting LVDS Reference Clock Input. Connect an LVDS-compatible crystal reference clock to the RCLK inputs. |
| 58 | RCLK- | Inverting LVDS Reference Clock Input. Connect an LVDS-compatible crystal reference clock to the RCLK inputs. |
| 59 | CLKSET | Reference Clock Rate Programming Pin:<br>CLKSET = $V_{CC}$: Reference Clock Rate = 155.52MHz<br>CLKSET = Open: Reference Clock Rate = 77.76MHz<br>CLKSET = 20kΩ to GND: Reference Clock Rate = 51.84MHz<br>CLKSET = GND: Reference Clock Rate = 38.88MHz |
| 61 | FIL- | Filter Capacitor Input. Connect a 330nF capacitor between FIL+ and FIL-. |
| 62 | FIL+ | Filter Capacitor Input. Connect a 330nF capacitor between FIL+ and FIL-. |
| EP | Exposed Pad | Ground. This must be soldered to a circuit board for proper thermal performance (see *Package Information*). |

# +3.3V, 2.5Gbps, SDH/SONET 16:1 Serializer with Clock Synthesis and LVDS Inputs

## Detailed Description

The MAX3890 converts 16-bit-wide, 155Mbps data to 2.5Gbps serial data (Figure 1). It is composed of a 16-bit parallel input register, a 16-bit shift register, control and timing logic, PECL output buffers, LVDS input/output buffers, and a frequency-synthesizing PLL (consisting of a phase/frequency detector, loop filter/amplifier, voltage-controlled oscillator (VCO), and prescaler).

The PLL synthesizes an internal 2.5Gbps reference used to clock the output shift register. This clock is generated by locking onto the external 155.52MHz, 77.76MHz, 51.84MHz, or 38.88MHz reference-clock signal (RCLK).

The incoming parallel data is clocked into the MAX3890 on the rising transition of the parallel-clock-input signal (PCLKI). Proper operation is ensured if the parallel input register is latched within a window of time ($t_{SKEW}$) that is defined with respect to the parallel-clock-output signal (PCLKO). PCLKO is the synthesized 2.5Gbps internal serial-clock signal divided by 16. The allowable PCLKO-to-PCLKI skew is 0 to +4ns. This defines a timing window after the PCLKO rising edge, during which a PCLKI rising edge may occur (Figure 2).

### System Loopback

The MAX3890 is designed to allow system loopback testing. The loopback outputs (SLBO+, SLBO-) of the MAX3890 may be directly connected to the loopback inputs of a deserializer (such as the MAX3880) for system diagnostics. To enable the SLBO outputs, apply a TTL logic-high signal to the SOS input. **Note:** The same signal that controls the SOS enable input may also be used to control the SIS enable input on the MAX3880.

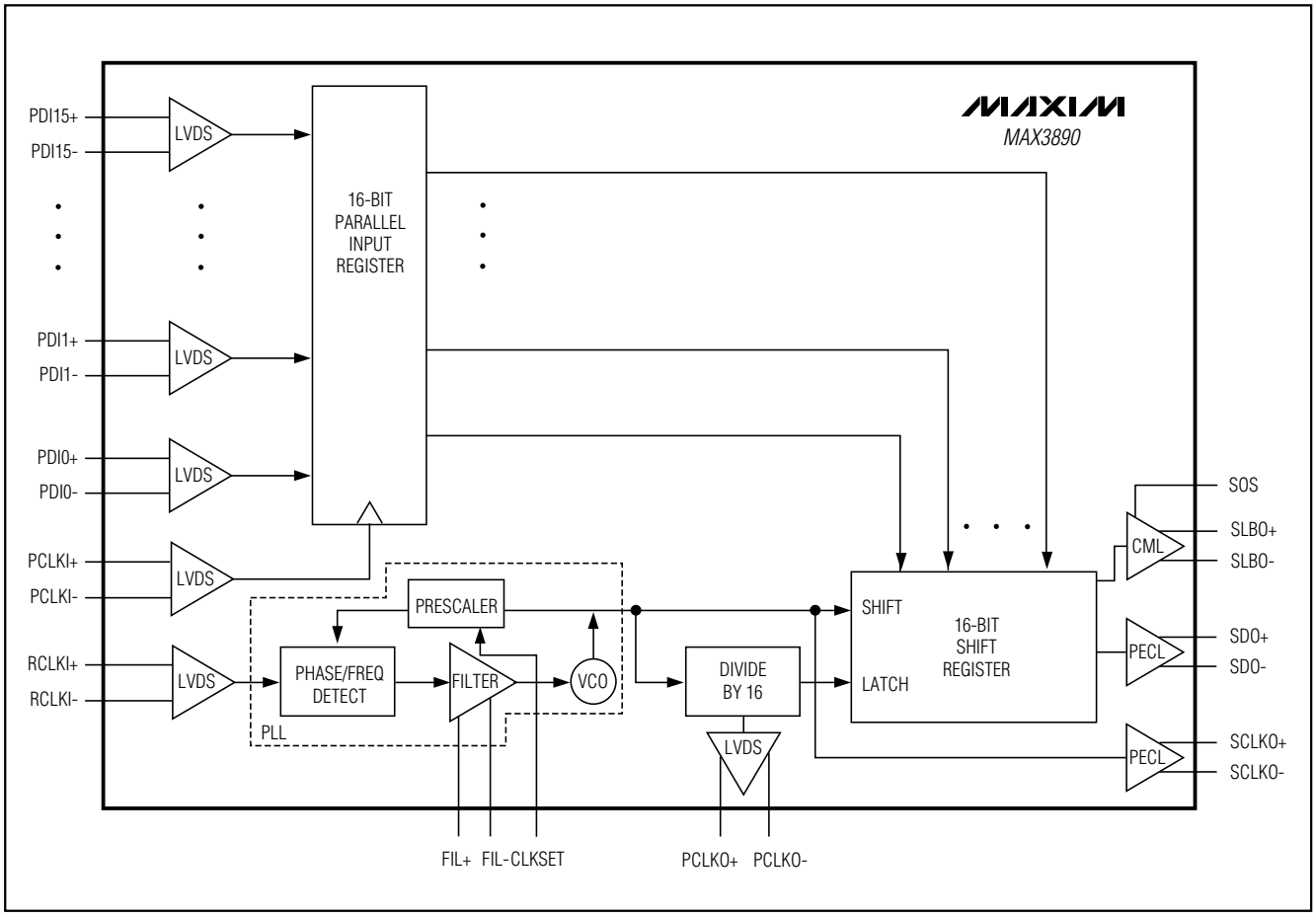
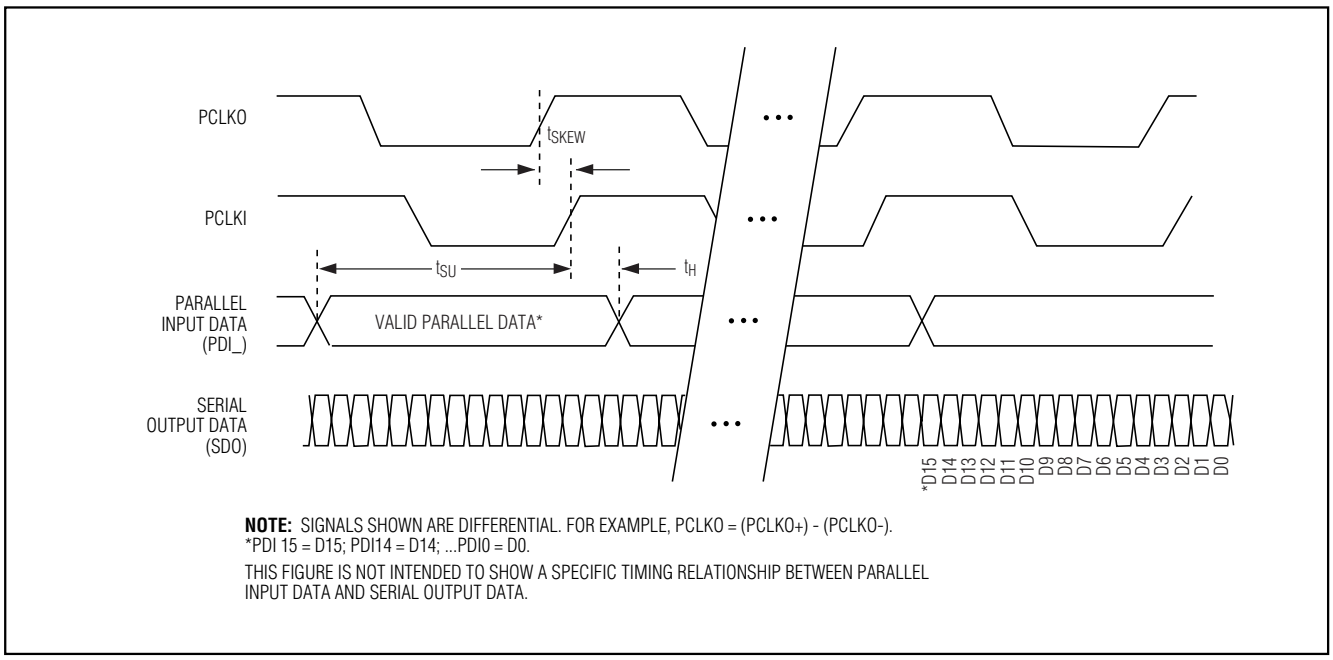



*Figure 1. Functional Diagram*




**NOTE:** SIGNALS SHOWN ARE DIFFERENTIAL. FOR EXAMPLE, PCLKO = (PCLKO+) - (PCLKO-).
*PDI 15 = D15; PDI14 = D14; ...PDI0 = D0.

THIS FIGURE IS NOT INTENDED TO SHOW A SPECIFIC TIMING RELATIONSHIP BETWEEN PARALLEL INPUT DATA AND SERIAL OUTPUT DATA.

*Figure 2. Timing Diagram*

### Low-Voltage Differential-Signal Inputs and Outputs

The MAX3890 has LVDS inputs and outputs for interfacing with high-speed digital circuitry. The LVDS standard is based on the IEEE 1596.3 LVDS specification. This technology uses 250mV to 400mV differential low-voltage swings to achieve fast transition times, minimized power dissipation, and noise immunity.

For proper operation, the parallel clock LVDS outputs (PCLKO+, PCLKO-) require 100Ω differential DC termination between the inverting and noninverting outputs. Do not terminate these outputs to ground.

The parallel data and parallel clock LVDS inputs (PDI_+, PDI_-, PCLKI+, PCLKI-, RCLK+, RCLK-) are internally terminated with 100Ω differential input resistance, and therefore do not require external termination.

### PECL Outputs

The serial-data PECL outputs (SDO+, SDO-, SCLKO+, SCLKO-) require 50Ω DC termination to ($V_{CC}$ - 2V) (see the *Alternative PECL-Output Termination* section).

### Current-Mode Logic Outputs

The system loopback outputs (SLBO+, SLBO-) of the MAX3890 are designed using CML. The configuration of the MAX3890 current-mode logic (CML) output circuit includes internal 50Ω back termination to $V_{CC}$ (Figure 3). These outputs are intended to drive a 50Ω transmission line terminated with a matched load impedance.

# +3.3V, 2.5Gbps, SDH/SONET 16:1 Serializer with Clock Synthesis and LVDS Inputs

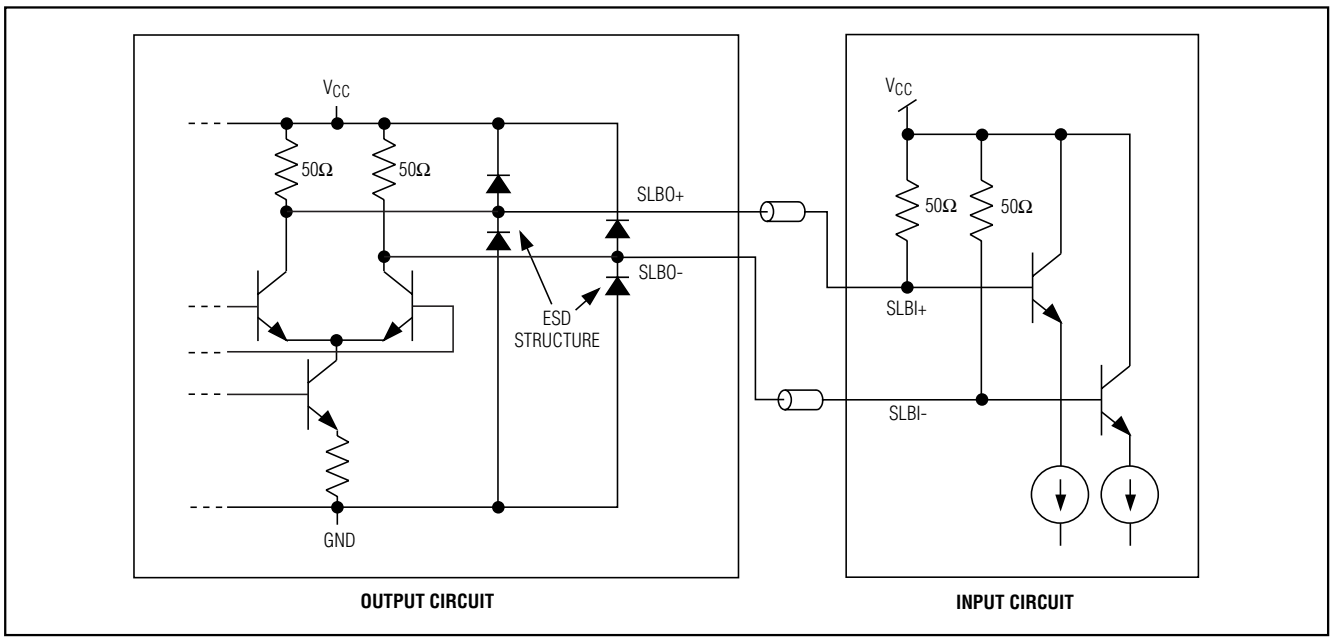



*Figure 3. Current-Mode Logic*

## Applications Information

### Alternative PECL-Output Termination

Figure 4 shows alternative PECL-output termination methods. Use Thevenin-equivalent termination when a ($V_{CC}$ - 2V) termination voltage is not available. If AC-coupling is necessary, be sure that the coupling capacitor is placed following the 50Ω or Thevenin-equivalent DC termination.

### Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies and keep ground connections short. Use multiple vias where possible. Also, use controlled-impedance transmission lines to interface with the MAX3890 clock and data inputs and outputs.

### Exposed Pad (EP) Package

The EP 64-pin TQFP incorporates features that provide a very low thermal resistance path for heat removal from the IC to a PC board. The MAX3890's exposed pad must be soldered directly to a ground plane with good thermal conductance.

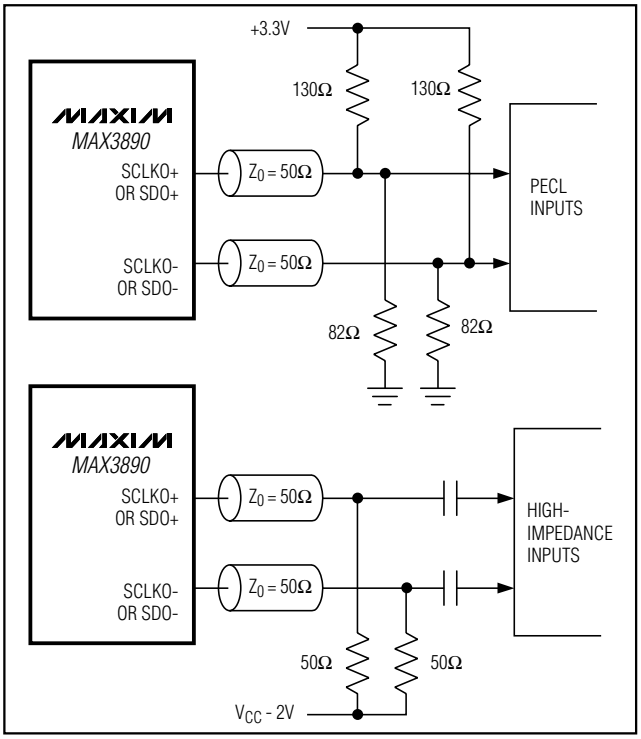



*Figure 4. Alternative PECL-Output Termination*

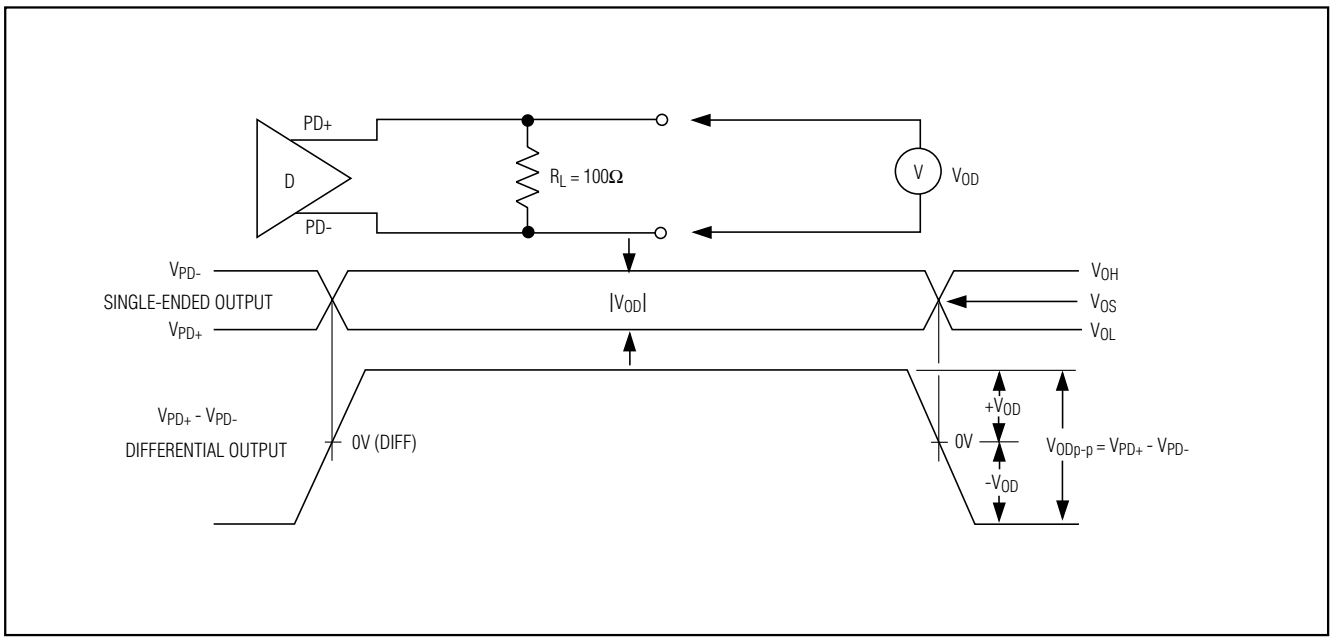
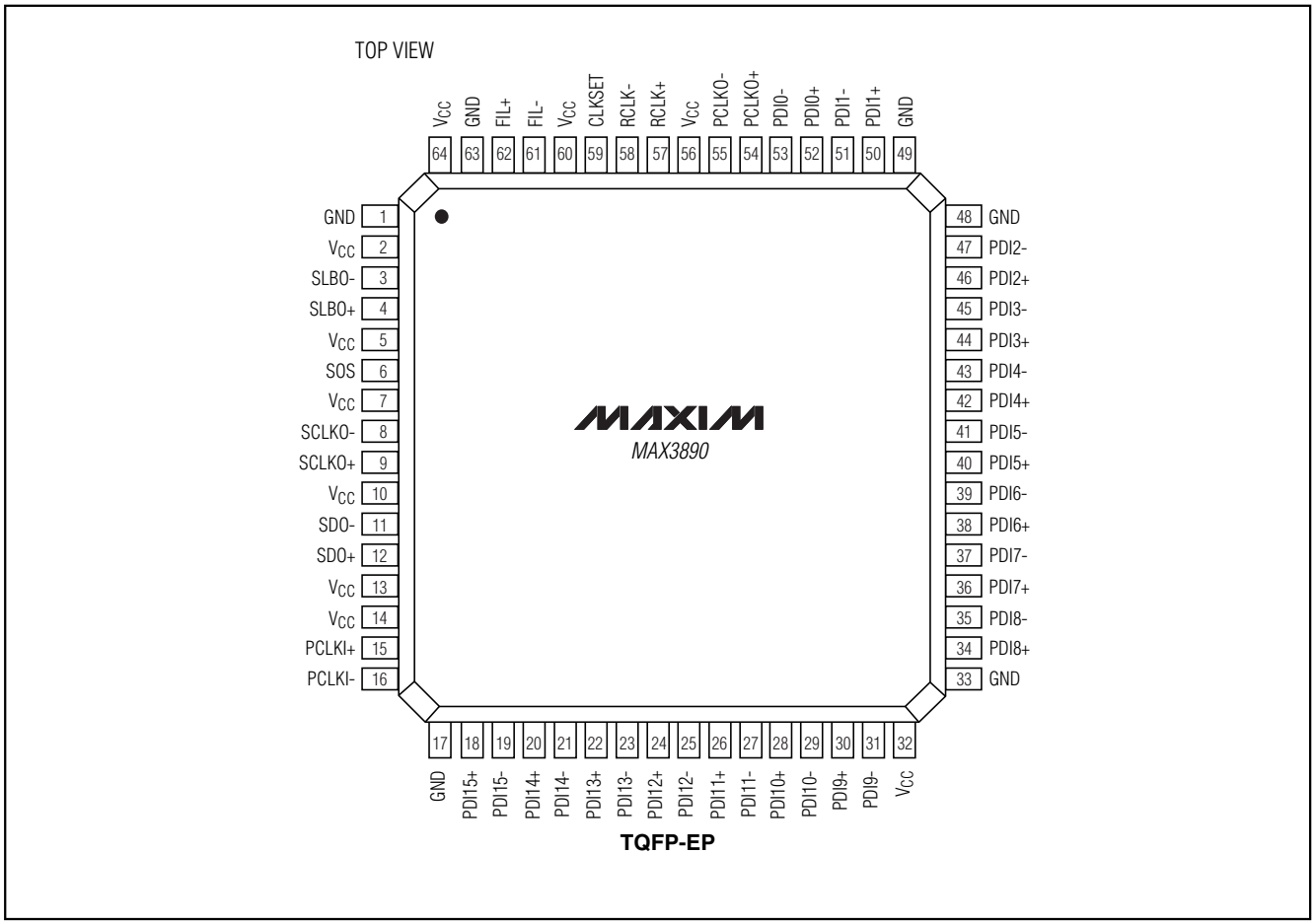



*Figure 5. Driver Output Levels*

# +3.3V, 2.5Gbps, SDH/SONET 16:1 Serializer with Clock Synthesis and LVDS Inputs

## Pin Configuration




**TQFP-EP**

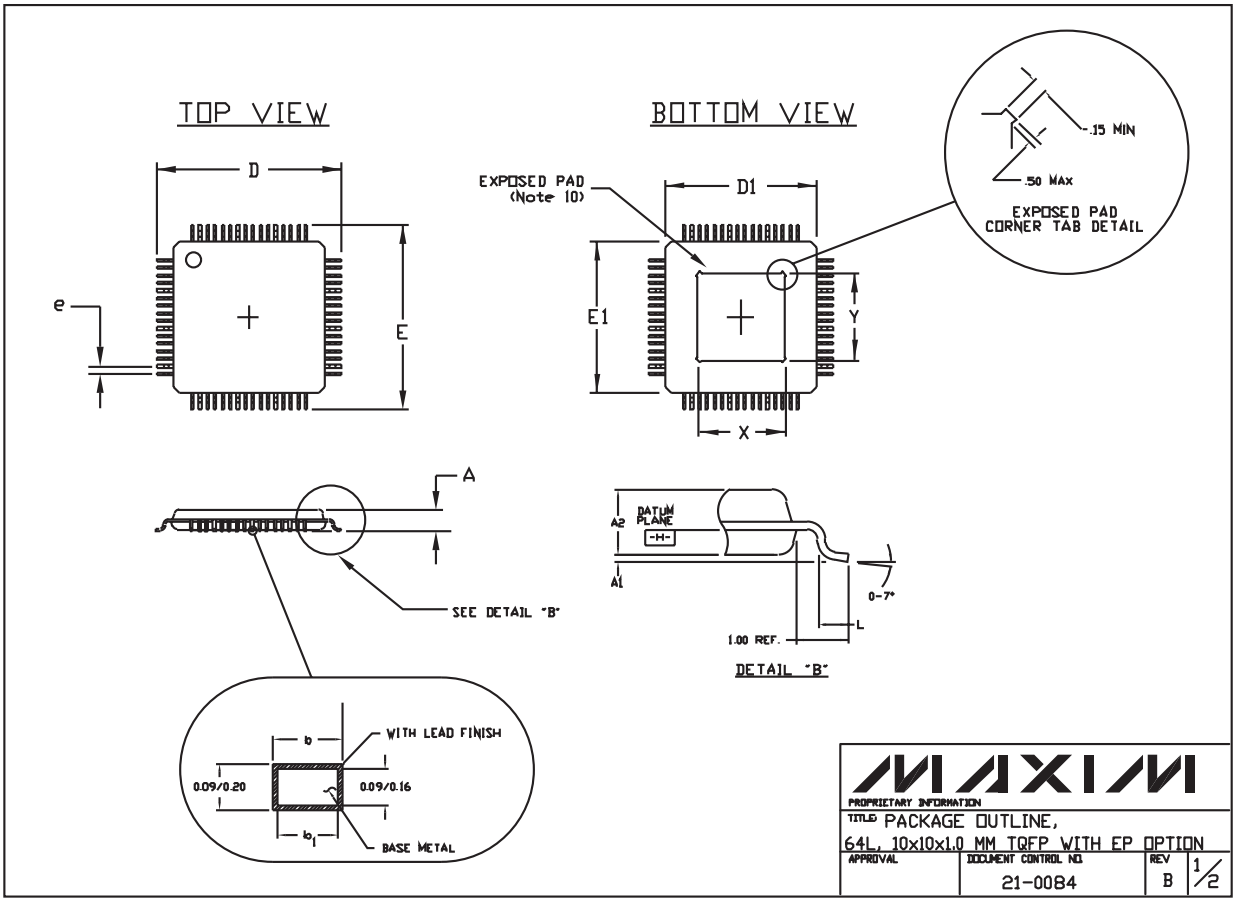
## Chip Information

TRANSISTOR COUNT: 4126

# +3.3V, 2.5Gbps, SDH/SONET 16:1 Serializer with Clock Synthesis and LVDS Inputs

## Package Information

64L, TQFP.EPS



# +3.3V, 2.5Gbps, SDH/SONET 16:1 Serializer with Clock Synthesis and LVDS Inputs

## Package Information (continued)

NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION AJ.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.

| SYMBOL | JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | |
|---|---|---|
| | AJ | |
| | MIN. | MAX. |
| A | — | 1.20 |
| $A_1$ | 0.05 | 0.15 |
| $A_2$ | 0.95 | 1.05 |
| D | 12.00 BSC. | |
| $D_1$ | 10.00 BSC. | |
| E | 12.00 BSC. | |
| $E_1$ | 10.00 BSC. | |
| L | 0.45 | 0.75 |
| N | 64 | |
| e | 0.50 BSC. | |
| b | 0.17 | 0.27 |
| $b_1$ | 0.17 | 0.23 |
| *X | 4.7 | 5.30 |
| *Y | 4.70 | 5.30 |

* EXPOSED PAD (Note 10)

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 64L, 10x10x1.0 MM TQFP WITH EP OPTION

| APPROVAL | DOCUMENT CONTROL NO. | REV | |
|---|---|---|---|
| | 21-0084 | B | 2/2 |

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