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FCH072N60F F085

N-Channel SuperFET II FRFET MOSFET 600 V, 52 A, 72 m Ω

Features

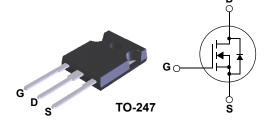
- Typical $R_{DS(on)}$ = 62 m Ω at V_{GS} = 10 V, I_D = 26 A
- Typical $Q_{q(tot)}$ = 160 nC at V_{GS} = 10V, I_D = 26 A
- UIS Capability
- Qualified to AEC Q101
- RoHS Compliant

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently SuperFETII is very well suited for the Soft switching

and Hard Switching topologies like High Voltage Full Bridge and Half Bridge DC-DC, Interleaved Boost PFC, Boost PFC for HEV-EV automotive.

SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



For current package drawing, please refer to the Fairchild website at https://www.fairchildsemi.com/package-drawings/TO/TO247A03.pdf

Application

- Automotive On Board Charger
- Automotive DC/DC converter for HEV



November 2014

Maximum Ratings $T_C = 25$ °C unless otherwise noted

Symbol	Parameter		Ratings	Units	
V_{DSS}	Drain to Source Voltage		600	V	
V_{GS}	Gate to Source Voltage		±20	V	
		T _C = 25°C	52	Α	
I _D	Drain Current - Continuous (V _{GS} =10) (Note 1)	T _C = 25°C T _C = 100°C	33	Α	
	Pulsed Drain Current		See Fig 4	Α	
E _{AS}	Single Pulse Avalanche Rating	(Note 2)	1128	mJ	
al/al4	MOSFET dv/dt		100	1//	
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	50	V/ns	
D	Power Dissipation		481	W	
P_{D}	Derate Above 25°C	3.85	W/°C		
T _J , T _{STG}	Operating and Storage Temperature		-55 to + 150	°C	
$R_{\theta JC}$	Maximum Thermal Resistance Junction to Case		0.26	°C/W	
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambie	ent (Note 4)	40	°C/W	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH072N60F	FCH072N60F_F085	TO-247	-	-	30

Notes:

- 1: Current is limited by bondwire configuration.
- 2: Starting $T_J = 25^{\circ}C$, L = 25mH, $I_{AS} = 9.5\text{A}$, $V_{DD} = 100\text{V}$ during inductor charging and $V_{DD} = 0\text{V}$ during time in avalanche.
- 3: $I_{SD} \le 26A$, di/dt ≤ 200 A/us, $V_{DD} \le 380V$, starting $T_J = 25$ °C.
- 4: R_{0,JA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0,JC} is guaranteed by design, while R_{0,JA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units		
Off Chai	Off Characteristics							

	B _{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$		600	-	-	V
	I _{DSS} Drain to Source Leakage Current	V _{DS} =600V,	$T_J = 25^{\circ}C$	-	-	10	μΑ	
IDSS Drain to Source Leaks	Diam to Source Leakage Current	$V_{GS} = 0V$	$T_J = 150^{\circ}C(Note 5)$	-	-	1	mA	
	I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V$		-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D}$	= 250μA	3.0	4.0	5.0	V
r _{DS(on)} Drain to Source On Resistance	Drain to Course On Desigtance	I _D = 26A,	$T_{J} = 25^{\circ}C$	-	62	72	mΩ
	$V_{GS} = 10V$	$T_J = 150^{\circ}C(Note 5)$	-	154	195	mΩ	

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 100V, V _{GS} = 0V, f = 1MHz	-	6330	-	pF
C _{oss}	Output Capacitance		-	199	-	pF
C _{rss}	Reverse Transfer Capacitance		1	1.25		pF
R_g	Gate Resistance	f = 1MHz	1	0.46		Ω
$Q_{g(ToT)}$	Total Gate Charge	V _{DD} = 380V I _D = 26A V _{GS} = 10V	-	160	210	nC
Q _{g(th)}	Threshold Gate Charge		-	11	16	nC
Q _{gs}	Gate to Source Gate Charge		-	34	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	67	-	nC

Switching Characteristics

t _{on}	Turn-On Time		-	75	100	ns
t _{d(on)}	Turn-On Delay Time		-	44	-	ns
t _r	Rise Time	V _{DD} = 380V, I _D = 26A,	-	31	-	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10V, R_{G} = 4.7\Omega$	-	128	-	ns
t _f	Fall Time		-	22	-	ns
t _{off}	Turn-Off Time		-	150	200	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	I_{SD} = 26A, V_{GS} = 0V	-	-	1.2	V
T _{rr}	Reverse Recovery Time	$I_F = 26A$, $dI_{SD}/dt = 100A/\mu s$	-	185	-	ns
Q_{rr}	Reverse Recovery Charge	V _{DD} = 480V	-	1515	1	nC

Note

5: The maximum value is specified by design at T_J = 150°C. Product is not tested to this condition in production.

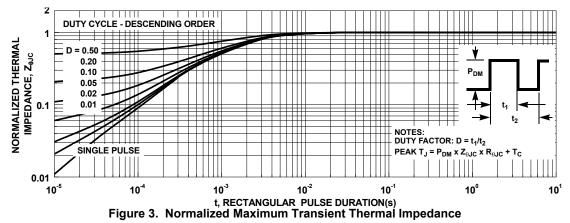
150

V_{GS} = 10V

Typical Characteristics 60 50 ID, DRAIN CURRENT (A) 40 30 20 10 0 0 75 100 150 50 75 100 125 T_C, CASE TEMPERATURE(°C) 25 T_C, CASE TEMPERATURE(°C)

Figure 1. Normalized Power Dissipation vs. Case **Temperature**

Figure 2. Maximum Continuous Drain Current vs. **Case Temperature**



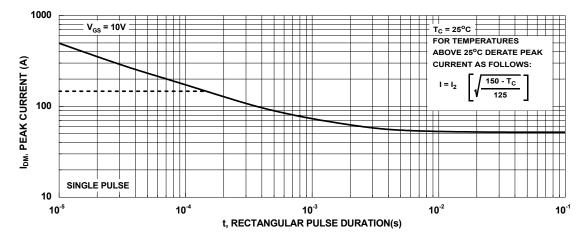


Figure 4. Peak Current Capability

Typical Characteristics

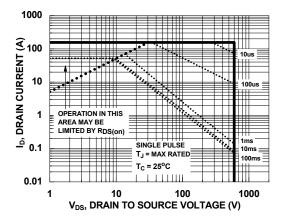


Figure 5. Forward Bias Safe Operating Area

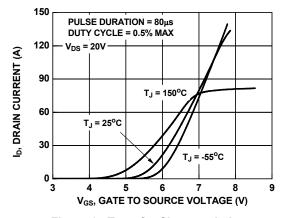


Figure 6. Transfer Characteristics

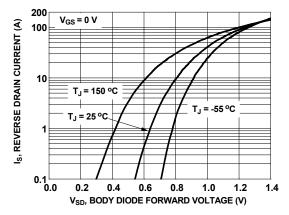


Figure 7. Forward Diode Characteristics

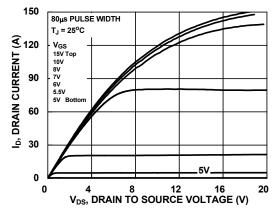


Figure 8. Saturation Characteristics

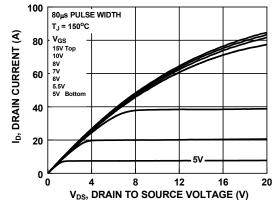


Figure 9. Saturation Characteristics

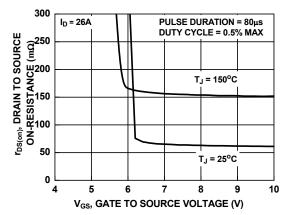


Figure 10. R_{DSON} vs. Gate Voltage

Typical Characteristics

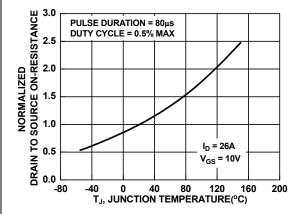


Figure 11. Normalized R_{DSON} vs. Junction Temperature

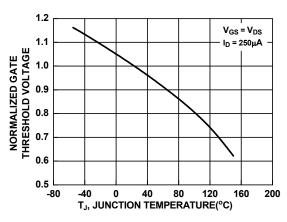


Figure 12. Normalized Gate Threshold Voltage vs.
Temperature

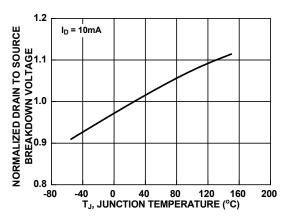


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

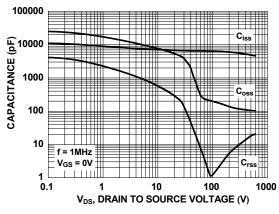


Figure 14. Capacitance vs. Drain to Source Voltage

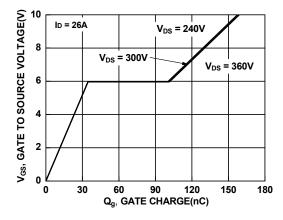


Figure 15. Gate Charge vs. Gate to Source Voltage

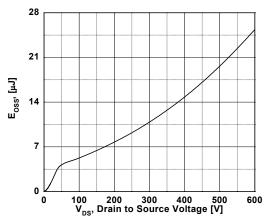


Figure 16. Eoss vs. Drain to Source Voltage

5

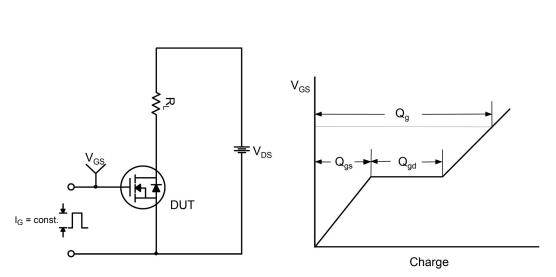


Figure 17. Gate Charge Test Circuit & Waveform

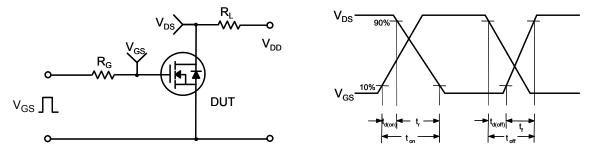


Figure 18. Resistive Switching Test Circuit & Waveforms

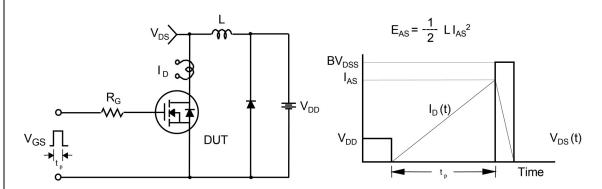
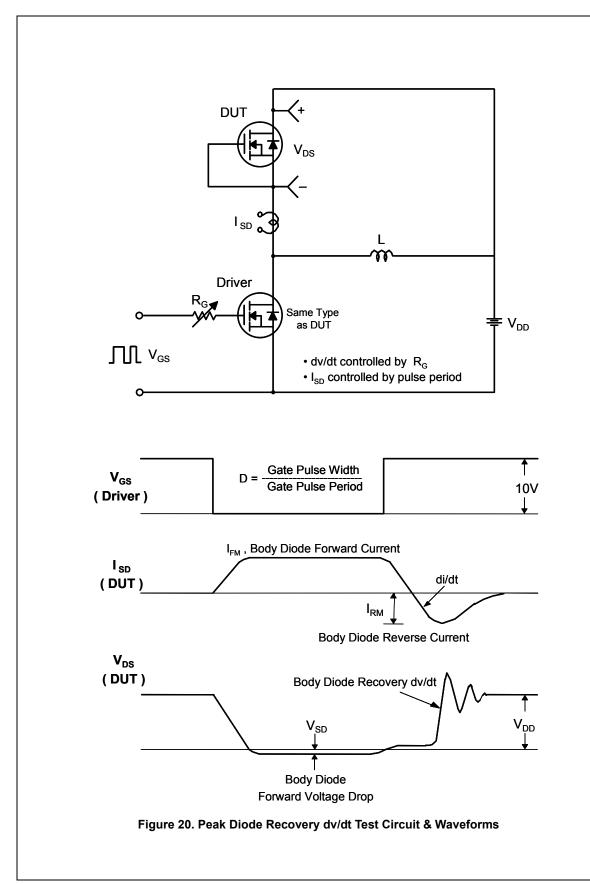
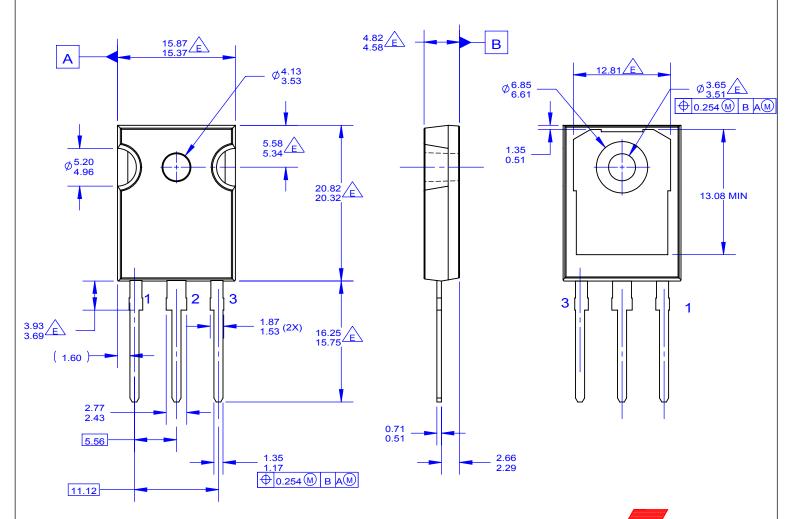


Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms







NOTES: UNLESS OTHERWISE SPECIFIED.

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