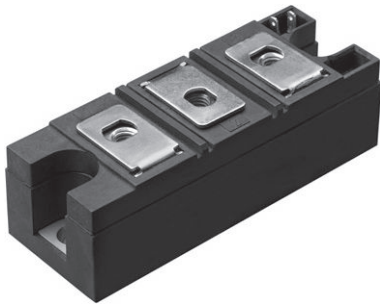


INT-A-PAK Power Module Thyristor/Diode, 300 A


INT-A-PAK

FEATURES

- Electrically isolated base plate
- 3000 V_{RMS} isolating voltage
- Industrial standard package
- Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- UL approved file E78996
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

APPLICATIONS

- Battery chargers
- Welders
- Power converters
- Alternators

PRODUCT SUMMARY	
$I_{T(AV)}$	300 A
Type	Modules - Thyristor, Standard
Package	INT-A-PAK
Circuit	SCR/diode doubler circuit, negative control

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
V_{DRM}/V_{RRM}		800	V
$I_{T(AV)}$	53 °C	300	A
I_{TSM}	50 Hz	6500	A
	60 Hz	6900	
I^2t	50 Hz	214	kA ² s
	60 Hz	195	
$I^2\sqrt{t}$		2140	kA ² √s
T_J	Range	-40 to 140	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS			
TYPE NUMBER	V_{RRM}/V_{DRM} , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM}/V_{DSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} AT 125 °C mA
VS-VSKL300/08PbF	800	900	50



ON-STATE CONDUCTION					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction half sine wave		300	A
				53	°C
Maximum RMS on-state current	$I_{T(RMS)}$	As AC switch		116	A
Maximum peak, one-cycle on-state, non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reappplied	6600	
		t = 8.3 ms		6900	
		t = 10 ms	100 % V_{RRM} reappplied	5500	
		t = 8.3 ms		5800	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reappplied	214	
		t = 8.3 ms		195	
		t = 10 ms	100 % V_{RRM} reappplied	151	
		t = 8.3 ms		138	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reappplied		2140	kA ² √s
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$), T_J maximum		0.796	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > $\pi \times I_{T(AV)}$), T_J maximum		0.868	
Low level value on-state slope resistance	r_{t1}	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$), T_J maximum		0.972	mΩ
High level value on-state slope resistance	r_{t2}	(I > $\pi \times I_{T(AV)}$), T_J maximum		0.88	
Maximum on-state voltage drop	V_{TM}	$T_J = 25\text{ °C}$, 500 A I_{pk}	SCR	1.35	V
	V_{FM}		DIODE	1.20	

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Typical delay time	t_d	Gate current 1 A, $dI_g/dt = 1\text{ A}/\mu\text{s}$ $V_d = 0.67\% V_{DRM}$, $T_J = 25\text{ °C}$		1.0	μs
Typical turn-off time	t_q	$I_{TM} = 300\text{ A}$, $T_J = T_J$ maximum, $dI/dt = 20\text{ A}/\mu\text{s}$, $V_R = 50\text{ V}$ $dV/dt = 20\text{ V}/\mu\text{s}$, Gate 0 V 100 Ω, $t_p = 500\text{ μs}$		100	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 67 % rated V_{DRM}		500	V/μs
Maximum peak reverse and off-state leakage current	I_{DRM} , I_{RRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied		50	mA
RMS insulation voltage	V_{INS}	50 Hz, circuit to base, all terminal shorted, t = 1 s		3000	V



TRIGGERING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10.0	W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	2.0	
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	3.0	A
Maximum required DC gate voltage to trigger	V_{GT}	$T_J = 25$ °C Anode supply: 12 V resistive load	3	V
Maximum required DC gate current to trigger	I_{GT}		200	mA
Maximum holding current	I_H		600	
Maximum peak positive gate voltage	$+V_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	20	V
Maximum peak negative gate voltage	$-V_{GM}$		5.0	
DC gate voltage not to trigger	V_{GD}	$T_J = T_J$ maximum Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode to cathode applied	0.30	V
DC gate current not to trigger	I_{GD}		10	mA
Maximum non-repetitive rate of rise of turned-on current	di/dt	Gate drive 20 V, 20 Ω , $t_r \leq 1$ μ s $T_J = T_J$ maximum, anode voltage $\leq 80\%$ V_{DRM}	1000	A/ μ s

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	T_J		-40 to 140	°C
Maximum storage temperature range	T_{Stg}		-40 to 150	
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	0.19	K/W
Maximum thermal resistance, case to heatsink per module	R_{thCS}	Mounting surface smooth, flat and greased	0.035	
Mounting torque $\pm 10\%$	IAP to heatsink	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound. Lubricated threads.	4 to 6	Nm
	busbar to IAP			
Approximate weight			500	g
			17.8	oz.
Case style				INT-A-PAK

ΔR CONDUCTION PER JUNCTION											
DEVICES	SINUSOIDAL CONDUCTION AT T_J MAXIMUM					RECTANGULAR CONDUCTION AT T_J MAXIMUM					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VSKL300	0.019	0.022	0.028	0.041	0.068	0.013	0.023	0.031	0.043	0.069	K/W

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

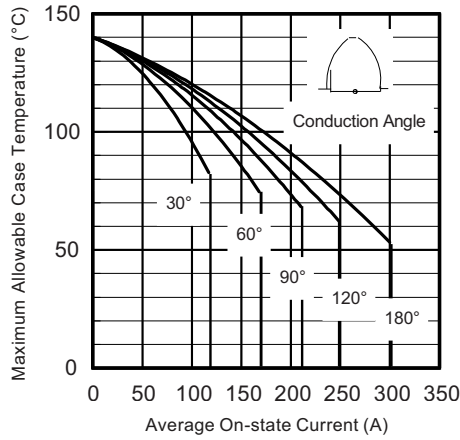


Fig. 1 - Current Ratings Characteristics

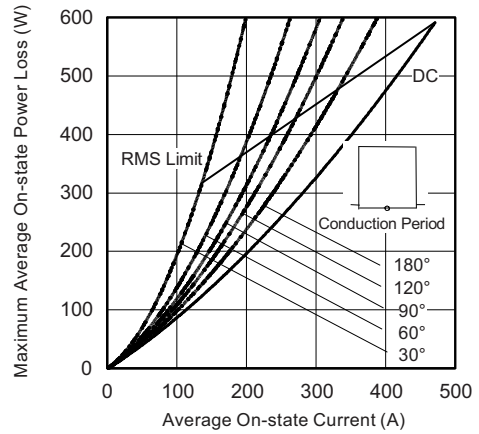


Fig. 4 - On-State Power Loss Characteristics

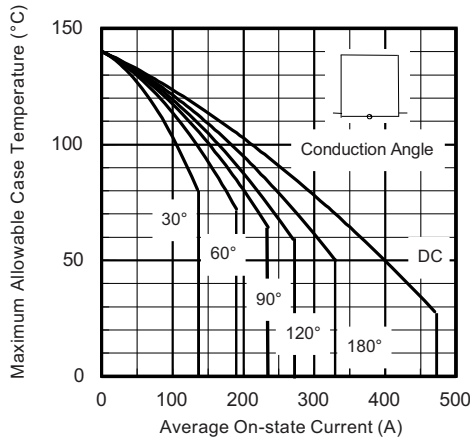


Fig. 2 - Current Ratings Characteristics

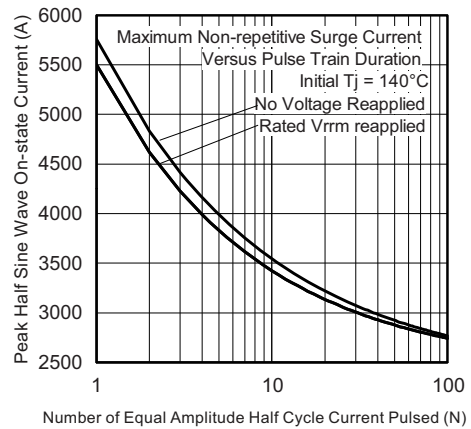


Fig. 5 - Maximum Non-Repetitive Surge Current

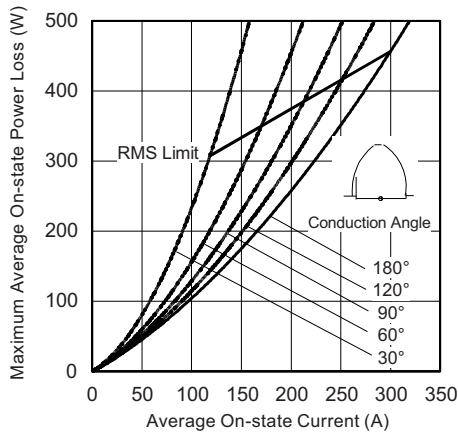


Fig. 3 - On-State Power Loss Characteristics

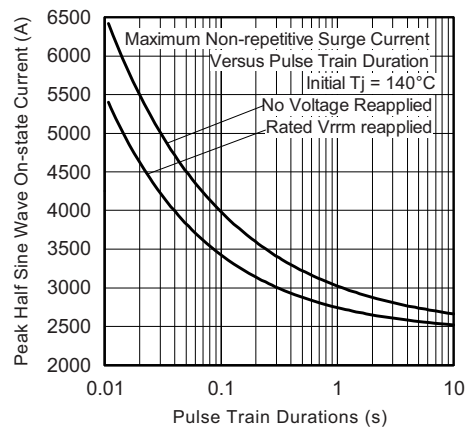


Fig. 6 - Maximum Non-Repetitive Surge Current

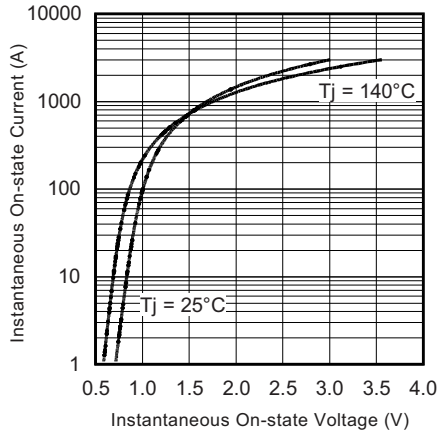


Fig. 7 - On-State Voltage Drop Characteristics (SCR)

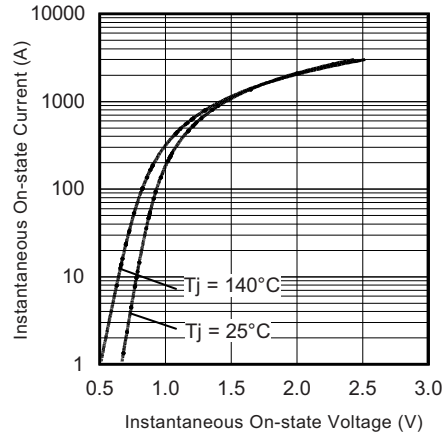


Fig. 8 - On-State Voltage Drop Characteristics (Diode)

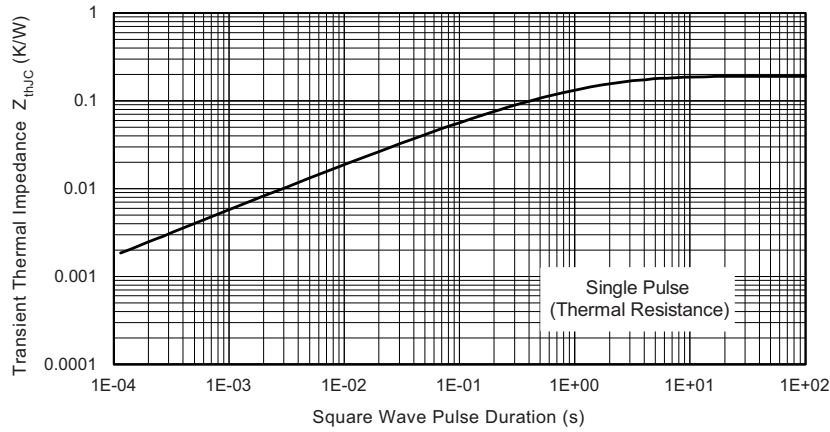


Fig. 9 - Thermal Impedance Z_{thJC} Characteristics

ORDERING INFORMATION TABLE

Device code	VS-VS	KL	300	08	PbF
	①	②	③	④	⑤
	1	-	Vishay Semiconductors product		
	2	-	Circuit configuration		
	3	-	Current rating (300 = 300 A)		
	4	-	Voltage rating (08 = 800 V)		
	5	-	PbF = Lead (Pb)-free		

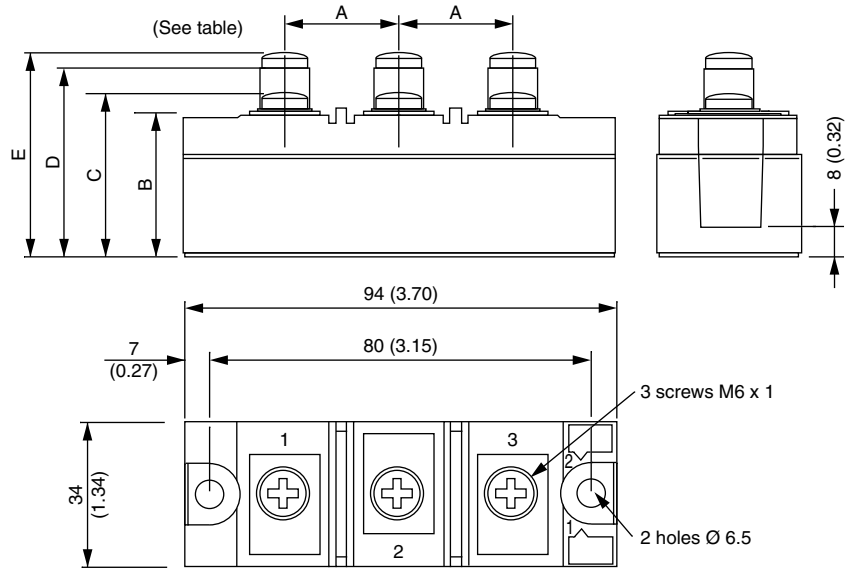


CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
SCR/diode doubler circuit, negative control	L	

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95010

INT-A-PAK Diode

DIMENSIONS in millimeters (inches)



A	B	C	D	E
23 (0.91)	30 (1.18)	36 (1.42)	-	-



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