

1. General description

Planar passivated high commutation three quadrant triac in a TO252 (DPAK) surface mountable plastic package. This triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers. This "series ET" triac will commutate the full rated RMS current at the maximum rated junction temperature ($T_{j(max)} = 150\text{ °C}$) without the aid of a snubber.

2. Features and benefits

- High voltage capability
- High commutation capability with maximum false trigger immunity
- Direct interfacing with low level power drivers and logic ICs
- High junction operating temperature capability ($T_{j(max)} = 150\text{ °C}$)
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only
- Sensitive gate for easy logic level triggering
- Surface mountable package

3. Applications

- Compressor starting control circuits
- General purpose motor controls
- Reversing induction motor controls e.g. vertical axis washing machines
- Applications subject to high temperature ($T_{j(max)} = 150\text{ °C}$)

4. Quick reference data

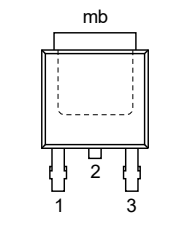
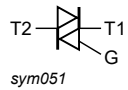
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 131\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	60	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	-	65	A
T_j	junction temperature		-	-	150	°C
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7	-	-	10	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2+ \text{ G-}; T_j = 25\text{ }^\circ\text{C}; \text{ Fig. 7}$	-	-	10	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2- \text{ G-}; T_j = 25\text{ }^\circ\text{C}; \text{ Fig. 7}$	-	-	10	mA
I_H	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{ Fig. 9}$	-	-	30	mA
V_T	on-state voltage	$I_T = 10\text{ A}; T_j = 25\text{ }^\circ\text{C}; \text{ Fig. 10}$	-	1.3	1.65	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}; T_j = 125\text{ }^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM}); \text{ exponential waveform; gate open circuit}$	400	-	-	V/ μs
		$V_{DM} = 536\text{ V}; T_j = 150\text{ }^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM}); \text{ exponential waveform; gate open circuit}$	200	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}; T_j = 150\text{ }^\circ\text{C}; I_{T(RMS)} = 8\text{ A}; dV_{com}/dt = 20\text{ V}/\mu\text{s}; \text{ snubberless condition; gate open circuit; Fig. 12}$	3	-	-	A/ms
		$V_D = 400\text{ V}; T_j = 150\text{ }^\circ\text{C}; I_{T(RMS)} = 8\text{ A}; dV_{com}/dt = 10\text{ V}/\mu\text{s}; \text{ gate open circuit}$	4	-	-	A/ms
		$V_D = 400\text{ V}; T_j = 150\text{ }^\circ\text{C}; I_{T(RMS)} = 8\text{ A}; dV_{com}/dt = 1\text{ V}/\mu\text{s}; \text{ gate open circuit}$	6	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>DPAK (TO252N)</p>	 <p>sym051</p>
2	T2	main terminal 2		
3	G	gate		
mb	T2	mounting base; main terminal 2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BTA308S-800ET	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	TO252N

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 131\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	60	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	65	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	18	A ² s
di_T/dt	rate of rise of on-state current	$I_G = 20\text{ mA}$	-	100	A/ μ s
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	150	°C

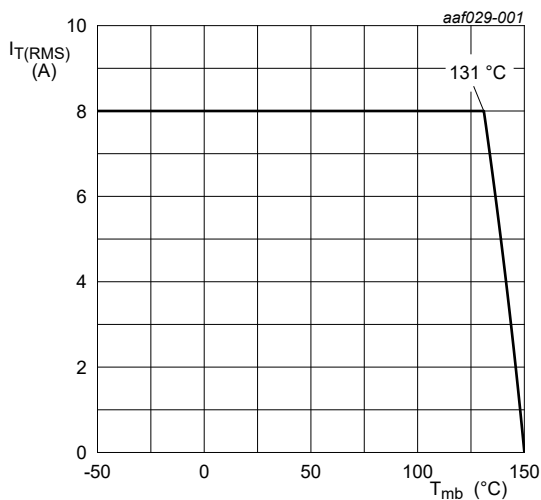
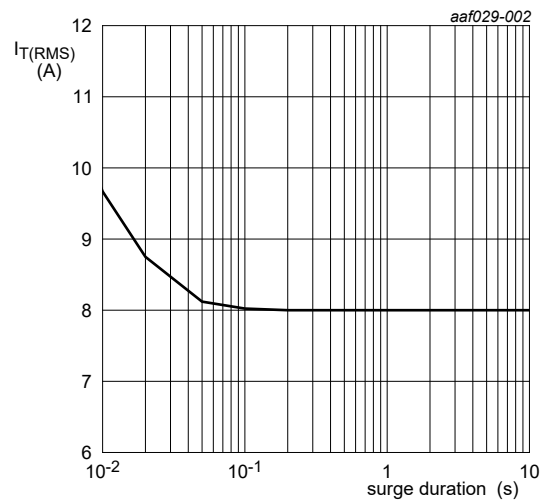


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



$f = 50\text{ Hz}$; $T_{mb} = 131\text{ °C}$

Fig. 2. RMS on-state current as a function of surge duration; maximum values

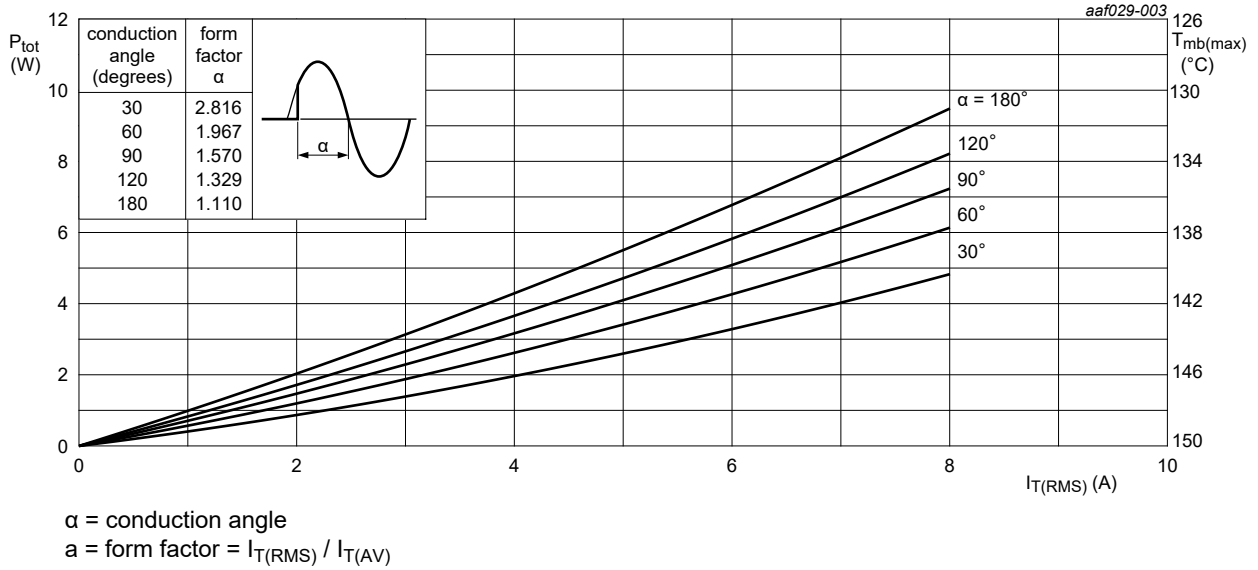


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

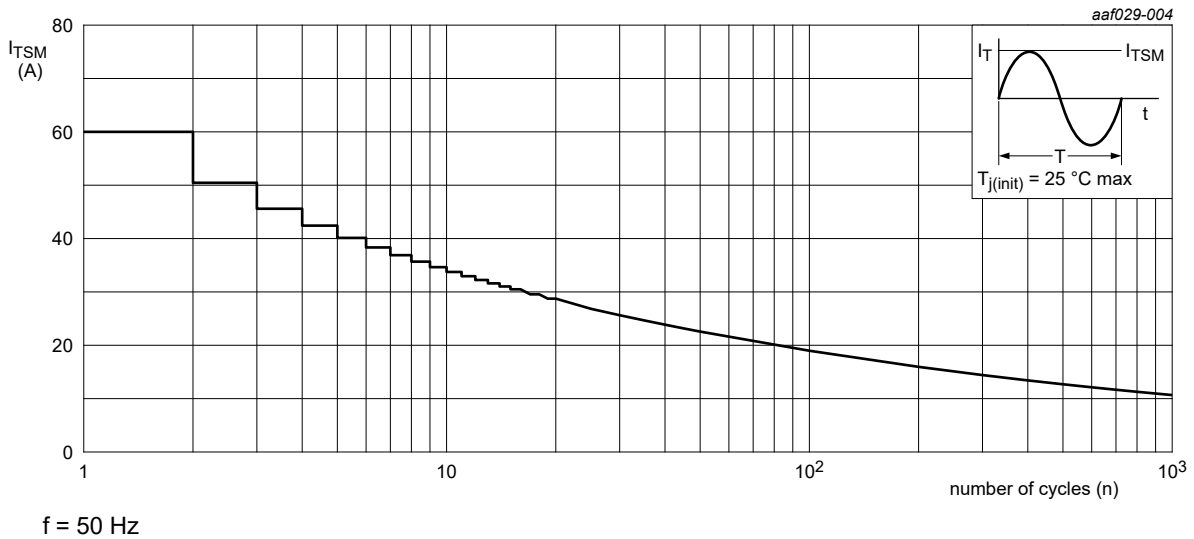
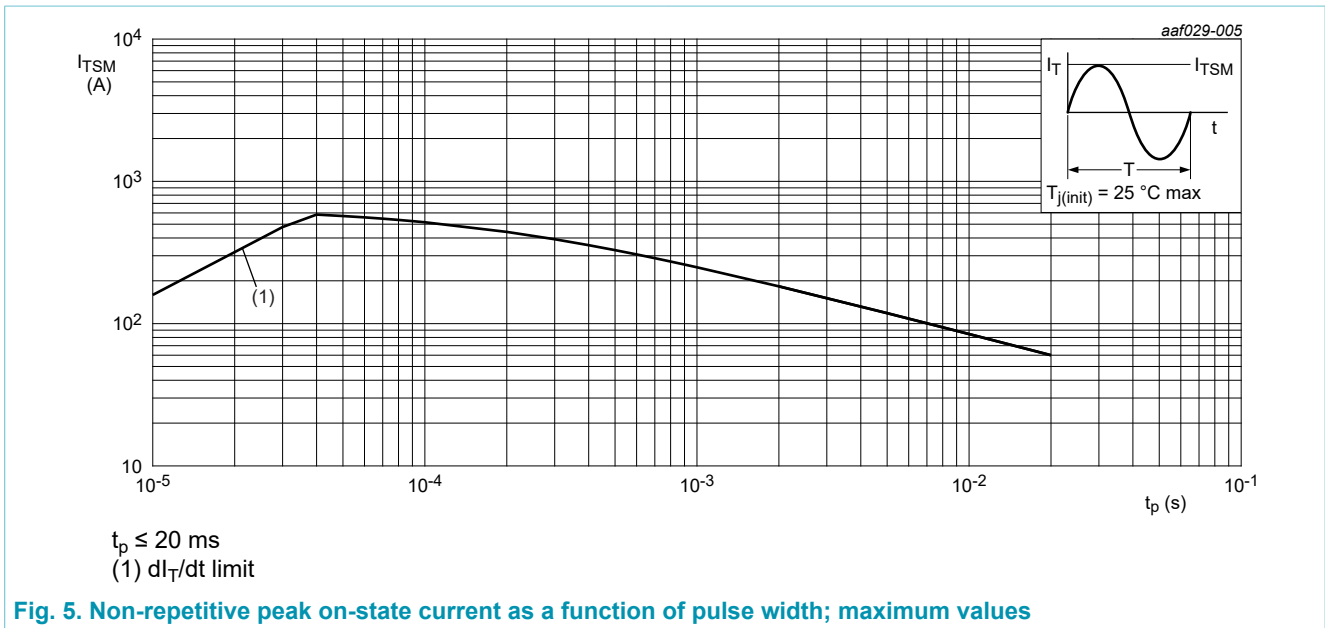


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6	-	-	2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board (FR4) mounted	-	75	-	K/W

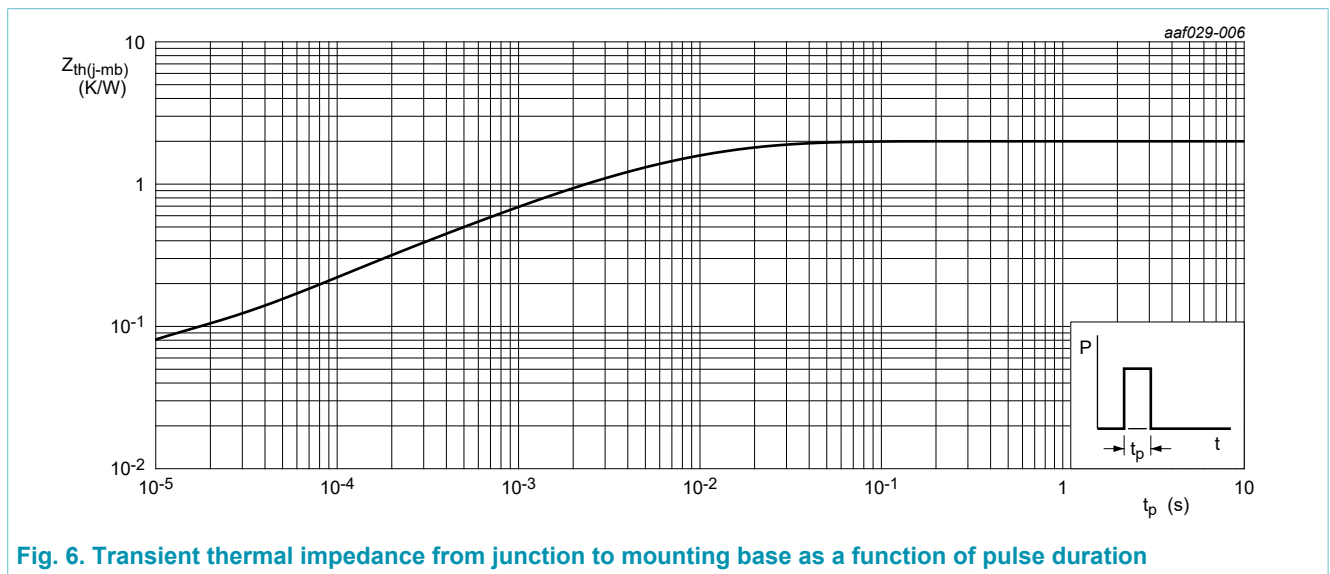
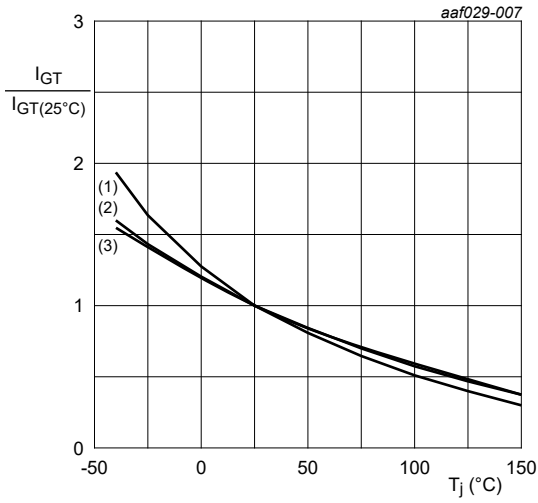


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 7	-	-	10	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 7	-	-	10	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; Fig. 7	-	-	10	mA
I _L	latching current	V _D = 12 V; I _G = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 8	-	-	50	mA
		V _D = 12 V; I _G = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 8	-	-	75	mA
		V _D = 12 V; I _G = 0.1 A; T2- G-; T _j = 25 °C; Fig. 8	-	-	50	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 9	-	-	30	mA
V _T	on-state voltage	I _T = 10 A; T _j = 25 °C; Fig. 10	-	1.3	1.65	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11	-	0.7	1	V
		V _D = 400 V; I _T = 0.1 A; T _j = 150 °C; Fig. 11	0.2	0.45	-	V
I _D	off-state current	V _D = 800 V; T _j = 25 °C	-	-	10	μA
		V _D = 800 V; T _j = 150 °C	-	-	0.5	mA
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	400	-	-	V/μs
		V _{DM} = 536 V; T _j = 150 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	200	-	-	V/μs
di _{com} /dt	rate of change of commutating current	V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 8 A; dV _{com} /dt = 20 V/μs; snubberless condition; gate open circuit; Fig. 12	3	-	-	A/ms
		V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 8 A; dV _{com} /dt = 10 V/μs; gate open circuit	4	-	-	A/ms
		V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 8 A; dV _{com} /dt = 1 V/μs; gate open circuit	6	-	-	A/ms



- (1) T2- G-
- (2) T2+ G-
- (3) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

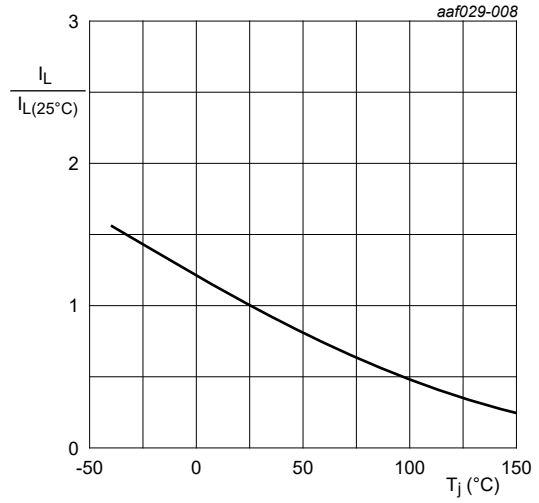


Fig. 8. Normalized latching current as a function of junction temperature

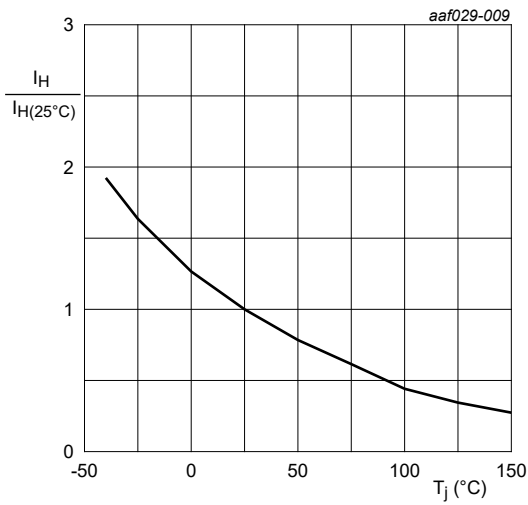
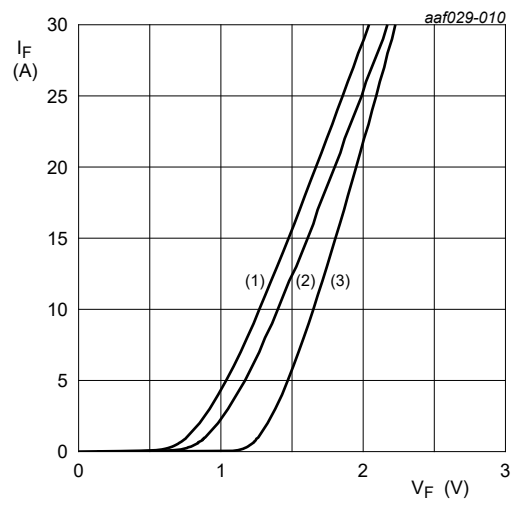


Fig. 9. Normalized holding current as a function of junction temperature



- $V_o = 1.067 \text{ V}; R_s = 0.0281 \ \Omega$
- (1) $T_j = 150 \text{ }^\circ\text{C}$; typical values
 - (2) $T_j = 150 \text{ }^\circ\text{C}$; maximum values
 - (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

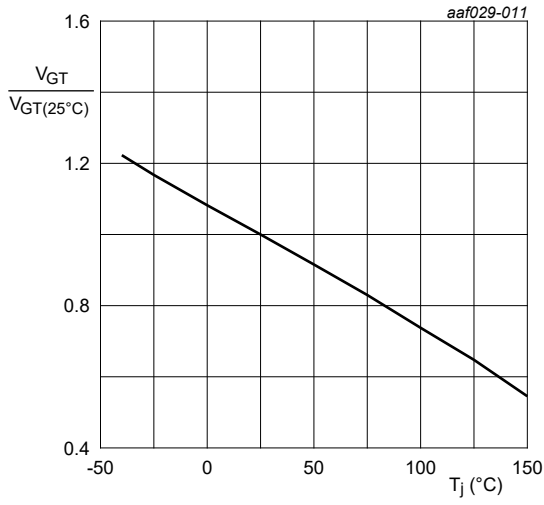


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

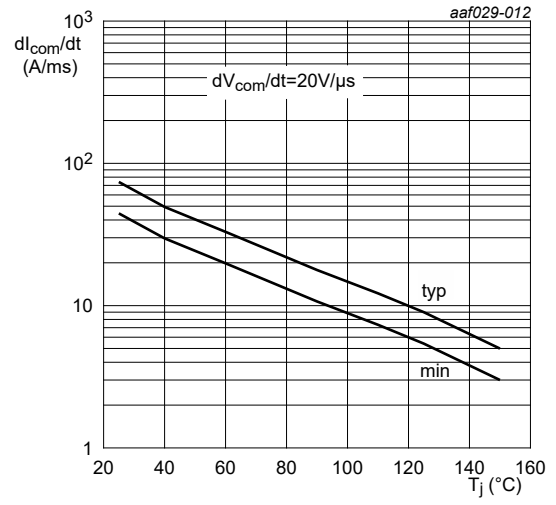


Fig. 12. Rate of change of commutating current as a function of junction temperature; typical and minimum values

10. Package outline

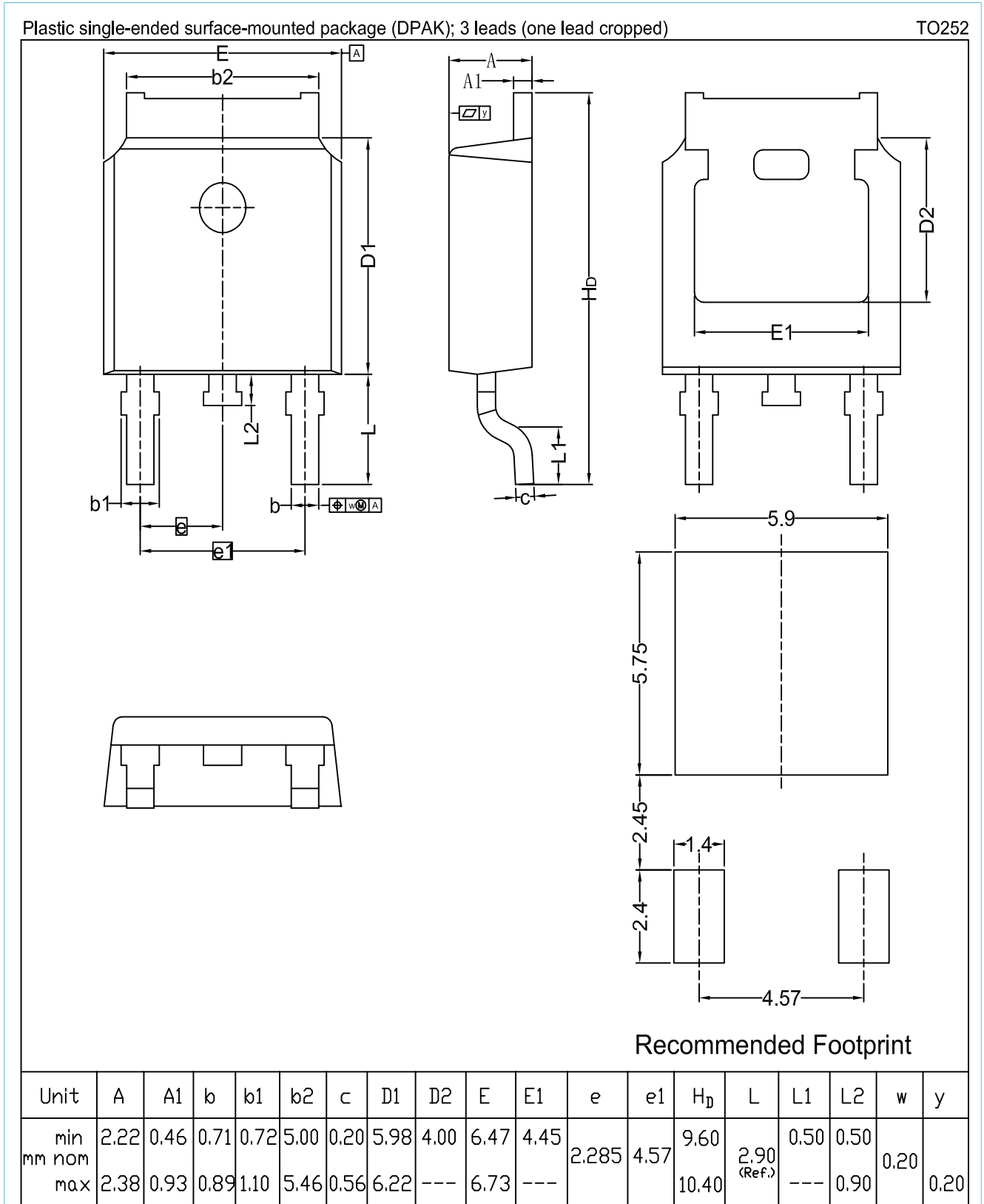


Fig. 13. Package outline DPAK (TO252N)

11. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 14 July 2017

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Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

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