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December 2013

### **FCH47N60**

# N-Channel SuperFET® MOSFET

600 V, 47 A, 70 m $\Omega$ 

#### **Features**

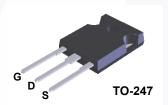
- 650 V @ T<sub>J</sub> = 150°C
- Typ.  $R_{DS(on)}$  = 58 m $\Omega$
- Ultra Low Gate Charge (Typ. Q<sub>g</sub> = 210 nC)
- Low Effective Output Capacitance (Typ. C<sub>oss(eff.)</sub> = 420 pF)
- 100% Avalanche Tested
- · RoHS Compliant

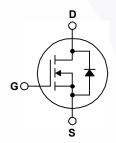
### **Applications**

- · Solar Inverter
- · AC-DC Power Supply

### Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low onresistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.





### MOSFET Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FCH47N60_F133	Unit
V <sub>DSS</sub>	Drain to Source Voltage		600	V
. \	Drain Current	Continuous (T <sub>C</sub> = 25°C)	47	Α
ID	Drain Current	Continuous (T <sub>C</sub> = 100°C)	29.7	_ A
I <sub>DM</sub>	Drain Current	Pulsed (Note 1)	141	Α
V <sub>GSS</sub>	Gate to Source Voltage		±30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)		1800	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)		47	Α
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1		41.7	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
В	Power Dissipation	(T <sub>C</sub> = 25°C)	417	W
$P_{D}$	Power Dissipation	Derate Above 25°C	3.33	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Tempe	rature Range	-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature 1 1/8" from Case for 5 Seconds	or Soldering,	300	°C

#### **Thermal Characteristics**

Symbol	Parameter	FCH47N60_F133	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Case-to-Sink, Typ.	0.24	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	41.7	°C/W

### **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH47N60_F133	FCH47N60	TO-247	Tube	N/A	N/A	30 units

### **Electrical Characteristics** $T_C = 25$ °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
Decis to Course Bookletows Valteres	Drain to Source Prockdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}, T_C = 25^{\circ}\text{C}$	600	-	-	V
BV <sub>DSS</sub> Drain-to-Source Breakdown Voltage		$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}, T_C = 150^{\circ}\text{C}$	-	650	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	-	0.6	-	V/°C
BV <sub>DS</sub>	Drain to Source Avalanche Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 47 A	-	700	-	V
ı	Zoro Cata Voltago Drain Current	$V_{DS} = 600 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°C	-	-	10	μA
I <sub>GSS</sub>	Gate-to-Body Leakage Current	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V	-	-	±100	nA

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain-to-Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 23.5 \text{ A}$	-	0.058	0.070	Ω
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_{D} = 23.5 \text{ A}$	-	40	-	S

### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 05.V.V 0.V	-	5900	8000	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		3200	4200	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			250	-	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	-	160	-	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	-	420	-	pF

### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay		-	185	430	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 300 \text{ V}, I_{D} = 47 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{G} = 25 \Omega$		210	450	ns
t <sub>d(off)</sub>	Turn-Off Delay			520	1100	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note	4) -	75	160	ns
Q <sub>g(tot)</sub>	Total Gate Charge at 10 V	V <sub>DS</sub> = 480 V. I <sub>D</sub> = 47 A.		210	270	nC
$Q_{gs}$	Gate to Source Gate Charge	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 47 A, V <sub>GS</sub> = 10 V	-	38	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	(Note	4) _	110	-	nC

#### **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain-to-Source Diode Forward Current		-	-	47	Α
I <sub>SM</sub>	Maximum Pulsed Drain-to-Source Diode Forward Current		-	-	141	Α
$V_{SD}$	Drain-to-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 47 A	-	-	1.4	V
t <sub>rr</sub>	Reverse-Recovery Time	$V_{GS} = 0 \text{ V, } I_{SD} = 47 \text{ A,}$ $dI_F/dt = 100 \text{ A/}\mu\text{s}$	-	590	-	ns
Q <sub>rr</sub>	Reverse-Recovery Charge	dI <sub>F</sub> /dt = 100 A/μs	_	25	-	μС

#### Notes:

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. I $_{AS}$  = 18 A, V $_{DD}$  = 50 V, R $_{G}$  = 25  $\Omega$ , starting T $_{J}$  = 25°C.
- 3.  $I_{SD} \le 48$  A, di/dt  $\le 200$  A/ $\mu$ s,  $V_{DD} \le BV_{DSS}$ , starting  $T_J$  = 25°C.
- 4. Essentially independent of operating temperature.

### **Typical Performance Characteristics**

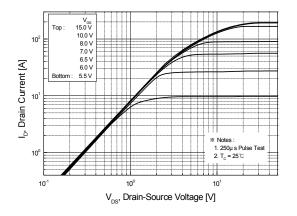


Figure 1. On-Region Characteristics

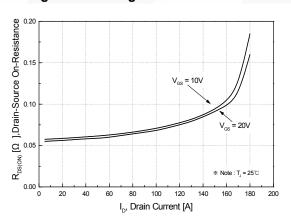


Figure 2. Transfer Characteristics

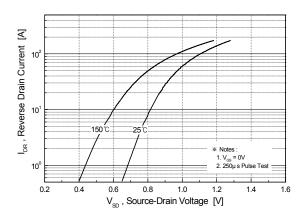


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

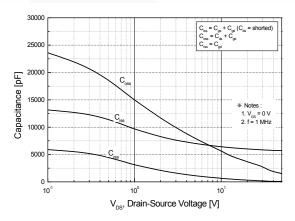


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

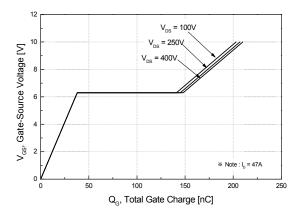
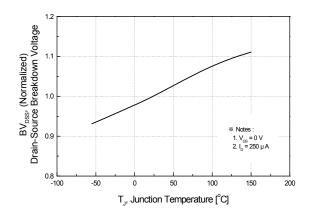


Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

### **Typical Performance Characteristics** (Continued)



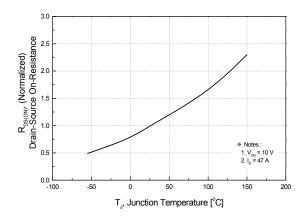


Figure 7. Breakdown Voltage Variation vs. Temperature

Figure 8. On-Resistance Variation vs. Temperature

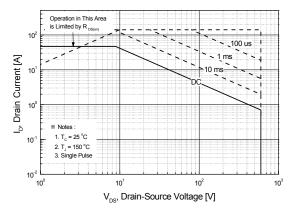


Figure 9. Safe Operating Area

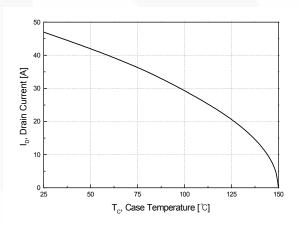


Figure 10. Maximum Drain Current vs. Case Temperature

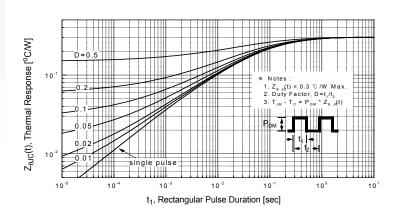


Figure 11. Transient Thermal Response Curve

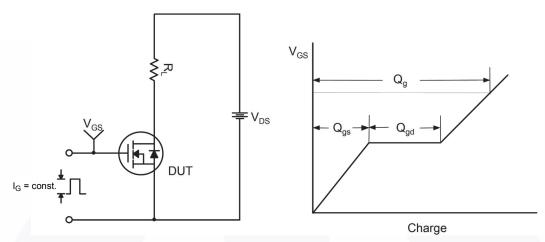


Figure 13. Gate Charge Test Circuit & Waveform

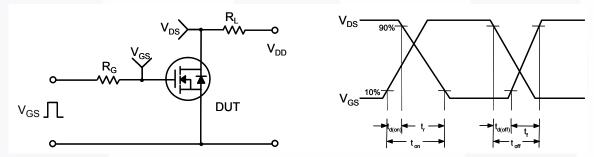


Figure 14. Resistive Switching Test Circuit & Waveforms

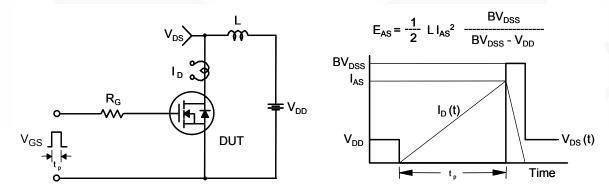


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

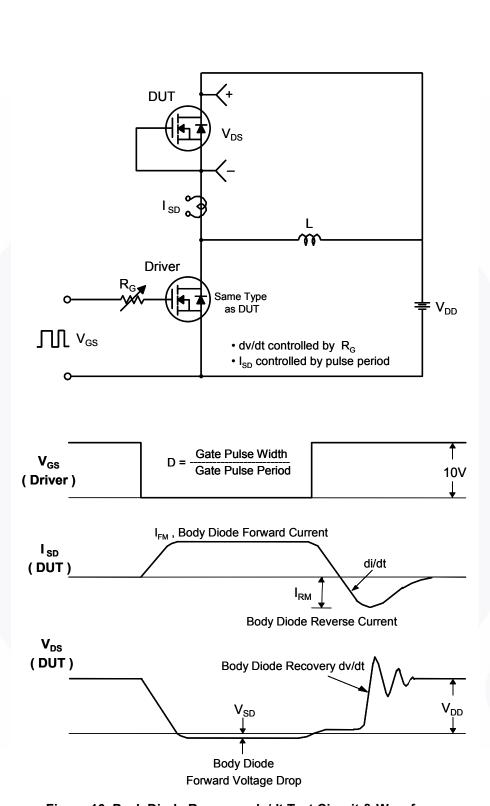
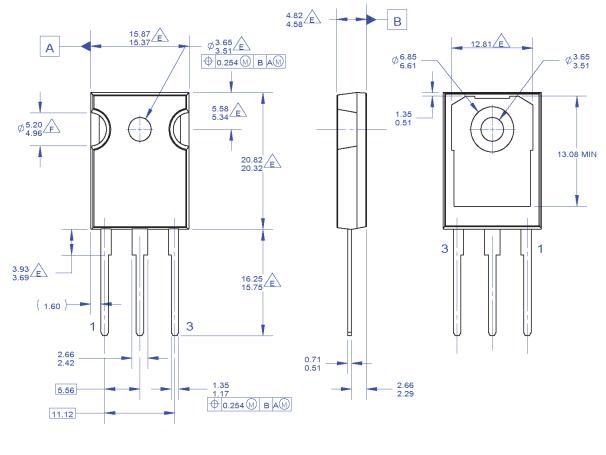


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

#### **Mechanical Dimensions**



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Figure 17. TO-247, Molded, 3-Lead, Jedec Variation AB

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