

1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT223 (SC-73) surface-mountable plastic package intended for applications requiring direct interfacing to logic level ICs and low power gate drivers.

2. Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Surface-mountable package
- Triggering in all four quadrants
- Very sensitive gate in four quadrants

3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

4. Quick reference data

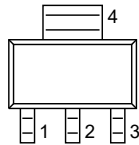
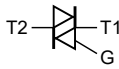
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| V_{DRM} | repetitive peak off-state voltage | | - | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq 105\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | - | 1 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | - | 8 | A |
| | | full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$ | - | - | 8.5 | A |
| T_j | junction temperature | | - | - | 125 | °C |
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 9 | - | - | 3 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 9 | - | - | 3 | mA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------------------|
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | - | 3 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | - | 5 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10 | - | - | 7 | mA |
| V_T | on-state voltage | $I_T = 1.4\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11 | - | 1.3 | 1.6 | V |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 402\text{ V}$; $T_j = 110\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 13 | 10 | - | - | V/ μs |
| dV_{com}/dt | rate of change of commutating voltage | $V_D = 400\text{ V}$; $T_j = 110\text{ }^\circ\text{C}$; $dI_{com}/dt = 0.44\text{ A/ms}$; gate open circuit | 0.5 | - | - | V/ μs |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------|-----------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|
| 1 | T1 | main terminal 1 |  <p>SC-73 (SOT223)</p> |  <p>sym051</p> |
| 2 | T2 | main terminal 2 | | |
| 3 | G | gate | | |
| 4 | T2 | main terminal 2 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|------------------------------------------------------------------|---------|
| | Name | Description | Version |
| Z0103MN | SC-73 | plastic surface-mounted package with increased heatsink; 4 leads | SOT223 |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------|-----|------|------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq 105\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | 1 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | 8 | A |
| | | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$ | - | 8.5 | A |
| I^2t | I^2t for fusing | $t_p = 10\text{ ms}$; SIN | - | 0.32 | A ² s |
| di_T/dt | rate of rise of on-state current | $I_G = 20\text{ mA}$; T2+ G+ | - | 50 | A/ μ s |
| | | $I_G = 20\text{ mA}$; T2+ G- | - | 50 | A/ μ s |
| | | $I_G = 20\text{ mA}$; T2- G- | - | 50 | A/ μ s |
| | | $I_G = 20\text{ mA}$; T2- G+ | - | 20 | A/ μ s |
| I_{GM} | peak gate current | | - | 1 | A |
| P_{GM} | peak gate power | | - | 2 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | - | 0.1 | W |
| T_{stg} | storage temperature | | -40 | 150 | °C |
| T_j | junction temperature | | - | 125 | °C |



Fig. 1. RMS on-state current as a function of surge duration; maximum values



Fig. 2. RMS on-state current as a function of solder point temperature; maximum values



Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

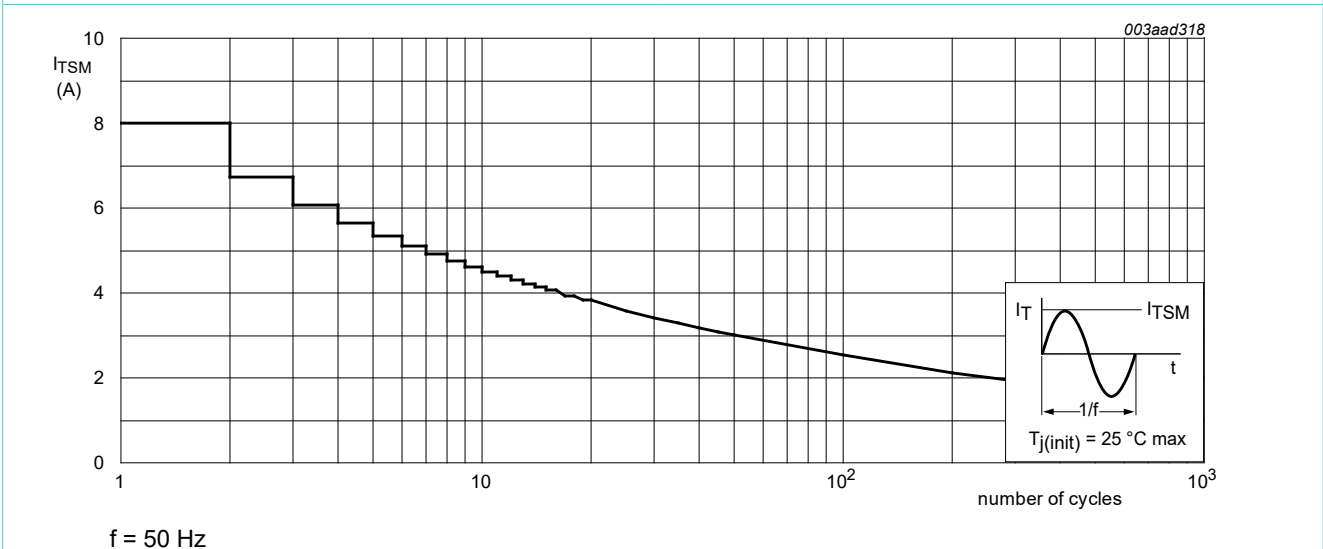
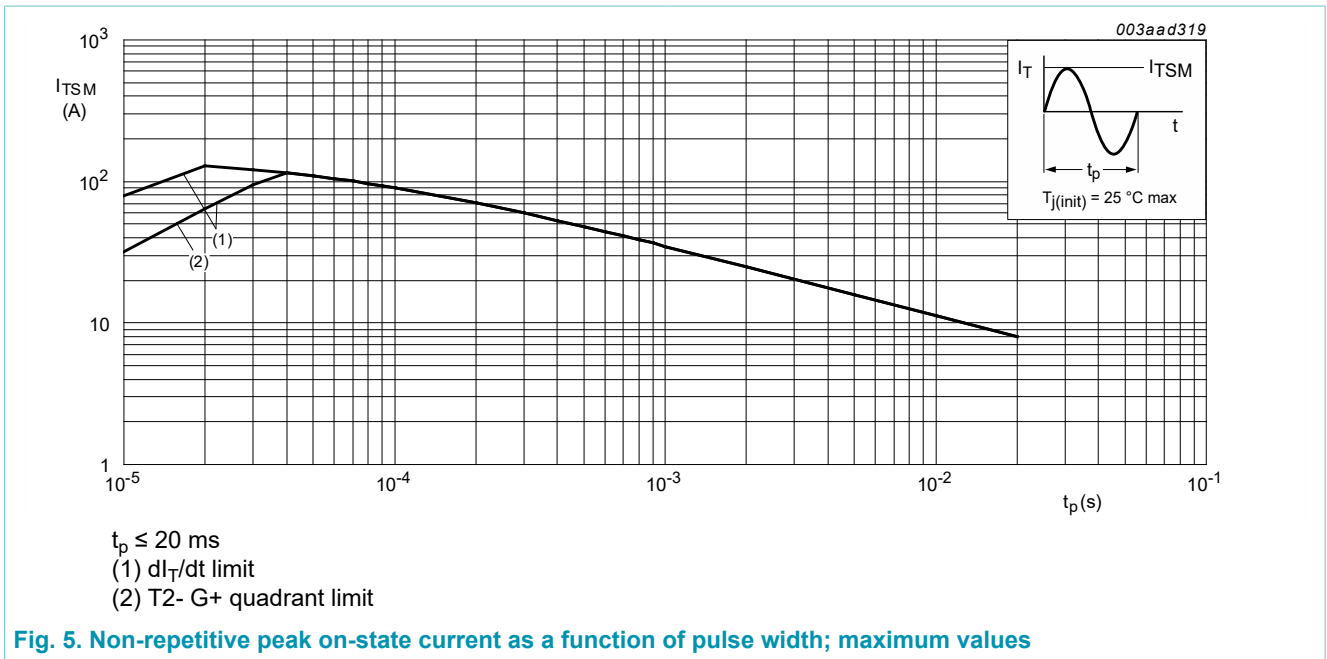


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|------------------------------------------------------|--------------------------------------------------------------------------------------|-----|-----|-----|------|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | full cycle; Fig. 6 | - | - | 15 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | full cycle; printed circuit board mounted; minimum footprint; Fig. 7 | - | 156 | - | K/W |
| | | full cycle; printed circuit board mounted; pad area; Fig. 8 | - | 70 | - | K/W |

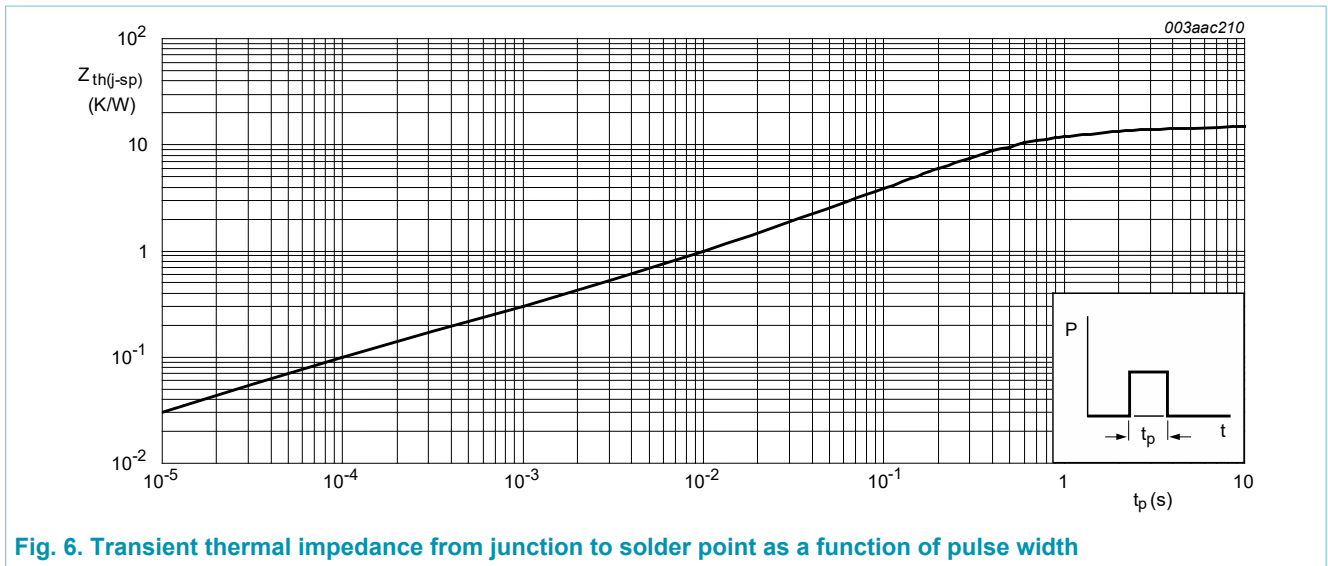


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width



All dimensions are in mm

Fig. 7. Minimum footprint SOT223



All dimensions are in mm

Printed circuit board:

FR4 epoxy glass (1.6 mm thick), copper laminate (35 um thick)

Fig. 8. Printed circuit board pad area: SOT223

9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------------|
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 9 | - | - | 3 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 9 | - | - | 3 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 9 | - | - | 3 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 9 | - | - | 5 | mA |
| I_L | latching current | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 10 | - | - | 7 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 10 | - | - | 15 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 10 | - | - | 7 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 10 | - | - | 7 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 10 | - | - | 7 | mA |
| V_T | on-state voltage | $I_T = 1.4\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11 | - | 1.3 | 1.6 | V |
| V_{GT} | gate trigger voltage | $V_D = 600\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ °C}$ | 0.2 | - | - | V |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12 | - | - | 1 | V |
| I_D | off-state current | $V_D = 600\text{ V}$; $T_j = 125\text{ °C}$ | - | - | 0.5 | mA |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 402\text{ V}$; $T_j = 110\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 13 | 10 | - | - | V/ μ s |
| dV_{com}/dt | rate of change of commutating voltage | $V_D = 400\text{ V}$; $T_j = 110\text{ °C}$; $dI_{com}/dt = 0.44\text{ A/ms}$; gate open circuit | 0.5 | - | - | V/ μ s |



Fig. 9. Normalized gate trigger current as a function of junction temperature

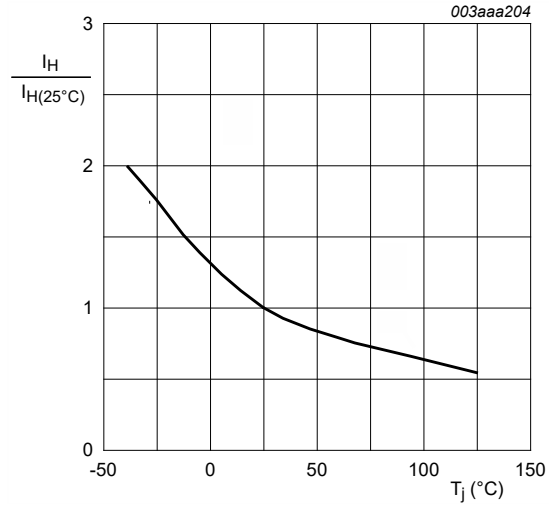


Fig. 10. Normalized holding current as a function of junction temperature

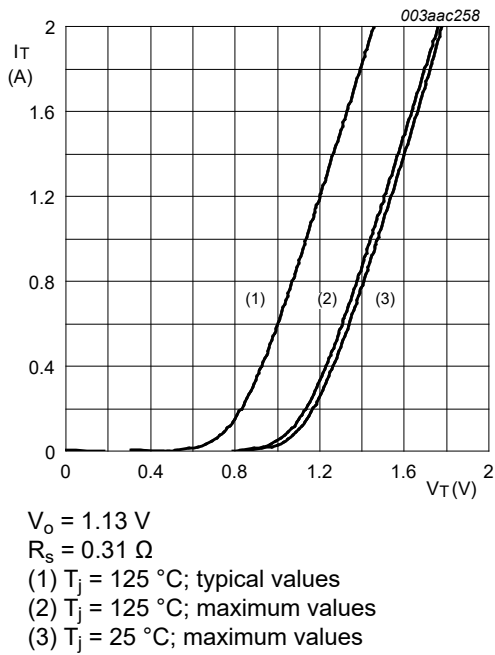


Fig. 11. On-state current as a function of on-state voltage

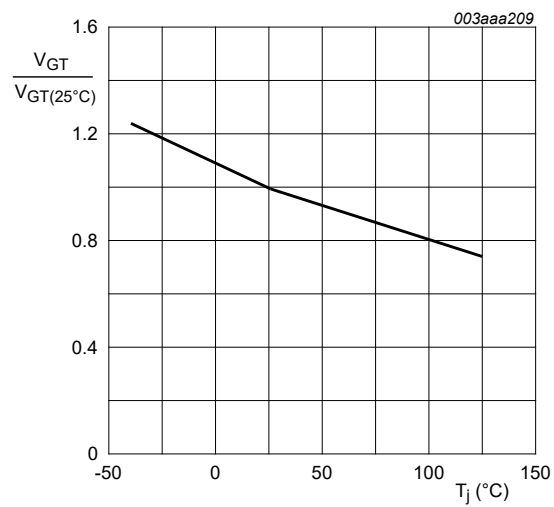
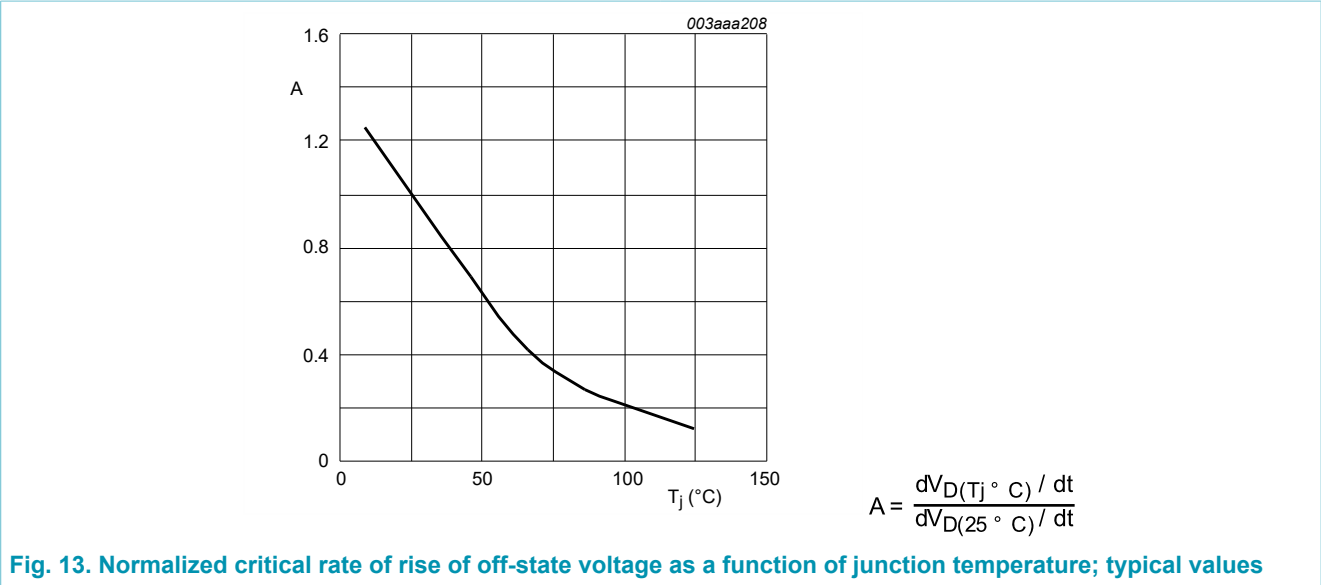


Fig. 12. Normalized gate trigger voltage as a function of junction temperature



10. Package outline



Fig. 14. Package outline SC-73 (SOT223)

11. Legal information

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