Si3068

FCC+ Embedded Direct Access Arrangement

Features

- 80 dB dynamic range TX/RX paths to support up to V.92 modem speeds
- Compliant with 49 PTTs, including FCC, JATE, China, and Korea
- Integrated analog front end (AFE) and 2- to 4-wire hybrid
- Integrated ring detector
- Pulse dialing support
- Patented >6000 V isolation technology
- Proprietary isolation capacitor interface to integrated DAA module
- Line voltage monitor
- Loop current monitor
- Caller ID support
- Lead-free and RoHS-compliant 8-pin ESOIC package

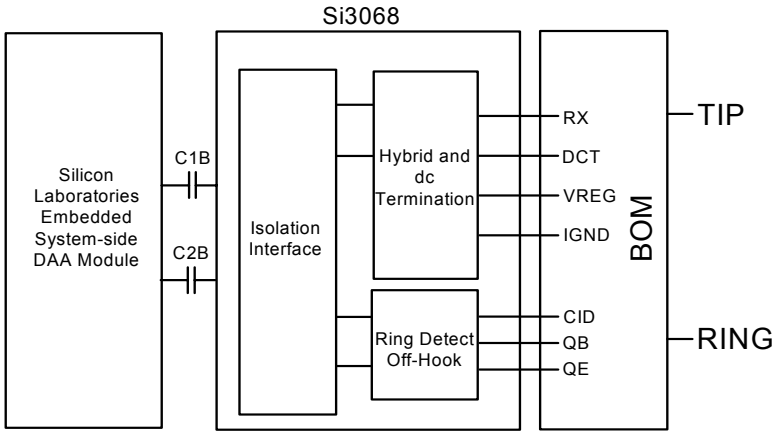
Applications

- V.92 modems
- Digital televisions
- PDAs
- Set-top boxes
- Fax machines
- ePOS terminals
- Internet appliances
- Multi-function printers

Description

The Si3068 is an integrated direct access arrangement (DAA) for use with an integrated DAA system-side module. It includes a V.92 quality codec, dc termination, ac termination, and an integrated hybrid, eliminating the need for an analog front end (AFE), isolation transformer, relays, optoisolator, and a 2- to 4-wire hybrid. It interfaces directly to the integrated system-side module and features Silicon Laboratories' patented isolation technology. The Si3068 dramatically reduces the board space, component count, and cost required to implement a DAA compliant with the regulatory requirements of 49 different PTTs including FCC, JATE, China, and Korea.

Functional Block Diagram

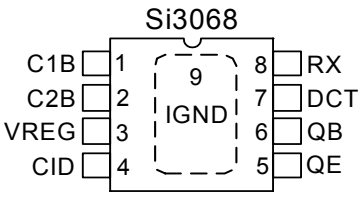


Ordering Information

See page 36.

Pin Assignments

Si3068



US Patent # 5,870,046
US Patent # 6,061,009
Other Patents Pending

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter*	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A	F-Grade	0	25	70	°C

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.

Table 2. DAA Loop Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C, see Figure 1)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 120 mA	9	—	—	V
On-Hook Leakage Current	I_{LK}	V_{TR} = –100 V	—	—	12	µA
Operating Loop Current	I_{LP}		15	—	120	mA
DC Ring Current		dc current flowing through ring detection circuitry	—	1.5	3	µA
Ring Detect Voltage*	V_{RD}		10	15	35	V_{rms}
Ring Frequency	F_R		15	—	68	Hz
Ringer Equivalence Number	REN		—	—	0.2	

***Note:** The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.

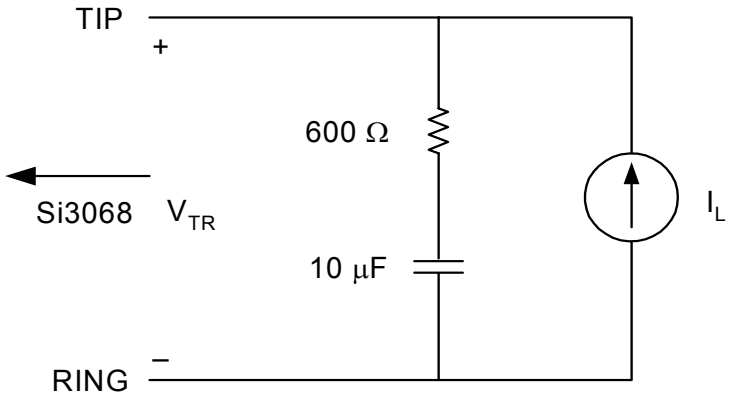


Figure 1. Test Circuit for Loop Characteristics

Table 3. DAA AC Characteristics
(T_A = 0 to 70 °C, Fs = 8 kHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate	Fs		7.2	—	16	kHz
Receive Frequency Response		Low –3 dBFS Corner	—	5	—	Hz
Transmit Full Scale Level[1]	V_{FS}	–1 dBm	—	0.98	—	V_{PEAK}
Receive Full Scale Level[1,2]	V_{FS}	–1 dBm	—	0.98	—	V_{PEAK}
Dynamic Range[3,4,5]	DR	I_L = 100 mA	—	80	—	dB
Dynamic Range[3,4,5]	DR	I_L = 20 mA	—	80	—	dB
Transmit Total Harmonic Distortion[5,6]	THD	I_L = 20 mA	—	75	—	dB
Receive Total Harmonic Distortion[5,6]	THD	I_L = 20 mA	—	–78	—	dB
Dynamic Range (caller ID mode)[7]	DR_{CID}	V_{IN} = 1 kHz, –13 dBm	—	50	—	dB
Caller ID Full Scale Level	V_{CID}		—	6	—	V_{PP}

Notes:
1. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1.
2. Receive full scale level produces –0.9 dBFS.
3. DR = 20 x log (rms V_{FS}/rms V_{IN})+ 20 x log (rms V_{IN}/rms noise, excluding harmonics). V_{FS} is the –1 dBm full-scale level.
4. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths.
5. V_{IN} = 1 kHz, –3 dBFS
6. THD = 20 x log (rms distortion / rms signal).
7. DR_{CID} = 20 x log (rms V_{CID}/rms V_{IN})+ 20 x log (rms V_{IN}/rms noise). V_{CID} is the 6 V full-scale level.

Table 4. Digital FIR Filter Characteristics—Transmit and Receive
(Sample Rate = 8 kHz, T_A = 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (0.1 dB)	$F_{(0.1\ dB)}$	0	—	3.3	kHz
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.1	—	0.1	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–74	—	—	dB
Group Delay	t_{gd}	—	12/Fs	—	s
Note: Typical FIR filter characteristics for Fs = 8000 Hz are shown in Figures 2, 3, 4, and 5.					

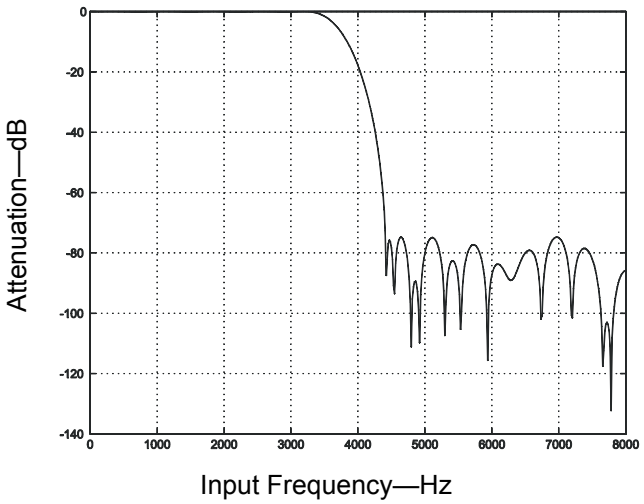


Figure 2. FIR Receive Filter Response

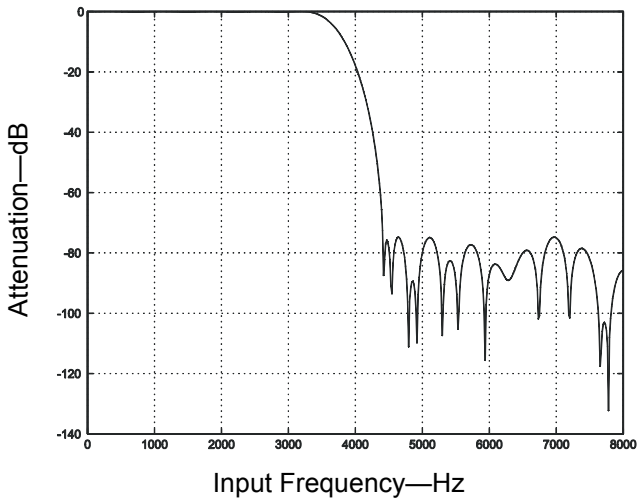


Figure 4. FIR Transmit Filter Response

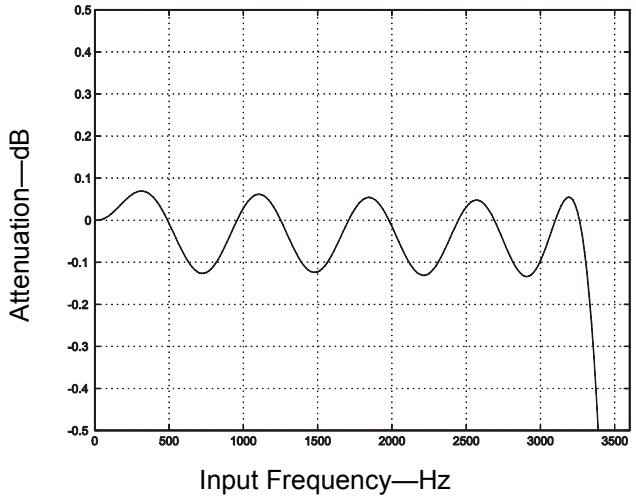


Figure 3. FIR Receive Filter Passband Ripple

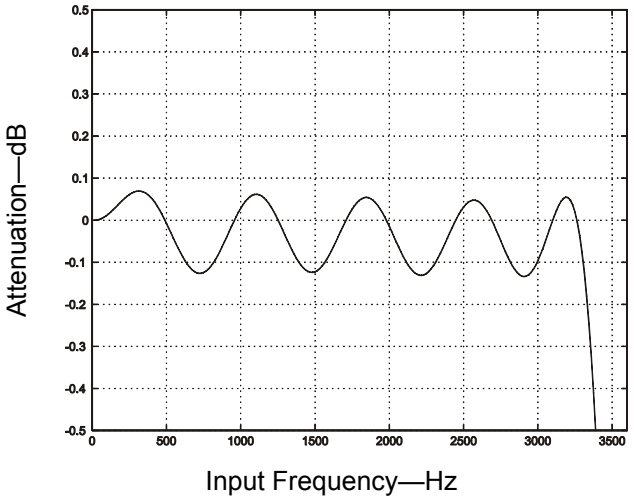


Figure 5. FIR Transmit Filter Passband Ripple

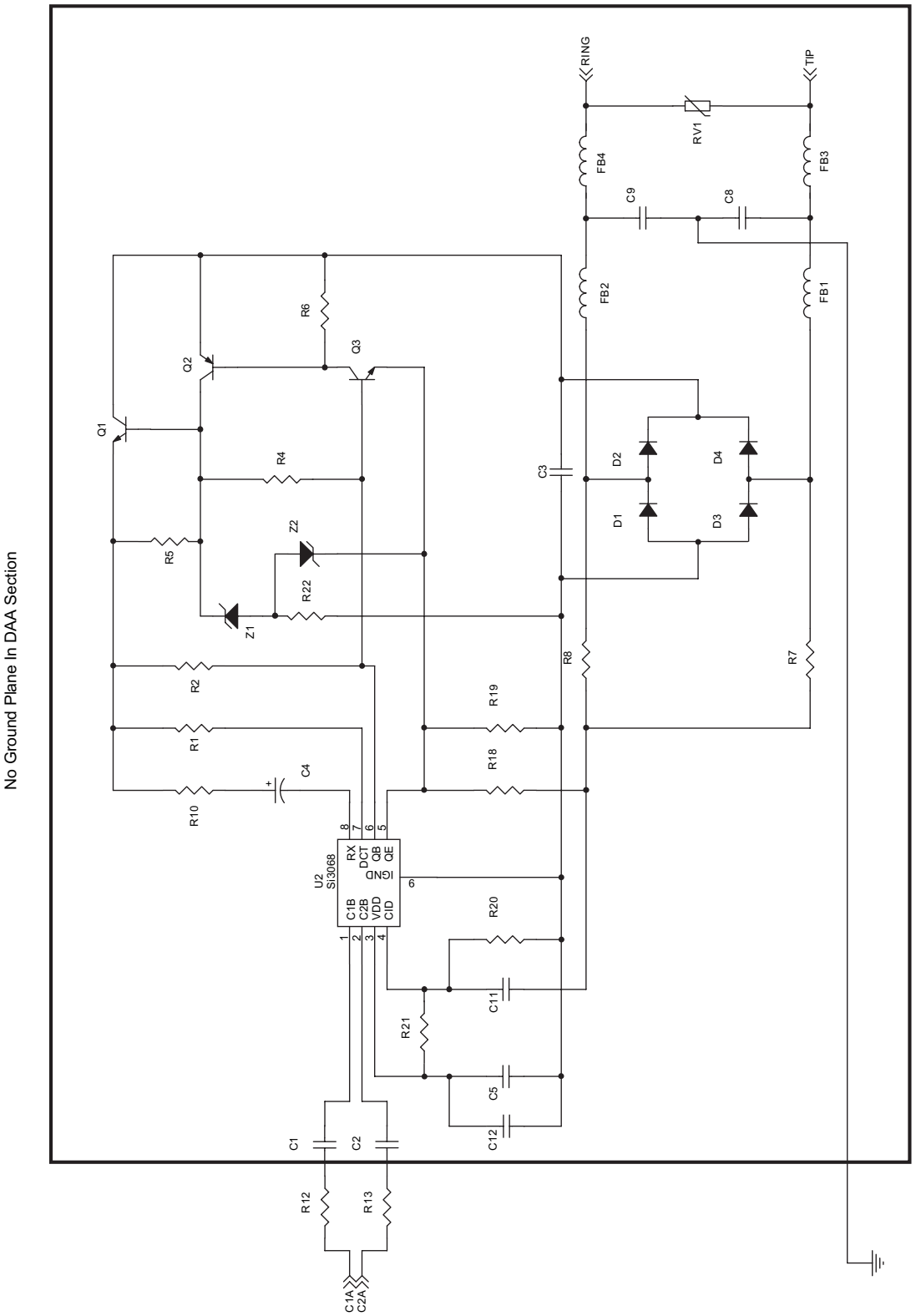
For Figures 2–5, all filter plots apply to a sample rate of Fs = 8 kHz. The filters scale with the sample rate as follows:

$F_{(0.1\ dB)}$ = 0.4125 Fs

$F_{(-3\ dB)}$ = 0.45 Fs

where Fs is the sample frequency.

2. Typical Application Schematic



3. Bill of Materials

Component	Value	Supplier(s)
C1, C2	33 pF, Y2, X7R, ±10%	Panasonic, Murata, Vishay
C3	10 nF, 250 V, X7R, ±20%	Venkel, SMEC
C4	1.0 µF, 35 V, Elec, ±20%	Panasonic
C5	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC
C8, C9	680 pF, Y2, X7R, ±10%	Panasonic, Murata, Vishay
C11	220 pF, 50 V, X7R, ±10%	Venkel, SMEC
C12	DNP 0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC
D1, D2, D3, D4[1]	Diode, 400 V, 1N4004	Central Semiconductor
FB1, FB2, FB3, FB4[2]	Ferrite Bead, BLM18AG601SN1B	Murata
Q1, Q3	NPN, 300 V, MPSA42	OnSemi, Fairchild
Q2	PNP, 300 V, MPSA92	OnSemi, Fairchild
RV1	Sidactor, 275 V, 100A	Teccor, Protek, ST Micro
R1[3]	205 Ω, 1 W, 1%	Venkel, SMEC, Panasonic
R2[4]	243 Ω, 1 W, 1%	Venkel, SMEC, Panasonic
R4	3.9 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R5, R6	100 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R7, R8	10 MΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R10	1 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R12, R13	56 Ω, 1/16 W, 1%	Venkel, SMEC, Panasonic
R22	DNP 0 Ω, 1/16 W, 5%	Venkel, SMEC, Panasonic
R18	1.5 MΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R19	180 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R20, R21	3 MΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
U2	Si3068	Silicon Laboratories
Z1, Z2	Zener Diode, 20 V, 1/2 W	General Semiconductor

Notes:

1. Several diode bridge configurations are acceptable, parts such as a single DF-04S or two CMPD2004S dual diodes may be used (suppliers include General Semiconductor, Diodes Inc., etc.)
2. 0 Ω may be substituted for FB3, FB4 depending on emissions performance.
3. Three 619 Ω 1/4 W 1% in parallel configuration may be substituted for R1.
4. Three 732 Ω 1/4 W 1% in parallel configuration may be substituted for R2.

4. Telephone Line Interface Functional Description

Together, the integrated system-side and Si3068 comprise an integrated direct access arrangement (DAA) that provides a programmable line interface to meet the telephone line interface requirements of countries worldwide. The device implements Silicon Laboratories' patented isolation technology, which offers the highest level of integration by replacing an analog front end (AFE), an isolation transformer, relays, opto-isolators, a 2- to 4-wire hybrid, and other circuitry.

The Si3068 can be fully programmed to meet international requirements and is compliant with FCC, JATE, and numerous other country-specific PTT specifications as shown in Table 5. Also, the Si3068 meets the most stringent requirements for out-of-band energy, emissions, immunity, lightning surges, and safety.

4.1. Initialization

The following is an example initialization procedure:

1. Select the desired sample rate using the SRC bits (Register 7, bits 3:0).
2. Power up the line side by clearing the PDL bit (Register 6, bit 4).
3. Enable AOUT (if applicable) by setting ARM[7:0] (Register 20, bits 7:0) and ATM[7:0] (Register 21, bits 7:0) to the desired level.
4. Prior to receiving or transmitting data, ensure FDT (Register 12) is set indicating the Si3068 is ready for normal operation.

After the procedure is complete, the DAA is ready for off-hook, on-hook line monitoring, and ring detection.

4.2. Isolation Barrier

The Si3068 achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with Silicon Laboratories' proprietary signal processing techniques. These techniques eliminate signal degradation from capacitor mismatches, common mode interference, or noise coupling. The C1, C2, C8, and C9 capacitors isolate the system-side device from the Si3068 line-side device. All transmit, receive, control, ring detect, and caller ID data are communicated through this barrier. Y2 class capacitors can be used to achieve surge performance of 6 kV or greater.

The isolated communications link is disabled by default. To enable it, the PDL bit (Register 6, bit 4) must be cleared. No communication between the system-side and Si3068 can occur until this bit is cleared and the FDT bit (Register 12, bit 6) is high.

4.3. Parallel Handset Detection

The Si3068 can detect a parallel handset going off-hook. When the DAA is off-hook, the loop current can be monitored via the LCS bits (Register 12, bits 4:0). A significant drop in loop current can signal a parallel handset going off-hook. If a parallel handset causes the LCS bits to read 0s, the DropOut Detect Interrupt bit (Register 4, bit 3) can be checked to verify that a valid line still exists.

For the Si3068 to operate in parallel with another handset, the parallel handset must have a sufficiently high dc termination impedance to support two DAAs off hook on the same line.

Table 5. Country-Specific PTT Specifications

Country	
Argentina	Kyrgyzstan
Armenia	Macao
Bahamas	Mexico
Bangladesh	Moldova
Belarus	New Zealand[2]
Bermuda	Paraguay
Brazil	Peru
Brunei	Puerto Rico
Canada	Russia
Caribbean	Saudi Arabia
Chile	Singapore
China	South Korea[3]
Colombia	Sri Lanka
Costa Rica	Taiwan
Dominican Republic	Thailand
Ecuador	Tunisia
El Salvador	UAE
Georgia	Ukraine
Guam	Uruguay
Hong Kong	Uzbekistan
India	USA
Indonesia	Venezuela
Japan[1]	Vietnam
Kazakhstan	Yemen
Kuwait	

Notes:

1. DCR exceeds 300 Ω; disclaimer required in product documentation.
2. 600 Ω ac termination used; disclaimer required in product documentation.
3. Additional components required to pass ringer impedance specifications.

4.4. Loop Current Sensing

The Si3068 measures loop current when off-hook. The LCS[4:0] bits measure loop current with 3.3 mA/bit resolution. The following functions can be performed with the LCS bits:

- While off-hook, detect if a parallel phone goes on- or off-hook.
- Determine if sufficient loop current is available for proper operation.
- Detect if there is an overload condition.

4.4.1. Loop Current Measurement

When the DAA is off-hook, the LCS[4:0] bits measure loop current with 3.3 mA/bit resolution. These bits can be used to detect another device going off-hook by monitoring the dc loop current. The transfer function for LCS is shown in Figure 6 and is detailed in Table 6. The LCS bits report loop current down to the minimum operating loop current for the DAA. Below this threshold, the reported value of loop current is unpredictable and may vary between zero and the minimum operating current.

When the LCS bits have reached their maximum value, the Loop Current Sense Overload Interrupt bit fires; however, LCSOI firing does not necessarily guarantee that an overload situation has occurred.

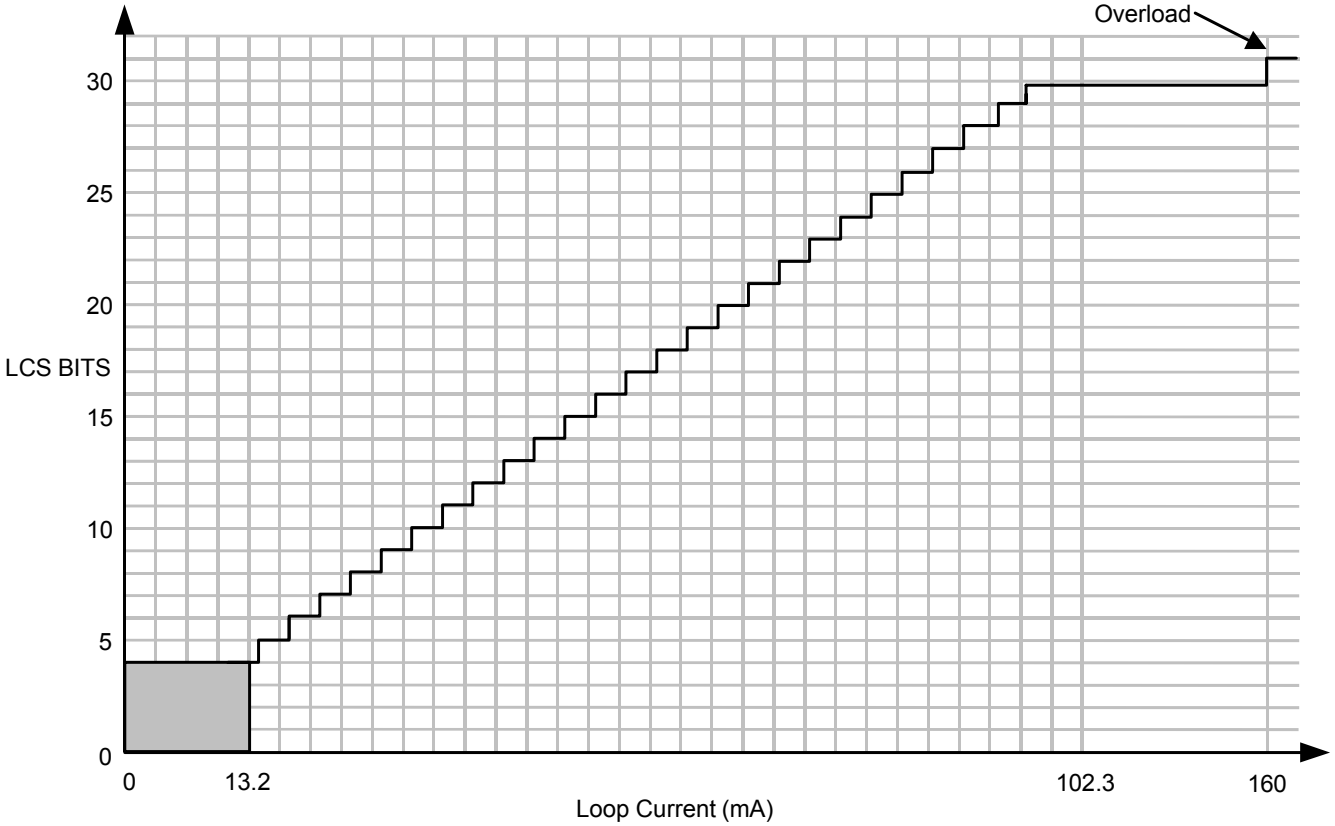


Figure 6. Typical LCS Transfer Function

Table 6. Loop Current Sense Transfer Function

LCS[4:0]	Condition
00000_b – 00011_b	Insufficient line current for normal operation. Use the DODI bit (Register 4, bit 3) to determine if a line is still connected.
00100_b – 11110_b	Normal operation.
11111_b	Loop current is excessive (>160 mA).

4.5. Line Voltage Sensing

The Si3068 measures line voltage when on-hook. The LVS[6:0] bits (register 29) report line voltage with 1 V/bit resolution (typical). The LVS bits can be used to determine if a line is present and, if so, if it is idle or in use. Since these operations can be performed while on-hook, there is no need to enter the off-hook state and possibly disturb a call in progress to determine the status of the line. The typical LVS transfer function is shown in Figure 7 and detailed in Table 7.

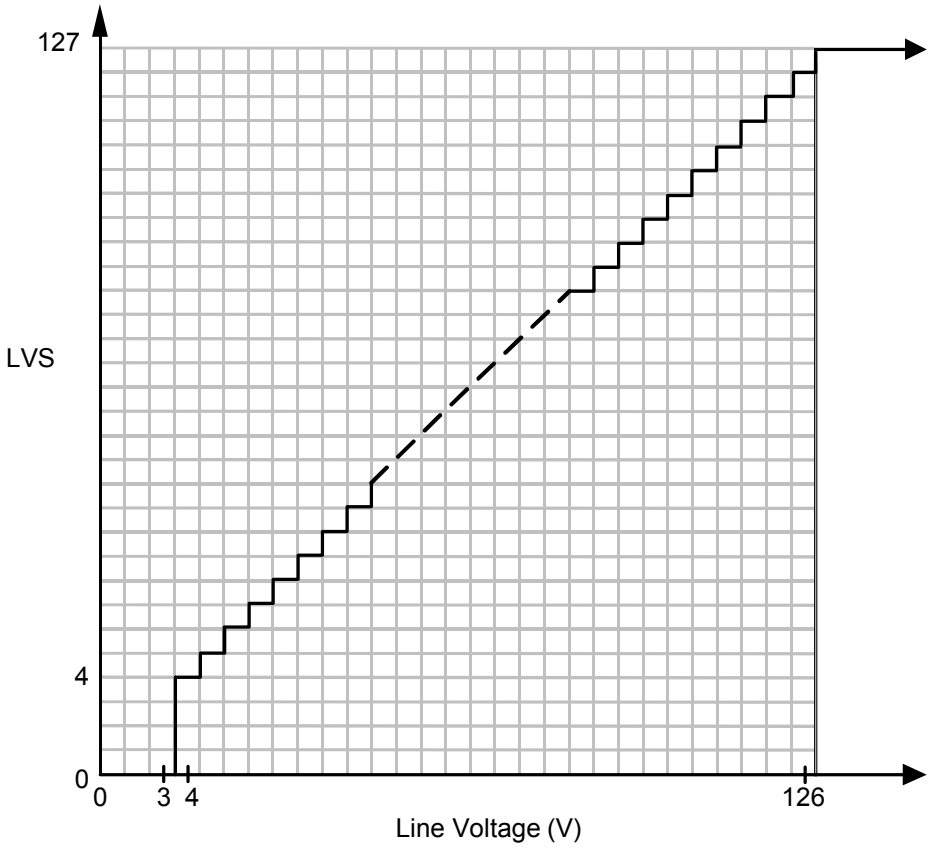


Figure 7. Line Voltage Status Transfer Function

Table 7. Line Voltage Status Transfer Function

LVS[6:0]	Line Voltage
0000000_b	V_{LINE} < 3.5 V
0000100_b – 1111110_b	3.5 V ≤ V_{LINE} < 126.5 V
1111111_b	V_{LINE} ≥ 126.5 V

4.6. Off-Hook

The software generates an off-hook command by setting the OH bit (Register 5, bit 0). This seizes the line for incoming/outgoing calls and can also be used for pulse dialing. When on-hook, negligible dc current flows through the hookswitch. When off-hook, the hookswitch transistor pair, Q1 and Q2, turn on. A termination impedance is applied across TIP and RING and causes dc loop current to flow.

Several events occur internally to the DAA when the OH bit is set. There is a 250 µs latency for the off-hook command to communicate to the line-side device. When the line-side device goes off-hook, an off-hook counter forces a delay before transmission or reception can occur. After this, an ADC calibration is performed for 256 ms. The ADC calibration can be disabled by setting the ADCC bit (Register 17, bit 5). Refer to Section "4.20. Calibration" on page 16 for more information on automatic calibration. To calculate the total time required to go off-hook and start transmission or reception, the digital filter delay (typically 1.5 ms with the FIR filter) should be included in the calculation.

4.7. DC Termination

The Si3068 dc I/V characteristics, shown in Figure 8, support a transmit full scale level of –1 dBm at TIP and RING. This meets FCC requirements and the requirements of many other countries.

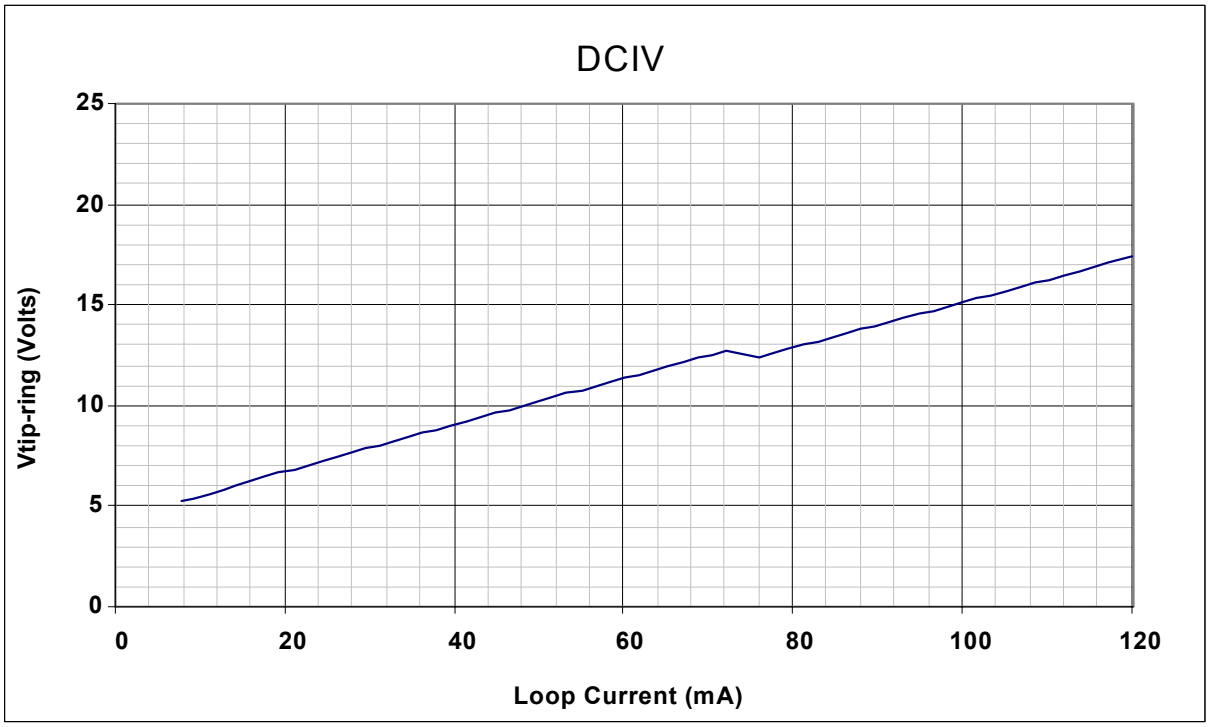


Figure 8. DC I/V Characteristics

4.8. Transhybrid Balance

The Si3068 contains an on-chip analog hybrid that performs the 2- to 4-wire conversion and near-end echo cancellation.

4.9. Ring Detection

Ring detection can be performed by monitoring the ring detector output or by observing the audio CODEC data. The ring detector output can be monitored with the register bits, RDTN, RDTP, and RDT (Register 5, bits 6, 5, and 2). Software must detect the frequency of the ring signal to distinguish a ring from pulse dialing by telephone equipment connected in parallel.

Alternatively, hardware ring validation can be used. See Section "4.10. Ring Validation".

The ring detector output is controlled by the RFWE bit (Register 18, bit 1). When the RFWE bit is 0 (default mode), only positive ring signals are reported by the ring detector. A positive ring signal is defined as a voltage greater than the ring threshold at the QE pin. Conversely, a negative ring signal is defined as a voltage less than the negative ring threshold. When the RFWE bit is 1, the ring detector reports both positive and negative ring signals.

The RDTP and RDTN behavior is based on the ring voltage. When the signal is above the positive ring threshold, the RDTP bit is set. When the signal is below the negative ring threshold, the RDTN bit is set. When the signal is between these thresholds, neither bit is set. The RDT behavior is also based on the ring voltage. When the RFWE bit is 0, a positive ring signal sets the RDT bit for a period of time. When the RFWE bit is 1, either a positive or negative ring signal sets the RDT bit.

The audio CODEC data also signals ring events when on-hook. If the RFWE bit is 0, the CODEC output is fixed at –32768 when a ring is not present. The CODEC data becomes +32767 upon detection of a positive ring. Negative rings will be ignored and have no effect on the CODEC data while RFWE is 0.

When on-hook with RFWE = 1, the CODEC data is fixed at +1228 when a ring is not present. The CODEC data becomes +32767 upon detection of a positive ring or –32768 upon detection of a negative ring.

The RDT bit acts like a one shot. When a new ring signal is detected, the one shot is reset. If no new ring signals are detected before the one shot counter reaches 0 (5 seconds), the RDT bit returns to 0. The RDT bit is also reset to 0 by an off-hook event.

4.10. Ring Validation

This feature prevents false ring detection by validating the ring parameters. Invalid signals, such as line-voltage changes when a parallel handset goes off-hook, pulse dialing, polarity reversals, and high-voltage line tests, are ignored. Ring validation can be enabled during normal operation and in low-power sleep mode.

The ring validation circuit operates by calculating the time between alternating crossings of positive and negative ring thresholds to validate that the ring frequency is within tolerance. High- and low-frequency tolerances are programmable in the RAS[5:0] and RMX[5:0] fields. The RCC[2:0] bits define the length of time the ring signal must be within tolerance. Once the duration of the ring frequency is validated by the RCC bits, the circuitry stops checking for frequency tolerance and begins checking for the end of the ring signal, which is defined by a lack of additional threshold crossings for a period of time configured by the RTO[3:0] bits. When the ring frequency is first validated, a timer defined by the RDLY[2:0] bits is started. If the RDLY[2:0] timer expires before the ring timeout, the ring is validated, and a valid ring is indicated. If the ring timeout expires before the RDLY[2:0] timer, a valid ring is not indicated.

Ring validation requires five parameters:

- Timeout parameter to place a lower limit on the frequency of the ring signal on the RAS[5:0] bits (Register 24, bits 5:0). The frequency is measured by calculating the time between crossings of positive and negative ring thresholds.
- Minimum count to place an upper limit on the frequency on the RMX[5:0] bits (Register 22, bits [5:0]).
- Time interval over which the ring signal must be the correct frequency on the RCC[2:0] bits (Register 23, bits [2:0]).
- Timeout period that defines when the ring pulse has ended with the most recent ring threshold crossing on the RTO [3:0] bits (Register 23, bits 6:3).
- Delay period between when the ring signal is validated and when a valid ring signal is indicated to help accommodate distinctive ring on the RDLY [2] bit (Register 23, bit 7).

The ring validation enable bit, RNGV (Register 24, bit 7), enables or disables the ring validation feature in normal operating mode and low-power sleep mode. For further details, see “AN72: Ring Detection/Validation with the Si305x DAAs.”

4.11. Ringer Impedance and Threshold

The ring detector in many DAAs is ac-coupled to the line with a large 1 µF, 250 V decoupling capacitor. The ring detector on the Si3068 is resistively coupled to the line. The network presents a high ringer impedance to the line of approximately 5 MΩ to meet the majority of PTT specifications, including FCC. The ringer impedance network shown in Figure 9 is required for compliance with the ringer impedance requirements of South Korea. This network is only required if the application will be deployed in South Korea. The network components are detailed in Table 8.

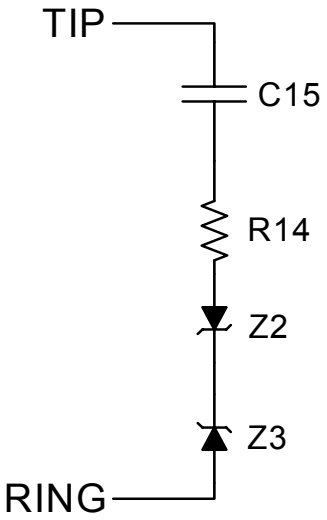


Figure 9. South Korea Ringer Impedance Network

Table 8. South Korea Ringer Impedance Network Components

Item	Value
C15	1 mF, 250 V
R14	7.5 kΩ, 1/4 W
Z2	18 V
Z3	18 V

4.12. DTMF Dialing

The Si3068 meets all the country requirements for DTMF dialing listed in Table 5 on page 10. Higher DTMF levels can be achieved if the amplitude is increased and the peaks of the DTMF signal are clipped at digital full scale, avoiding wrapping the waveform.

Clipping the signal produces distortion and intermodulation of the signal. Generally, increased distortion between 10 and 20% is acceptable during DTMF signaling. DTMF levels several dB higher can be achieved with this technique, compared with a digital full-scale peak signal.

4.13. Pulse Dialing

Going off- and on-hook to generate make and break pulses accomplishes pulse dialing. The nominal rate is 10 pulses per second.

4.14. Receive Overload

Certain line events, such as an off-hook event on a parallel phone, a billing tone, or a polarity reversal, can cause a receiver overload. Although the DAA may remain off-hook during such an event, the data received from the line may be corrupted.

If a disturbance on the line causes the loop current to collapse below the minimum operating current, the dropout detect bit, DOD, is set. An interrupt will be generated if the dropout detect interrupt mask bit, DODM, is set.

4.15. On-Hook Line Monitor Mode

The DAA monitors line activity when in on-hook line-monitor mode. This mode detects caller ID data, and no line current is drawn. See Section “4.16. Caller ID” on page 15. This mode is enabled by setting the ONHM bit (Register 5, bit 3). ARX [2:0] (Register 15, bits 2:0) provides gain to the normal receive path of the DAA and functions as a gain bit for the on-hook line monitor.

4.16. Caller ID

The DAA can pass caller ID data from the phone line to a software caller ID decoder.

4.16.1. Type I Caller ID

Type I Caller ID sends the CID data while the phone is on-hook. In systems where the caller ID data is passed on the phone line between the first and second rings, utilize the following method to capture the caller ID data:

1. After identifying a ring signal using one of the methods described in Section "4.9. Ring Detection" on page 14, determine when the first ring has completed.
2. Assert the ONHM bit (Register 5, bit 3) to enable the caller ID ADC. This low-current ADC, which is powered from the system-side device, digitizes the caller ID data.
3. Clear the ONHM bit after the caller ID data is received.

4.16.2. Type II Caller ID

Type II Caller ID sends the CID data while the phone is off-hook and is often referred to as caller ID/call waiting (CID/CW). To receive the CID data while off-hook, use the following procedure:

1. The Caller Alert Signal (CAS) tone is sent from the Central Office (CO) and is digitized along with the line data. The software must detect the presence of this tone.
2. Since the DAA is the only device on the line and is Type II CID-compliant, the software must mute its upstream data output to avoid propagation of its reply tone and the subsequent CID data. After muting its upstream data output, the software must then return an acknowledgement (ACK) tone to the CO to request the transmission of the CID data.
3. The CO then responds with the CID data, and the software unmutes the upstream data output and continues with normal operation.
4. The muting of the upstream data path by the software mutes the handset in a telephone application so the user cannot hear the acknowledgement tone and CID data being sent.

The CID data presented to the software could have up to a 10% dc offset. The software caller ID decoder must either use a high-pass or a band-pass filter to accurately retrieve the caller ID data.

4.17. Gain Control

The Si3068 supports multiple receive gain and transmit attenuation settings (Register 15). The receive path supports gains of 0, 3, 6, 9, and 12 dB, as selected with the ARX[2:0] bits. The receive path can be muted with the RXM bit. The transmit path supports attenuations of 0, 3, 6, 9, and 12 dB, as selected with the ATX[2:0] bits. The transmit path can be muted with the TXM bit.

4.18. Sample Rate Converter

The SRC [3:0] bits (Register 7, bits 3:0) are used to select the sample rate. The following sample rates are supported: 7200, 8000, 8229, 8400, 9000, 9600, 10286, 12000, 13714, and 16000 Hz.

4.19. Power Management

The Si3068 supports four basic power management operation modes: normal operation, reset operation, sleep mode, and full powerdown mode. The power management modes are controlled by the PDL and PDN bits (Register 6, bits [4:3]).

Upon powerup or following a reset, the Si3068 is in reset operation. The PDL bit is set, and the PDN bit is cleared. The system-side module is fully operational except for the isolated capacitor link. No communication between the system side and Si3068 can occur during reset operation. Register bits associated with the Si3068 are not valid in this mode.

The most common mode of operation is normal operation. The PDL and PDN bits are cleared, and the capacitive link is passing information between the system side and the Si3068. A valid sample rate must be programmed before entering this mode.

The Si3068 supports a low-power sleep mode for the wake-up-on-ring feature of many modems. The sample rate must be programmed with a valid non-zero value before enabling sleep mode. The PDN bit must then be set; the PDL bit cleared. To take the DAA out of sleep mode, pulse ($\overline{\text{RESET}}$) low.

In summary, the powerdown sequence for sleep mode is as follows:

1. SRC[3:0] must have a valid non-zero value.
2. Set the PDN bit (Register 6, bit 3) and clear the PDL bit (Register 6, bit 4).

The power-up sequence is as follows:

1. Reset the DAA by pulsing the $\overline{\text{RESET}}$ pin.
2. Program registers to required settings.

The Si3068 also supports an additional powerdown mode. When the PDN and PDL bits are set, the DAA enters a complete powerdown mode and draws negligible current (deep sleep mode). Normal operation is restored using the same process for taking the DAA out of sleep mode.

4.20. Calibration

The Si3068 initiates an auto-calibration by default when the device goes off-hook or experiences a loss in line power. Calibration removes offsets that are present in the on-chip ADC and could affect the ADC dynamic range. Auto-calibration is initiated after the DAA dc termination stabilizes and takes 273 ms to complete.

4.21. Revision Identification

The revision of the system-side module and line-side (Si3068) can be determined using the REVA[3:0] bits (Register 11, bits 3:0) and REVB[3:0] bits (Register 13, bits 5:2), respectively. Table 9 lists the revision values.

Table 9. Si3068 Revision Levels

Si3068 Revision	Si3068 REVB[3:0]
A	1000
B	1001

5. Register Summary

Offset	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Control 1	SR		PWMM[1:0]		PWME		IDL	
2	Control 2				WDTE	AL	RDM	HBE	RXE
3	Interrupt Mask	RDTM		FDTM		DODM	LCSM		
4	Interrupt Status	RDTI		FDTI		DODI	LCSI		
5	DAA Control 1		RDTN	RDTP		ONHM	RDT		OH
6	DAA Control 2				PDL	PDN			
7	Sample Rate Control					SRC[3:0]			
8	Reserved								
9	Reserved								
10	DAA Control 3								DDL
11	System-Side Revision	LSID[3:0]				REVA[3:0]			
12	Line-Side Status		FDT		LCS[4:0]				
13	Line-Side Revision			REVB[3:0]					
14	Reserved								
15	TX/RX Gain Control	TXM	ATX[2:0]			RXM	ARX[2:0]		
16	Reserved								
17	Calibration			ADCC					
18	International Control 3							RFWE	
19	Dropout Detect							DOD	
20	Call Progress RX Attenuation	ARM[7:0]							
21	Call Progress TX Attenuation	ATM[7:0]							
22	Ring Validation Control 1	RDLY[1:0]		RMX[5:0]					
23	Ring Validation Control 2	RDLY[2]	RTO[3:0]				RCC[2:0]		
24	Ring Validation Control 3	RNGV		RAS[5:0]					
25	Reserved								
26	Reserved								
27	Reserved								
28	Reserved								
29	Line Voltage Status		LVS[6:0]						
30–59	Reserved								
60	Line-side ID						LSID4		

DAA Register 1. Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR		PWMM[1:0]		PWME		IDL	
Type	R/W		R/W		R/W		R/W	

Reset settings = 0000_0x0x

Bit	Name	Function
7	SR	**Software Reset.** 0 = Enables DAA for normal operation. 1 = Sets all registers to their reset value. **Note:** Bit clears automatically after being set.
6	Reserved	Always write as zero. Reads undefined.
5:4	PWMM[1:0]	**Pulse-Width Modulation Mode.** Selects the type of signal on the call progress AOUT pin. 00 = PWM output clocked at 16.384 MHz. A local density of 1s and 0s tracks the combined transmit and receive signal. 01 = Balanced conventional PWM output signal has high and low portions of the modulated pulse centered on the 32 kHz sample clock. 10 = Conventionally PWM output signal returns to 0 at 32 kHz intervals and rises at a time in the 32 kHz period proportional to the instantaneous amplitude. 11 = Reserved.
3	PWME	**Pulse-Width Modulation Enable.** 0 = Call progress PWM AOUT disabled. 1 = Call progress PWM AOUT enabled.
2	Reserved	Read returns zero.
1	IDL	**Isolation Digital Loopback.** 0 = Digital loopback across isolation barrier disabled. 1 = Enables digital loopback mode across isolation barrier. The line-side device must be enabled and off-hook before setting this mode. This data path includes RX and TX filters. A valid phone line is not necessary for this mode.
0	Reserved	Read returns zero.

DAA Register 2. Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				WDTE	AL	RDM	HBE	RXE
Type				R/W	R/W	R/W	R/W	R/W

Reset settings = xxx0_0011

Bit	Name	Function
7:5	Reserved	Always write this bit to zero. Reads undefined.
4	WDTE	**DAA Watchdog Timer Enable.** 0 = Watchdog timer disabled. 1 = Watchdog timer enabled. When set, this bit is cleared only by a hardware reset. The watchdog timer monitors DAA register writes. If a register write does not occur within a 4.096 second window, the DAA is put into an on-hook state. Only a write of a DAA register restarts the timer.
3	AL	**Analog Loopback.** 0 = Analog loopback mode disabled. 1 = Enables external analog loopback mode.
2	RDM	**Ring Detect Mode.** 0 = Ring detect on positive threshold. 1 = Ring detect on positive and negative threshold.
1	HBE	**Hybrid Enable.** 0 = Disconnects hybrid in transmit path. 1 = Connects hybrid in transmit path.
0	RXE	**Receive Enable.** 0 = Receive path disabled. 1 = Enables receive path.

DAA Register 3. Interrupt Mask

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDTM		FDTM		DODM	LCSM		
Type	R/W		R/W		R/W	R/W		

Reset settings = 0x0x_00xx

Bit	Name	Function
7	RDTM	**Ring Detect Interrupt Mask.** 0 = A ring signal does not cause an interrupt. 1 = A ring signal causes an interrupt.
6	Reserved	Always write this bit to zero. Reads undefined.
5	FDTM	**Frame Detect Interrupt Mask.** 0 = Isolation capacitor frame lock does not cause an interrupt. 1 = Isolation capacitor frame lock causes an interrupt.
4	Reserved	Always write this bit to zero. Reads undefined.
3	DODM	**Drop Out Detect Interrupt Mask.** 0 = A line supply dropout does not cause an interrupt. 1 = A line supply dropout causes an interrupt.
2	LCSM	**Loop Current Sense Overload Interrupt Mask.** 0 = Loop current sense overload does not cause an interrupt. 1 = Loop current sense overload causes an interrupt.
1:0	Reserved	Always write this bit to zero. Reads undefined.

DAA Register 4. Interrupt Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDTI		FDTI		DODI	LCSI		
Type	R/W		R/W		R/W	R/W		

Reset settings = 0x0x_00xx

Bit	Name	Function
7	RDTI	**Ring Detect Interrupt Status.** 0 = No ring. 1 = Ring detected. Write 0 to clear.
6	Reserved	Always write this bit to zero. Reads undefined.
5	FDTI	**Frame Detect Interrupt Status.** 0 = Frame detect established. 1 = Frame detect lost. Write 0 to clear.
4	Reserved	Always write this bit to zero. Reads undefined.
3	DODI	**Drop Out Detect Interrupt Status.** 0 = Line-side power available. 1 = Line-side power unavailable.
2	LCSI	**Loop Current Sense Overload Interrupt.** 0 = The LCS bits have not reached max (all ones). 1 = The LCS bits have reached max value. If the LCSM bit is set, a hardware interrupt occurs. This bit must be written to 0 to clear it.
1:0	Reserved	Always write this bit to zero. Reads undefined.

DAA Register 5. DAA Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		RDTN	RDTP		ONHM	RDT		OH
Type		R	R		R/W	R		R/W

Reset settings = x00x_00x0

Bit	Name	Function
7	Reserved	Always write this bit to zero. Reads undefined.
6	RDTN	**Ring Detect Signal Negative.** 0 = No ring signal is occurring. 1 = A negative ring signal is occurring.
5	RDTP	**Ring Detect Signal Positive.** 0 = No ring signal is occurring. 1 = A positive ring signal is occurring.
4	Reserved	Always write this bit to zero. Reads undefined.
3	ONHM	**On-Hook Line Monitor.** 0 = Normal on-hook mode. 1 = Enables low-power monitoring mode allowing the DAA to receive line activity without going off-hook. This mode is used for caller-ID detection.
2	RDT	**Ring Detect.** 0 = Reset either five seconds after last positive ring is detected or when the system executes an off-hook. 1 = Indicates a ring is occurring.
1	Reserved	Always write this bit to zero. Reads undefined.
0	OH	**Off-Hook.** 0 = Line-side device on-hook. 1 = Causes the line-side device to go off-hook.

DAA Register 6. DAA Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				PDL	PDN			
Type				R/W	R/W			

Reset settings = xxx1_0xxx

Bit	Name	Function
7:5	Reserved	Always write this bit to zero. Reads undefined.
4	PDL	**Powerdown Line-Side Chip.** 0 = Normal operation. Program the clock generator before clearing this bit. 1 = Powers down the Si3068.
3	PDN	**Powerdown DAA.** 0 = Normal operation. 1 = Powers down the DAA logic. A DAA soft reset is required to restore normal operation.
2:0	Reserved	Always write this bit to zero. Reads undefined.

DAA Register 7. Sample Rate Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					SRC[3:0]			
Type	R/W							

Reset settings = xxxx_0001

Bit	Name	Function
7:4	Reserved	Always write this bit to zero. Reads undefined.
3:0	SRC[3:0]	**Sample Rate Control.** Sets the sampling rate. 0000 = 7200 Hz 0001 = 8000 Hz 0010 = 8229 Hz 0011 = 8400 Hz 0100 = 9000 Hz 0101 = 9600 Hz 0110 = 10286 Hz 0111 = 12000 Hz 1000 = 13714 Hz 1001 = 16000 Hz 1010–1111 = Reserved

DAA Register 8. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	Reserved	Always write this bit to zero. Reads undefined.

DAA Register 9. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	Reserved	Always write this bit to zero. Reads undefined.

DAA Register 10. DAA Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								DDL
Type								R/W

Reset settings = xxxx_xxx0

Bit	Name	Function
7:1	Reserved	Always write this bit to zero. Reads undefined.
0	DDL	**Digital Data Loopback.** 0 = Normal Operation. 1 = Loopback transmit to receive before the filters. Output data is identical to input data.

DAA Register 11. System-Side Revision

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LSID[3:0]				REVA[3:0]			
Type	R				R			

Reset settings = xxxx_xxxx

Bit	Name	Function
7:4	LSID[3:0]	**Line-Side ID.** 1011 = Si3068
3:0	REVA[3:0]	**System-Side Revision.** Four bit value indicating the revision of the system-side device.

DAA Register 12. Line-Side Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		FDT		LCS[4:0]				
Type	R			R				

Reset settings = xxxx_xxxx

Bit	Name	Function
7	Reserved	Read returns zero.
6	FDT	**Frame Detect.** 0 = Indicates isolation capacitor link has not established frame lock. 1 = Indicates isolation capacitor link frame lock is established.
5	Reserved	Always write this bit to zero. Reads undefined.
4:0	LCS[4:0]	**Loop Current Sense.** Five-bit value returning the loop current in 3.3 mA/bit resolution when the DAA is in an off-hook state. 00000–00011 = Indicates the loop current is less than required for normal operation. 00100 = Indicates minimum loop current for normal operation. 00101 = 11110 = Normal operation 11111 = Indicates loop current is > 160 mA.

DAA Register 13. Line-Side Revision

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			REVB[3:0]					
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:6	Reserved	Always write this bit to zero. Reads undefined.
5:2	REVB[3:0]	**Line-Side Revision.** Four-bit value indicating the revision of the Si3068 device. 1000 = Revision A; 1001 = Revision B
1:0	Reserved	Always write this bit to zero. Reads undefined.

DAA Register 14. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	Reserved	Always write this bit to zero. Reads undefined.

DAA Register 15. TX/RX Gain Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXM	ATX[2:0]			RXM	ARX[2:0]		
Type	R/W	R/W			R/W	R/W		

Reset settings = 0000_0000

Bit	Name	Function
7	TXM	**Transmit Mute.** 0 = Transmit signal is not muted. 1 = Mutes the transmit signal.
6:4	ATX[2:0]	**Analog Transmit Attenuation.** 000 = 0 dB attenuation 001 = 3 dB attenuation 010 = 6 dB attenuation 011 = 9 dB attenuation 1xx = 12 dB attenuation
3	RXM	**Receive Mute.** 0 = Receive signal is not muted. 1 = Mutes the receive signal.
2:0	ARX[2:0]	**Analog Receive Gain.** 000 = 0 dB gain 001 = 3 dB gain 010 = 6 dB gain 011 = 9 dB gain 1xx = 12 dB gain

DAA Register 16. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = xxx1_xxxx

Bit	Name	Function
7:0	Reserved	Always write this bit to zero. Reads undefined.

DAA Register 17. Calibration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			ADCC					
Type			R/W					

Reset Settings = xx0x_xxxx

Bit	Name	Function
7:6	Reserved	Always write this bit to zero. Reads undefined.
5	ADCC	**ADC Calibration.** 1 = Calibration disabled.
4:0	Reserved	Always write this bit to zero. Reads undefined.

DAA Register 18. International Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							RFWE	
Type							R/W	

Reset Settings = xxxx_xx0x

Bit	Name	Function
7:2	Reserved	Always write this bit to zero. Reads undefined.
1	RFWE	**Ring Detector Full-Wave Rectifier Enable.** When RNGV is disabled, this bit controls the ring detector mode. When RNGV is enabled, this bit configures the RDT bit to either follow the ringing signal detected by the ring validation circuit, or to follow an unqualified ring detect one-shot signal initiated by a ring-threshold crossing and terminated by a fixed counter timeout of approximately five seconds. **RNGV** **RFWE** **RDT bit** 0 0 Half-Wave 0 1 Full-Wave 1 0 Validated Ring Envelope 1 1 Ring Threshold Crossing One-Shot
0	Reserved	Always write this bit to zero. Reads undefined.

DAA Register 19. Dropout Detect

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							DOD	
Type							R	

Reset Settings = xxxx_xxxx

Bit	Name	Function
7:2	Reserved	Always write this bit to zero. Reads undefined.
1	DOD	**Dropout Detect.** 0 = Normal operation. 1 = Dropout detected.
0	Reserved	Always write this bit to zero. Reads undefined.

DAA Register 20. Call Progress Receive Attenuation

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ARM[7:0]							
Type	R/W							

Reset settings = xxxx_0000

Bit	Name	Function
7:0	ARM[7:0]	**AOUT Receive Path Attenuation.** When decremented from the default setting, these bits linearly attenuate the AOUT receive path signal used for call progress monitoring. Setting the bits to 0s mutes the AOUT receive path. 0111_1111 = +6 dB (gain) 0100_0000 = 0 dB 0010_0000 = –6 dB (attenuation) 0001_0000 = –12 dB ... 0000_0000 = Mute

DAA Register 21. Call Progress Transmit Attenuation

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ATM[7:0]							
Type	R/W							

Reset settings = xxxx_0000

Bit	Name	Function
7:0	ATM[7:0]	**AOUT Transmit Path Attenuation.** When decremented from the default setting, these bits linearly attenuate the AOUT transmit path signal used for call progress monitoring. Setting the bits to 0s mutes the AOUT transmit path. 0111_1111 = +6 dB (gain) 0100_0000 = 0 dB 0010_0000 = –6 dB (attenuation) 0001_0000 = –12 dB ... 0000_0000 = Mute

DAA Register 22. Ring Validation Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDLY[1:0]		RMX[5:0]					
Type	R/W		R/W					

Reset settings = 1001_0110

Bit	Name	Function
7:6	RDLY[1:0]	**Ring Delay.** These bits, in combination with the RDLY[2] bit, set the amount of time between when a ring signal is validated and when a valid ring signal is indicated. **RDLY[2] RDLY[1:0] Delay** 0 00 0 ms 0 01 256 ms 0 10 512 ms ... 1 11 1792 ms
5:0	RMX[5:0]	**Ring Assertion Maximum Count.** These bits set the maximum ring frequency for a valid ring signal within a 10% margin of error. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. When a subsequent TIP/RING event occurs, the timer value is compared to the RMX[5:0] field, and, if it exceeds the value in RMX[5:0], the frequency of the ring is too high and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/(2 x 20 Hz) = 25 ms. To calculate the correct RMX[5:0] value for a frequency range [f_min, f_max], the following equation should be used: $$RMX[5:0] = RAS[5:0] - \frac{1}{2 \times f\_max \times 2\ ms},\ RMX \leq RAS$$ To compensate for error margin and ensure a sufficient ring detection window, it is recommended that the calculated value of RMX[5:0] be incremented by 1.

DAA Register 23. Ring Validation Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDLY[2]	RTO[3:0]				RCC[2:0]		
Type	R/W	R/W				R/W		

Reset settings = 0010_1101

Bit	Name	Function
7	RDLY[2]	**Ring Delay Bit 2.** This bit, in combination with the RDLY[1:0] bits, sets the amount of time between when a ring signal is validated and when a valid ring signal is indicated. **RDLY[2] RDLY[1:0] Delay** 0 00 0 ms 0 01 256 ms 0 10 512 ms ... 1 11 1792 ms
6:3	RTO[3:0]	**Ring Timeout.** Determine when ringing is finished after the most recent ring threshold crossing. 0000 = Invalid 0001 = 128 x 1 = 128 ms 0010 = 128 x 2 = 256 ms ... 1111 = 128 x 15 = 1920 ms
2:0	RCC[2:0]	**Ring Confirmation Count.** Determine the time interval over which the ring signal must meet tolerances defined by RAS[5:0] and RMX[5:0] to be classified as a valid ring signal. 000 = 100 ms 001 = 150 ms 010 = 200 ms 011 = 256 ms 100 = 384 ms 101 = 512 ms 110 = 640 ms 111 = 1024 ms

DAA Register 24. Ring Validation Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RNGV		RAS[5:0]					
Type	R/W		R/W					

Reset settings = 0x01_1001

Bit	Name	Function
7	RNGV	**Ring Validation Enable.** 0 = Ring validation feature is disabled. 1 = Ring validation feature is enabled in normal operating mode and low-power mode.
6	Reserved	Always write this bit to zero. Reads undefined.
5:0	RAS[5:0]	**Ring Assertion Time.** These bits set the minimum ring frequency for a valid ring signal. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. If a second or subsequent TIP/RING event occurs after the timer has timed out, the frequency of the ring is too low and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/(2 x 20 Hz) = 25 ms. To calculate the correct RAS[5:0] value for a frequency range [f_min, f_max], the following equation should be used: $RAS[5:0] \geq \frac{1}{2 \times f\_min \times 2\ ms}$, $RMX \leq RAS$

DAA Register 25-28. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	Reserved	Always write this bit to zero. Reads undefined.

DAA Register 29. Line Voltage Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		LVS[6:0]						
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7	Reserved	Always write this bit to zero. Reads undefined.
6:0	LVS	**Line Voltage Status** 1 LSB = 1 V

DAA Register 30-59. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	Reserved	Always write this bit to zero. Reads undefined.

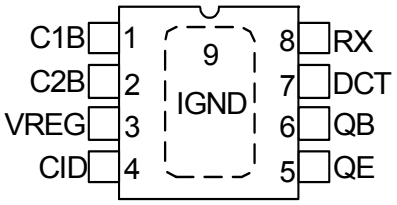
DAA Register 60. Line-Side ID

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						LSID4		
Type	R/W							

Reset settings = xxxx_x1xx

Bit	Name	Function
7:3	Reserved	Always write this bit to zero. Reads undefined.
2	LSID4	**Line-Side ID.** LSID = 1 for Si3068
1:0	Reserved	Always write this bit to zero. Reads undefined.

6. Pin Descriptions



Pin #	Pin Name	Description
1	C1B	**Isolation Capacitor 1B.** Connects to one side of isolation capacitor C1 and communicates with the system-side module.
2	C2B	**Isolation Capacitor 2B.** Connects to one side of isolation capacitor C2 and communicates with the system-side module.
3	VREG	**Voltage Regulator.** Connects to an external capacitor to provide bypassing for an internal power supply.
4	CID	**Caller ID.** Caller ID input.
5	QE	**Transistor Emitter.** Connects to the emitter of Q3.
6	QB	**Transistor Base.** Connects to the base of transistor Q3. Used to go on- and off-hook.
7	DCT	**DC Termination.** Provides dc termination to the telephone network.
8	RX	**Receive Input.** Serves as the receive side input from the telephone network.
9	IGND	**Isolated Ground (exposed pad).** Connects to ground on the line-side interface.

7. Ordering Guide

Part Number*	Package	Lead-Free	Temp Range
Si3068-B-FS	e-Pad SOIC	Yes	0 to 70 °C
***Note:** Add an “R” at the end of the device to denote tape and reel option; 2500 quantity per reel.			

8. Package Outline: 8-Pin Exposed Pad SOIC

Figure 10 illustrates the package details for the Si3068. Table 10 lists the values for the dimensions shown in the illustration.

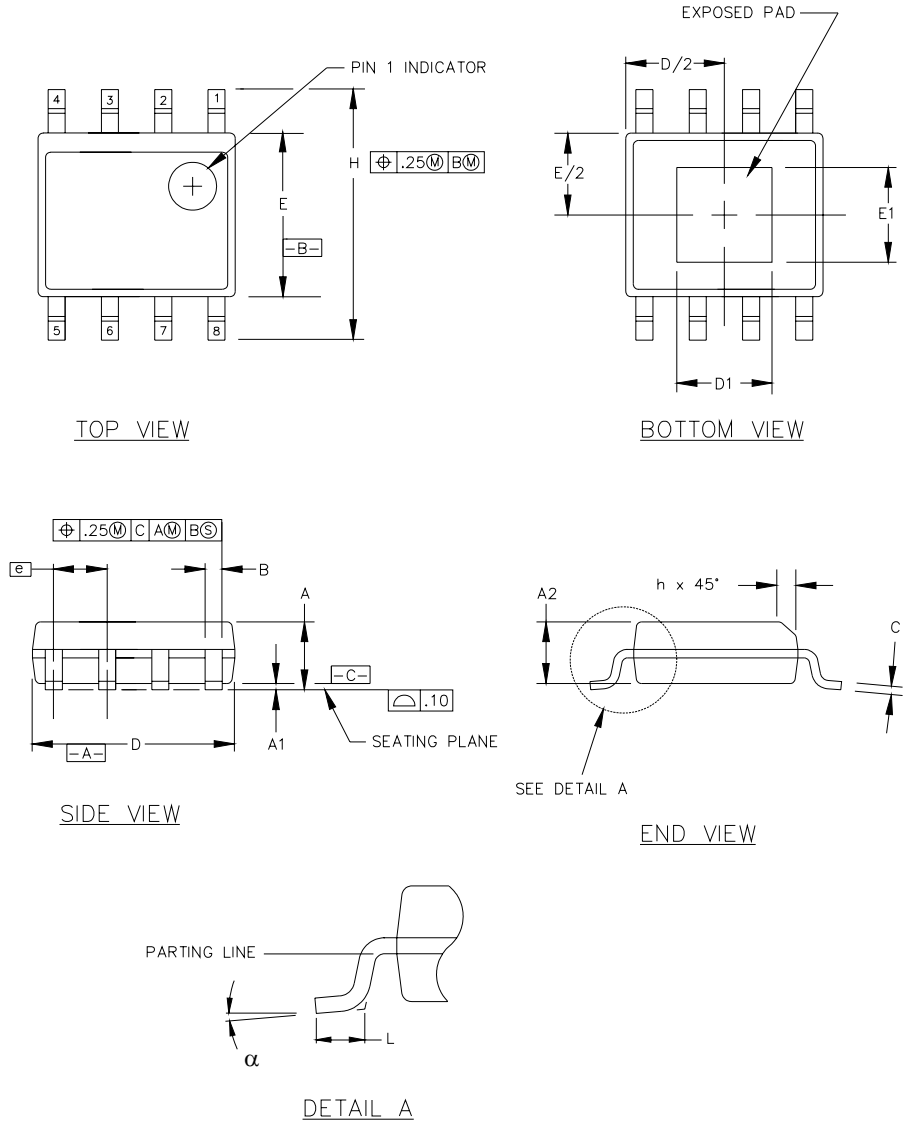


Figure 10. 8-pin Exposed Pad Small Outline Integrated Circuit (SOIC) Package

Table 10. Package Diagram Dimensions

Dimension	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.00	0.15
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
D1	2.14	2.44
E	3.80	4.00
E1	2.14	2.44
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
∝	0°	8°

Notes:
1. All dimensions shown are in millimeters (mm).
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

NOTES:

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SILICON LABORATORIES

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Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

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http://moschip.ru/get-element

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

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