

Digital Power Management IC 2 MHz, 600 mA DC/DC with Dual 300 mA/300 mA Low V_{IN} LDOs

Features

- 2.7V to 5.5V Input Voltage Range
- 2 MHz DC/DC Converter and Two LDOs
- Integrated Power-on Reset (POR)
 - Adjustable POR Delay Time
- LOWQ Mode
 - 30 μ A Total IQ when in LOWQ Mode
- DC/DC Converter
 - Up to 600 mA of Output Current in PWM Mode
 - LOWQ Mode: NO RIPPLE Light Load Mode
 - 75 μ V_{RMS} Output Noise in LOWQ Mode
 - 2 MHz PWM Mode Operation
 - > 90% Efficiency
- LDO1 Input Voltage Directly Connected to DC/DC Converter Output Voltage for Maximum Efficiency
 - Ideal for 1.8V to 1.5V Conversion
 - 300 mA Output Current from 1.8V Input
 - Output Voltage Down to 0.8V
- LDO2 – 300 mA Output Current Capable
- Thermal Shutdown Protection
- Current Limit Protection
- Simple, Leakage-Free Interfacing to Host MPU in Applications with Backup Power
- Tiny 16-Pin 3mm x 3mm QFN Package

Applications

- Embedded MPU and MCU Power
- Portable and Wearable Applications
- Low-Power RF Systems
- Backup Power Systems

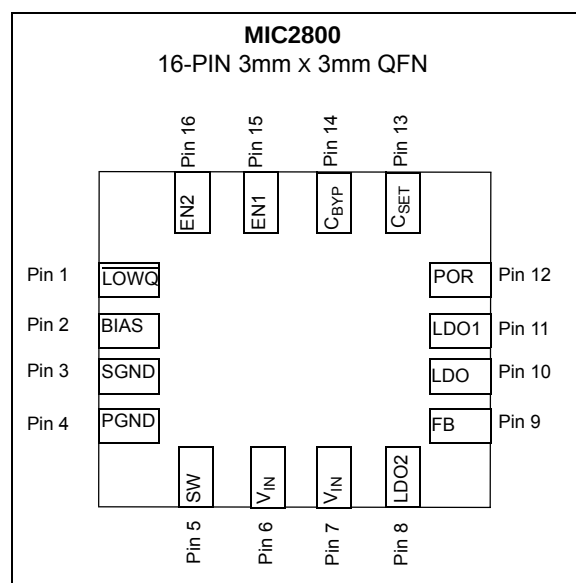
General Description

The MIC2800 is a high-performance power management IC, featuring three output voltages with maximum efficiency. Integrating a 2 MHz DC/DC converter with an LDO post-regulator, the MIC2800 gives two high-efficiency outputs with a second, 300 mA LDO for maximum flexibility. The MIC2800 features a LOWQ mode, reducing the total current draw while in this mode to less than 30 μ A. In LOWQ mode, the output noise of the DC/DC converter is reduced to 75 μ V_{RMS}, significantly lower than other converters that use a PFM light load mode that can interfere with sensitive RF circuitry.

The DC/DC converter uses small values of L and C to reduce board space but still retains efficiencies over 90% at load currents up to 600 mA.

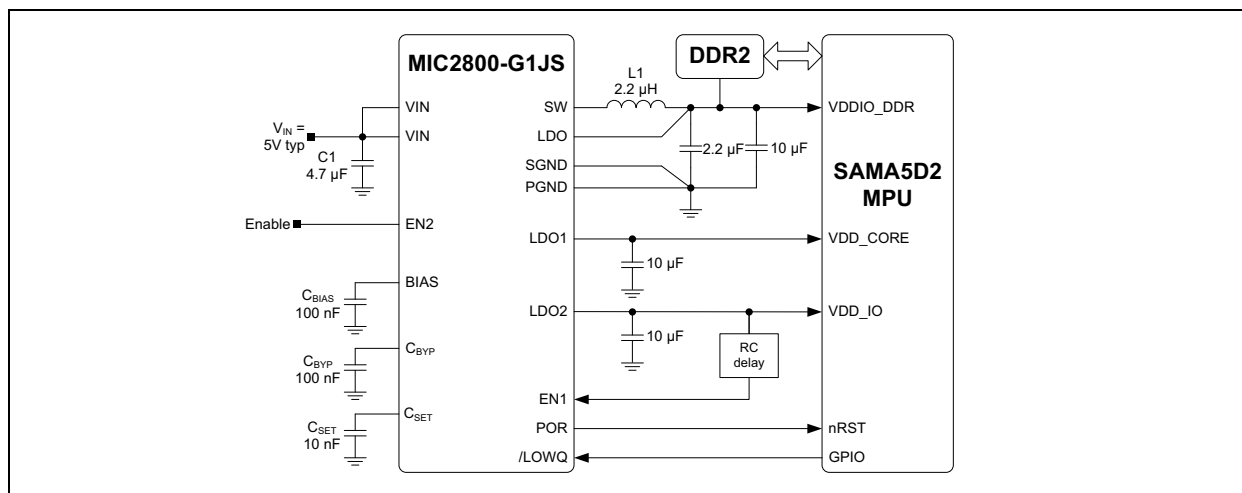
The MIC2800 operates with very small ceramic output capacitors and inductors for stability, reducing required board space and component cost and it is available in various output voltage options in the 16-pin 3mm x 3mm QFN leadless package.

Package Type

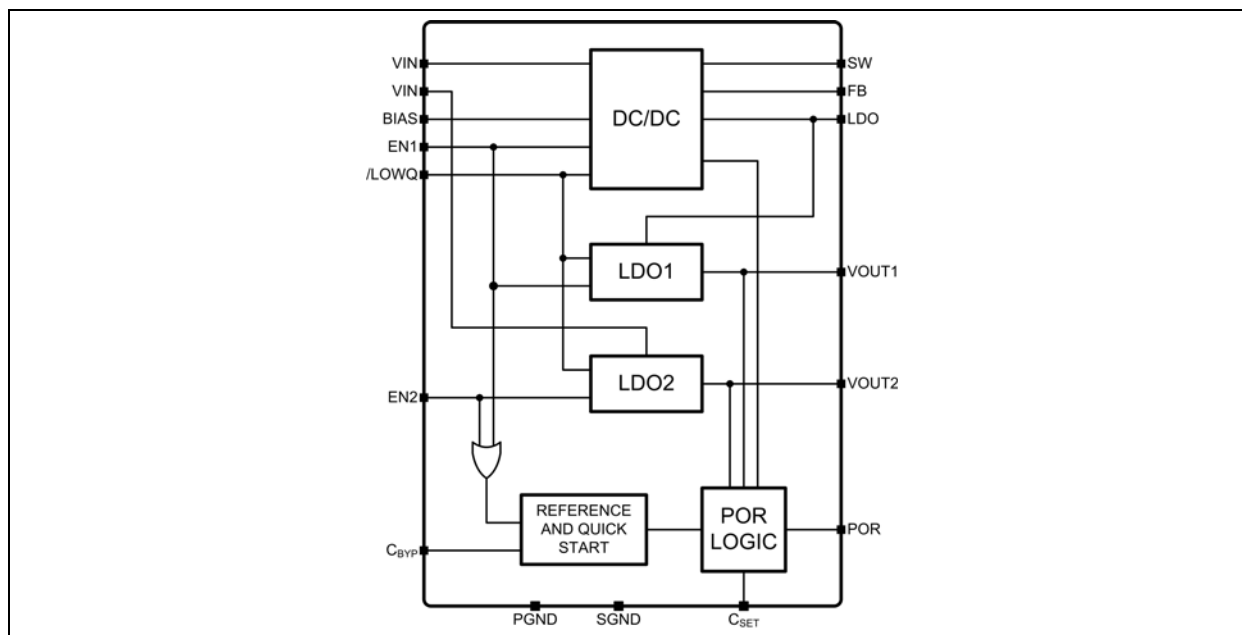


MIC2800

Typical Application Circuit (simplified)



Functional Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN})	-0.3 to +6.0V
Enable Input Voltage ($V_{EN1, EN2}$)	-0.3V to +(V _{IN} +0.3V)
LOWQ, POR	 -0.3V to +6.0V
Power Dissipation (Note 1)	 Internally Limited
Lead Temperature (soldering, 10 sec.)	 +260°C
Storage Temperature (T_S)	 -65°C to +150°C
ESD Rating (Note 2)	 2 kV

Operating Ratings ‡

Supply Voltage (V_{IN})	 +2.7V to +5.5V
Enable Input Voltage ($V_{EN1, EN2}$)	 0V to +V _{IN}
LOWQ, POR	 0V to +5.5V
Junction Temperature (T_J)	 -40°C to +125°C
Junction Thermal Resistance QFN-16 (θ_{JA})	 +45°C/W

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

- 1: The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
- 2: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

MIC2800

TABLE 1-1: ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: $V_{IN} = EN1 = EN2 = \overline{LOWQ} = V_{OUT}$ (Note 2) + 1V; $C_{OUTDC/DC} = 2.2 \mu F$, $C_{OUT1} = C_{OUT2} = 2.2 \mu F$; $I_{OUTDC/DC} = 100 \text{ mA}$;
 $I_{OUTLDO1} = I_{OUTLDO2} = 100 \mu A$; $T_J = 25^\circ C$, **bold values indicate** $-40^\circ C \leq T_J \leq +125^\circ C$; unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
UVLO Threshold	UVLO _{TH}	2.45	2.55	2.65	V	Rising input voltage during turn on
UVLO Hysteresis	UVLO _{HYS}	—	100	—	mV	
Ground Pin Current	I _{GND}	—	800 55	1100 85 95	μA	V _{FB} = GND (not switching); LDO2 Only (EN1 = LOW)
Ground Pin Current in Shutdown	I _{GND_SHDN}	—	0.2	5	μA	All EN = 0V
Ground Pin Current (LOWQ mode)	I _{GND_LOWQ}	—	30 20	60 80 70	μA μA μA	All channels ON, I _{DC/DC} = I _{LDO1} = I _{LDO2} = 0 mA DC/DC and LDO1 OFF; I _{LDO2} = 0 mA
Overtemperature Shutdown	T _{SD}	—	160	—	°C	
Overtemperature Shutdown Hysteresis	T _{SDHYS}	—	23	—	°C	
Enable Inputs (EN1; EN2; /LOWQ)						
Enable Input Voltage Logic Low	V _{IH}	—	—	0.2	V	
Enable Input Voltage Logic High	V _{IL}	1.0	—	—	V	
Enable Input Current	I _{ENLK}	—	0.1	1	μA	V _{IL} ≤ 0.2V
		—	0.1	1	μA	V _{IH} ≥ 1.0V
Turn-on Time						
Turn-on Time (LDO1 and LDO2)	t _{TURN-ON}	—	240 120	500 350	μs	EN2 = V _{IN} EN1 = V _{IN}
Turn-on Time (DC/DC)	t _{TURN-ON}	—	83	350	μs	EN2 = V _{IN} ; I _{LOAD} = 300 mA; C _{BYP} = 0.1 μF
POR Output						
POR Threshold Voltage, Falling	V _{THLOW_POR}	90	91	—	%	Low Threshold, % of nominal (V _{DC/DC} or V _{LDO1} or V _{LDO2}) (Flag ON)
POR Threshold Voltage, Rising	V _{THIGH_POR}	—	96	99	%	High Threshold, % of nominal (V _{DC/DC} AND V _{LDO1} AND V _{LDO2}) (Flag OFF)
VOL	VOL _{POR}	—	10	100	mV	POR Output Logic Low Voltage; IL = 250 μA
IPOR	ILEAK _{POR}	—	0.01	1	μA	Flag Leakage Current, Flag OFF
CSET INPUT						
CSET Pin Current Source	I _{CSET}	0.75	1.25	1.75	μA	V _{CSET} = 0V
CSET Pin Threshold Voltage	V _{TH_CSET}	—	1.25	—	V	POR = High

Note 1: Specification for packaged product only.

2: V_{OUT} denotes the highest of the three output voltage.

TABLE 1-2: ELECTRICAL CHARACTERISTICS - DC/DC CONVERTER

Electrical Characteristics: $V_{IN} = V_{OUTDC/DC} + 1V$; $EN1 = V_{IN}$; $EN2 = GND$; $I_{OUTDC/DC} = 100\text{ mA}$; $L = 2.2\text{ }\mu\text{H}$; $C_{OUTDC/DC} = 2.2\text{ }\mu\text{F}$; $T_J = 25^\circ\text{C}$, **bold** values indicate -40°C to $+125^\circ\text{C}$; unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
LOWQ = High (Full Power Mode)						
Output Voltage Accuracy	V_{OUT}	-2 -3	—	$+2$ $+3$	%	Fixed Output Voltages
Current Limit in PWM Mode	I_{LIM}	0.75	1	1.6	A	$V_{OUT} = 0.9 \cdot V_{NOM}$
FB pin voltage (ADJ only)	V_{FB}	—	800	—	mV	
FB pin input current (ADJ only)	I_{FB}	—	1	5	nA	
Output Voltage Line Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	—	0.2	—	%/V	$V_{OUT} > 2.4V$; $V_{IN} = V_{OUT} + 300\text{ mV}$ to $5.5V$, $I_{LOAD} = 100\text{ mA}$ $V_{OUT} < 2.4V$; $V_{IN} = 2.7V$ to $5.5V$, $I_{LOAD} = 100\text{ mA}$
Output Voltage Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.2	1.5	%	$20\text{ mA} < I_{LOAD} < 300\text{ mA}$
Maximum Duty Cycle	DC_{MAX}	100	—	—	%	$V_{FB} \leq 0.4V$
High-Side Switch ON-Resistance		—	0.6	—	Ω	$I_{SW} = 150\text{ mA}$ $V_{FB} = 0.7V_{FB_NOM}$
Low-Side Switch ON-Resistance			0.8			$I_{SW} = -150\text{ mA}$ $V_{FB} = 1.1V_{FB_NOM}$
Oscillator Frequency	f_{osc}	1.8	2	2.2	MHz	
Output Voltage Noise	V_N	—	60	—	μV_{RMS}	$C_{OUT} = 2.2\text{ }\mu\text{F}$; $C_{BYP} = 0.1\text{ }\mu\text{F}$; 10 Hz to 100 KHz
LOWQ = Low (Light Load Mode)						
Output Voltage Accuracy	V_{OUT}	-2.0	—	$+2.0$	%	Variation from nominal V_{OUT}
		-3.0		$+3.0$		Variation from nominal V_{OUT} ; -40°C to $+125^\circ\text{C}$
Output Voltage Temp. Coefficient	TC_{VOUT}	—	40	—	ppm/C	
Line Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	—	0.02	0.3 0.6	%/V	$V_{IN} = V_{OUT} + 1V$ to $5.5V$; $I_{OUT} = 100\text{ }\mu\text{A}$
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.2	1.5	%	$I_{OUT} = 100\text{ }\mu\text{A}$ to 50 mA
Ripple Rejection	PSRR	—	50	—	dB	$f = \text{up to } 1\text{ kHz}$; $C_{OUT} = 2.2\text{ }\mu\text{F}$; $C_{BYP} = 0.1\text{ }\mu\text{F}$
			30			$f = 20\text{ kHz}$; $C_{OUT} = 2.2\text{ }\mu\text{F}$; $C_{BYP} = 0.1\text{ }\mu\text{F}$
Current Limit	I_{LIM_LOWQ}	80	120	190	mA	$V_{OUT} = 0V$

MIC2800

TABLE 1-3: ELECTRICAL CHARACTERISTICS - LDO 1

Electrical Characteristics: $V_{IN} = V_{OUTDC/DC}$; $EN1 = V_{IN}$; $EN2 = GND$; $C_{OUT1} = 2.2 \mu F$; $I_{OUT1} = 100 \mu A$; $T_J = 25^\circ C$, **bold** values indicate $-40^\circ C \leq T_J \leq +125^\circ C$; unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
LOWQ = High (Full Power Mode)						
Output Voltage Accuracy	V_{OUT}	-2.0	—	+2.0	%	Variation from nominal V_{OUT}
		-3.0		+3.0		Variation from nominal V_{OUT} ; $-40^\circ C$ to $+125^\circ C$
Output Current Capability	I_{OUT}	300 120	—	—	mA	$V_{IN} \geq 1.8V$ $V_{IN} \geq 1.5V$
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.17 0.3	1.5	%	$I_{OUT} = 100 \mu A$ to 150 mA $I_{OUT} = 100 \mu A$ to 300 mA
Current Limit	I_{LIM}	350	500	700	mA	$V_{OUT} = 0V$
Ripple Rejection	PSRR		70	—	dB	$f = \text{up to } 1 \text{ kHz}$; $C_{OUT} = 2.2 \mu F$; $C_{BYP} = 0.1 \mu F$
			44			$f = 20 \text{ kHz}$; $C_{OUT} = 2.2 \mu F$; $C_{BYP} = 0.1 \mu F$
Output Voltage Noise	V_N	—	30	—	μV_{RMS}	$C_{OUT} = 2.2 \mu F$; $C_{BYP} = 0.1 \mu F$; 10 Hz to 100 KHz
LOWQ = Low (Light Load Mode)						
Output Voltage Accuracy	V_{OUT}	-3.0	—	+3.0	%	Variation from nominal V_{OUT}
		-4.0		+4.0		Variation from nominal V_{OUT} ; $-40^\circ C$ to $+125^\circ C$
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.2	0.5 1.0	%	$I_{OUT} = 100 \mu A$ to 10 mA
Current Limit	I_{LIM}	50	85	125	mA	$V_{OUT} = 0V$
Ripple Rejection	PSRR	—	70	—	dB	$f = \text{up to } 1 \text{ kHz}$; $C_{OUT} = 2.2 \mu F$; $C_{BYP} = 0.1 \mu F$
			42			$f = 20 \text{ kHz}$; $C_{OUT} = 2.2 \mu F$; $C_{BYP} = 0.1 \mu F$

TABLE 1-4: ELECTRICAL CHARACTERISTICS - LDO2

Electrical Characteristics: $V_{IN} = V_{OUTLDO2} + 1.0V$; $EN1 = GND$; $EN2 = V_{IN}$; $C_{OUT2} = 2.2 \mu F$; $I_{OUTLDO2} = 100 \mu A$; $T_J = 25^\circ C$, **bold** values indicate $-40^\circ C \leq T_J \leq +125^\circ C$; unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
LOWQ = High (Full Power Mode)						
Output Voltage Accuracy	V_{OUT}	-2.0	—	+2.0	%	Variation from nominal V_{OUT}
		-3.0		+3.0		Variation from nominal V_{OUT} ; $-40^\circ C$ to $+125^\circ C$
Line Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	—	0.02	0.3 0.6	%/V	$V_{IN} = V_{OUT} + 1V$ to 5.5V; $I_{OUT} = 100 \mu A$
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.20 0.25 0.40	1.5	%	$I_{OUT} = 100 \mu A$ to 150 mA $I_{OUT} = 100 \mu A$ to 200 mA $I_{OUT} = 100 \mu A$ to 300 mA
Dropout Voltage	V_{DO}	—	70 94 142	300	mV	$I_{OUT} = 150 mA$; $V_{OUTLDO2} \geq 2.7V$ $I_{OUT} = 200 mA$; $V_{OUTLDO2} \geq 2.7V$ $I_{OUT} = 300 mA$; $V_{OUTLDO2} \geq 2.7V$
Ripple Rejection	PSRR	—	75	—	dB	$f = \text{up to } 1 \text{ kHz}$; $C_{OUT} = 2.2 \mu F$; $C_{BYP} = 0.1 \mu F$
			40			$f = 20 \text{ kHz}$; $C_{OUT} = 2.2 \mu F$; $C_{BYP} = 0.1 \mu F$
Current Limit	I_{LIM}	400	550	850	mA	$V_{OUT} = 0V$
Output Voltage Noise	V_N	—	25	—	μV_{RMS}	$C_{OUT} = 2.2 \mu F$; $C_{BYP} = 0.1 \mu F$; 10 Hz to 100 KHz
LOWQ = Low (Light Load Mode)						
Output Voltage Accuracy	V_{OUT}	-3.0	—	+3.0	%	Variation from nominal V_{OUT}
		-4.0		+4.0		Variation from nominal V_{OUT} ; $-40^\circ C$ to $+125^\circ C$
Line Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	—	0.02	0.3 0.6	%/V	$V_{IN} = V_{OUT} + 1V$ to 5.5V
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.2	1.0	%	$I_{OUT} = 100 \mu A$ to 10 mA
Dropout Voltage	V_{DO}	—	22	35 50	mV	$I_{OUT} = 10 mA$; $V_{OUTLDO2} \geq 2.7V$
Ripple Rejection	PSRR	—	75	—	dB	$f = \text{up to } 1 \text{ kHz}$; $C_{OUT} = 2.2 \mu F$; $C_{BYP} = 0.1 \mu F$
			55			$f = 20 \text{ kHz}$; $C_{OUT} = 2.2 \mu F$; $C_{BYP} = 0.1 \mu F$
Current Limit	I_{LIM}	50	85	125	mA	$V_{IN} = 2.7V$; $V_{OUT} = 0V$

TABLE 1-5: TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	-65	—	+150	°C	
Lead Temperature	—	—	—	+260	°C	Soldering, 10 sec.
Junction Temperature	T_J	-40	—	+125	°C	
Package Thermal Resistance						
16-Ld QFN	θ_{JA}	—	45	—	°C/W	

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A , T_J , θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

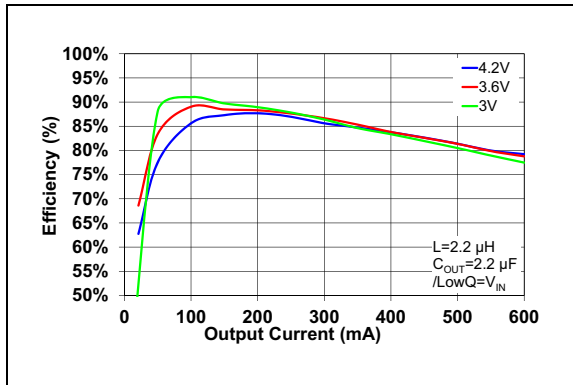


FIGURE 2-1: DC/DC 1.87V_{OUT} Efficiency.

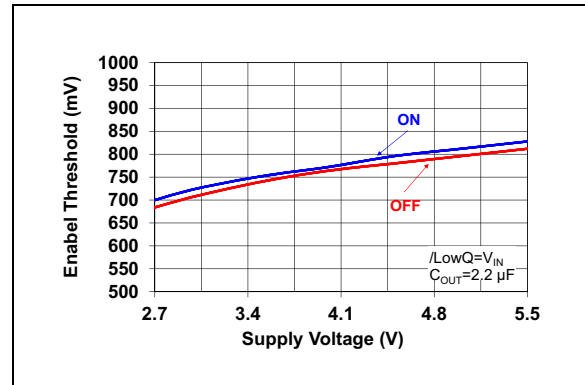


FIGURE 2-4: DC/DC Enable Threshold vs. Supply Voltage.

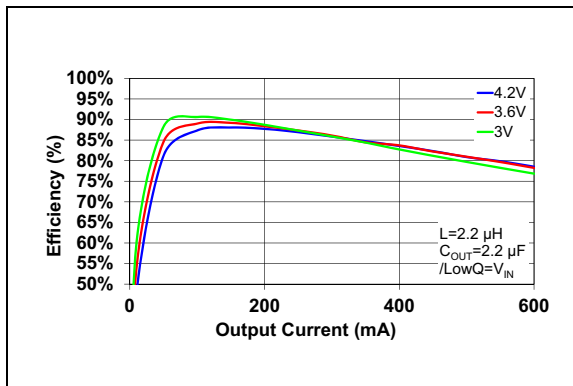


FIGURE 2-2: DC/DC 1.8V_{OUT} Efficiency.

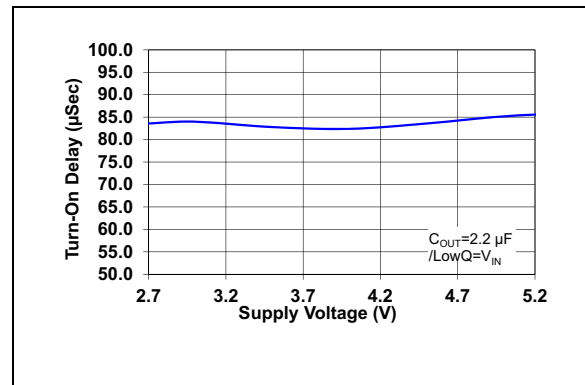


FIGURE 2-5: DC/DC Turn-on Delay vs. Supply Voltage.

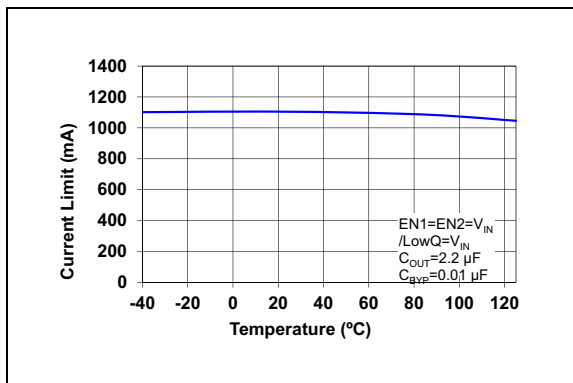


FIGURE 2-3: DC/DC Current Limit vs. Temperature.

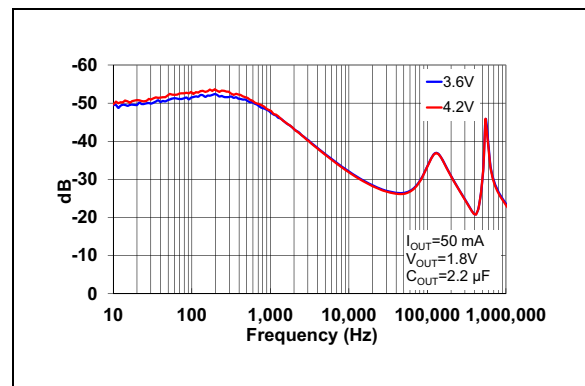


FIGURE 2-6: DC/DC LowQ Mode Power Supply Rejection Ratio vs. Input Voltage.

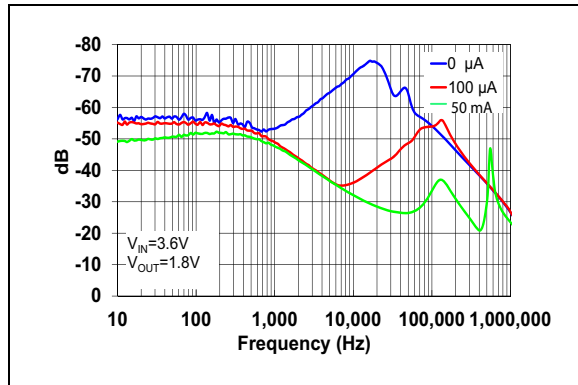


FIGURE 2-7: DC/DC LowQ Mode Power Rejection Ratio vs. Output Current.

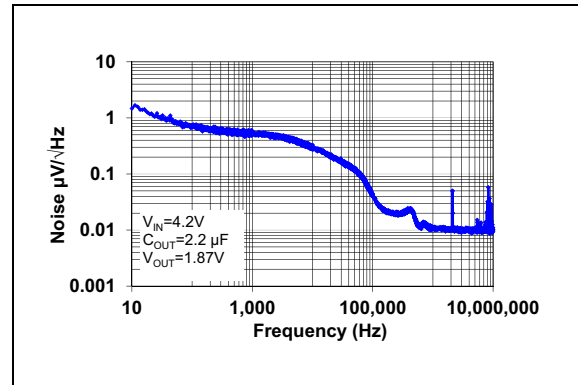


FIGURE 2-10: DC/DC LowQ Mode LDO Output Noise Spectral Density.

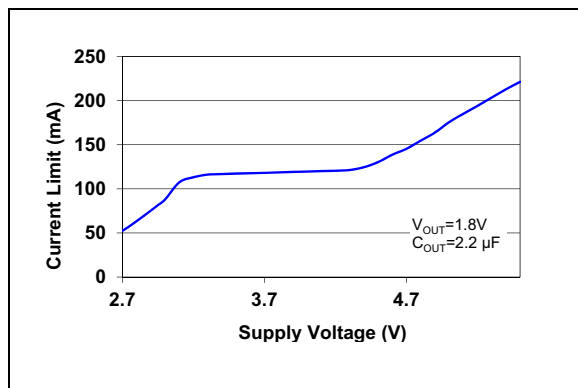


FIGURE 2-8: DC/DC LowQ Mode LDO Current Limit vs. Supply Voltage.

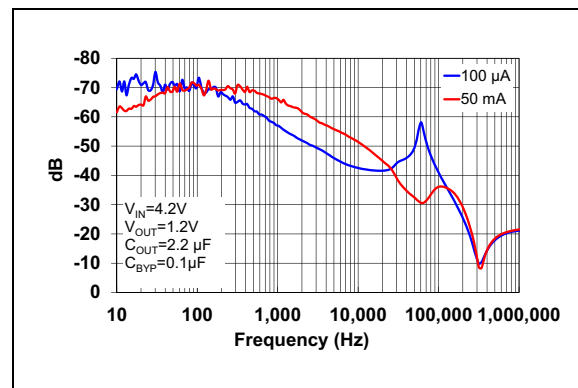


FIGURE 2-11: Power Supply Rejection Ratio (LDO1 LowQ Mode).

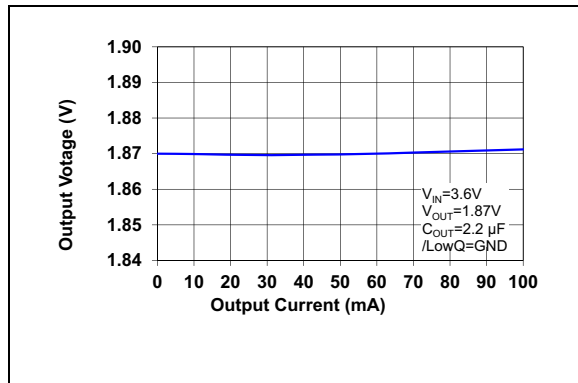


FIGURE 2-9: DC/DC LowQ Mode LDO Output Voltage vs. Output Current.

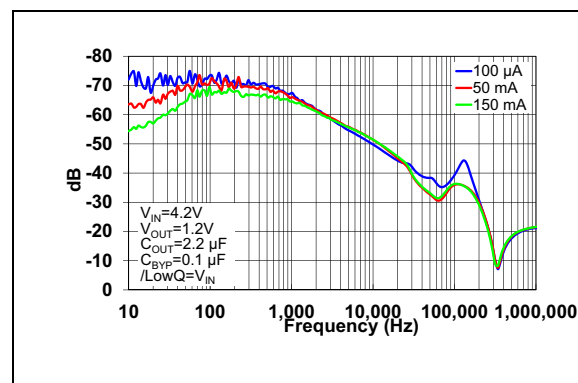


FIGURE 2-12: Power Supply Rejection Ratio (LDO1 Normal Mode).

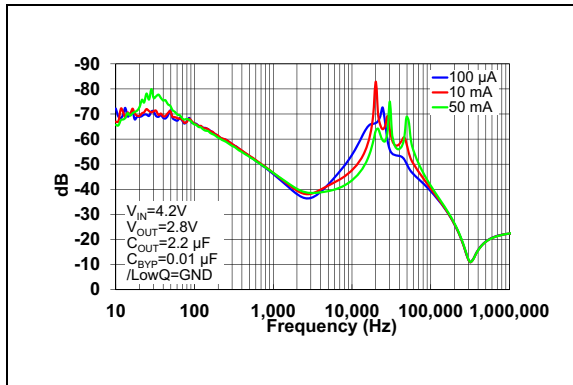


FIGURE 2-13: Power Supply Rejection Ratio (LDO2 LowQ Mode).

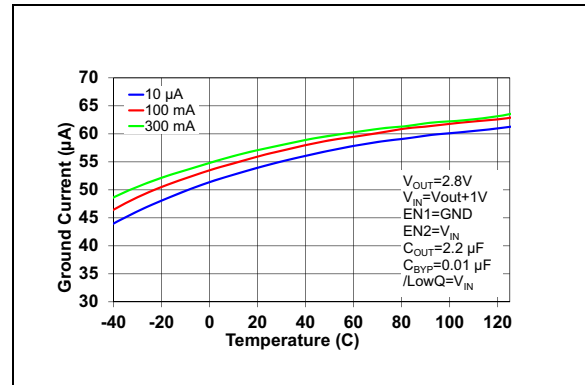


FIGURE 2-16: Ground Current vs. Temperature.

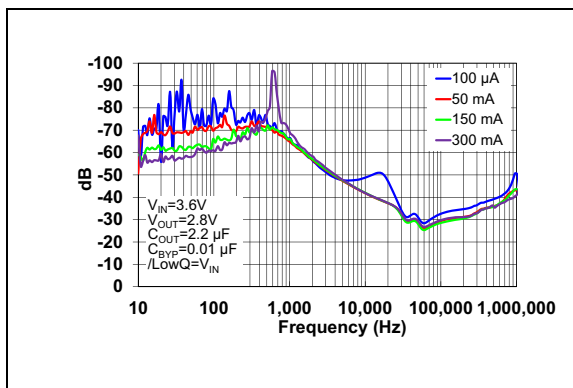


FIGURE 2-14: Power Supply Rejection Ratio (LDO2 Normal Mode).

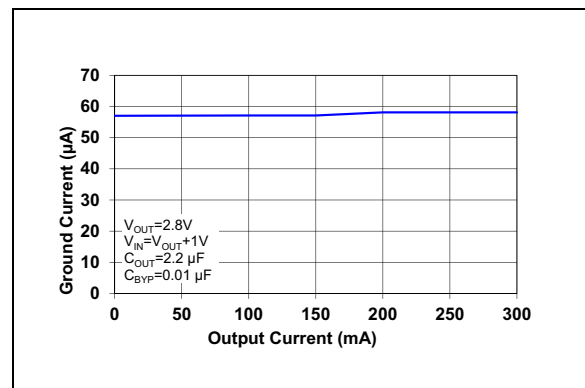


FIGURE 2-17: Ground Current vs. Output Current.

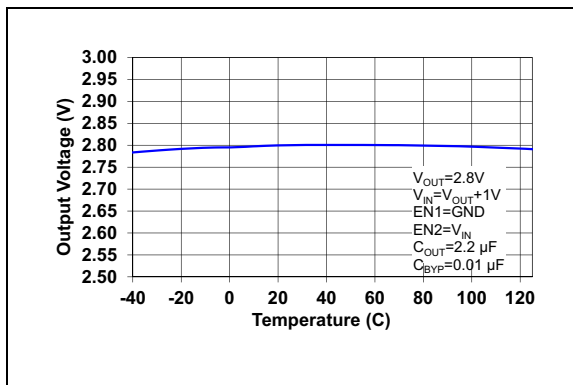


FIGURE 2-15: LDO2 Output Voltage vs. Temperature.

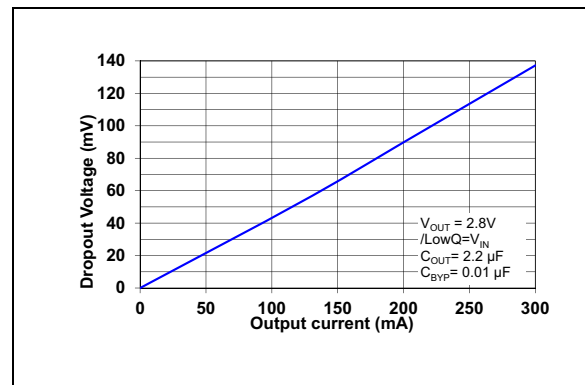


FIGURE 2-18: LDO2 Dropout Voltage vs. Output Current.

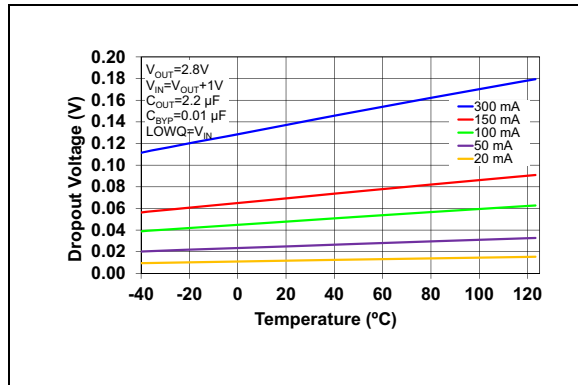


FIGURE 2-19: LDO 2 Dropout Voltage vs. Temperature.

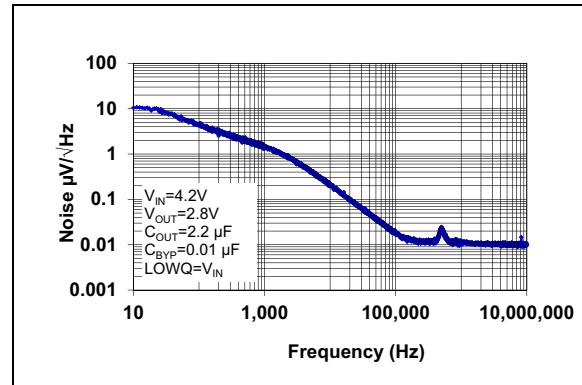


FIGURE 2-22: LDO2 Output Noise Spectral Density.

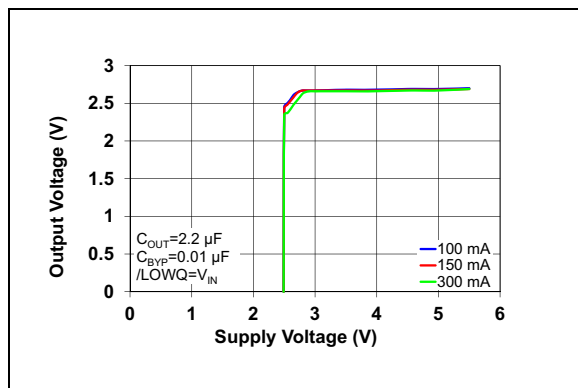


FIGURE 2-20: Dropout Characteristics.

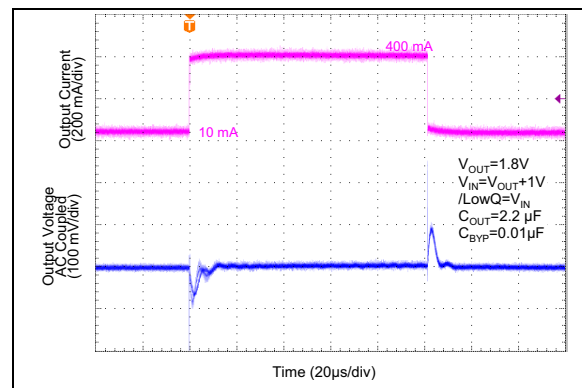


FIGURE 2-23: DC/DC Load Transient PWM Mode.

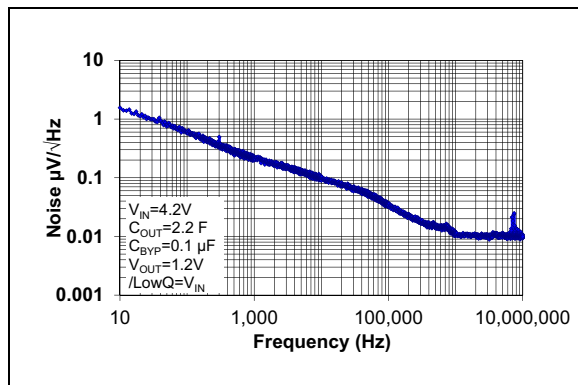


FIGURE 2-21: LDO1 Output Noise Spectral Density.

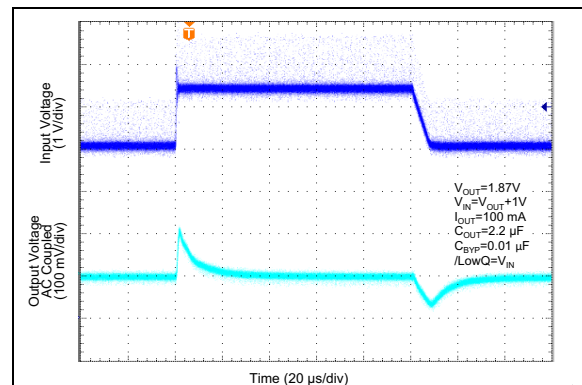


FIGURE 2-24: DC/DC Line Transient PWM Mode.

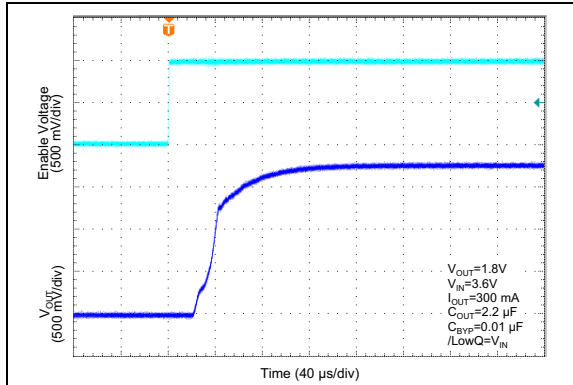


FIGURE 2-25: Enable Transient PWM Mode.

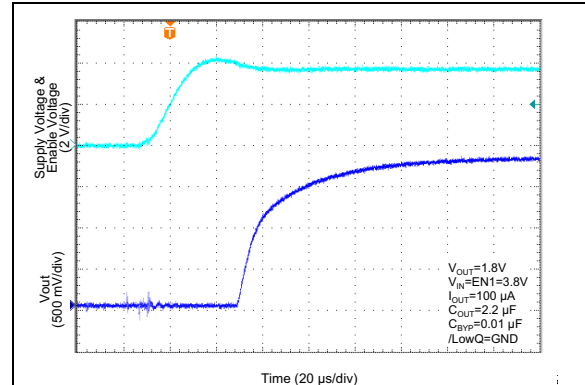


FIGURE 2-28: Enable Transient LowQ Mode.

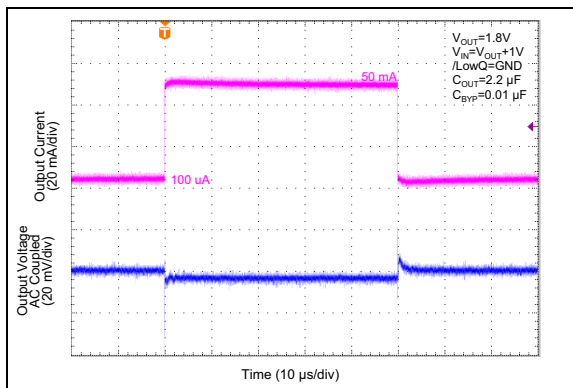


FIGURE 2-26: DC/DC Load Transient LowQ Mode.

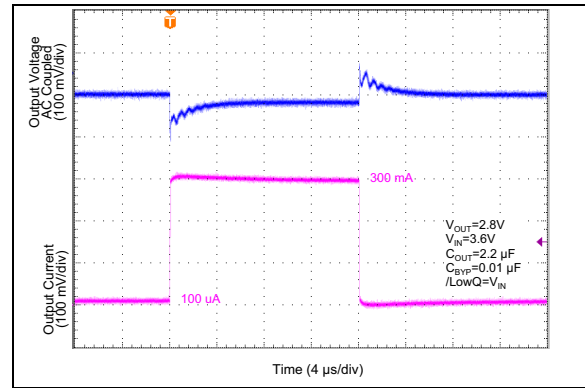


FIGURE 2-29: LDO2 Load Transient Normal Mode.

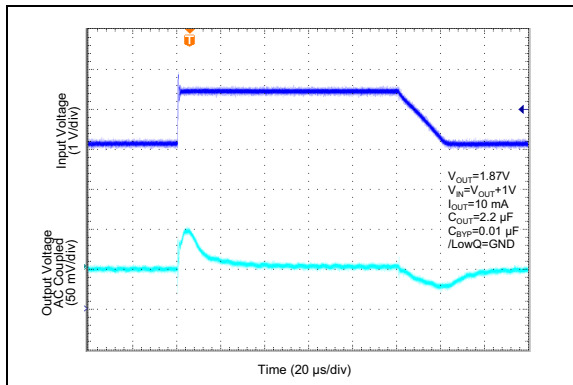


FIGURE 2-27: DC/DC Line Transient LowQ Mode.

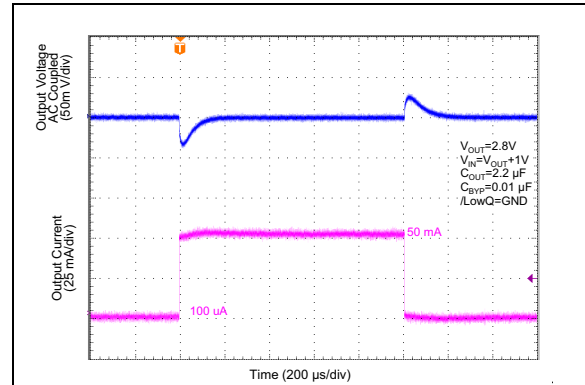


FIGURE 2-30: LDO Load Transient LowQ Mode.

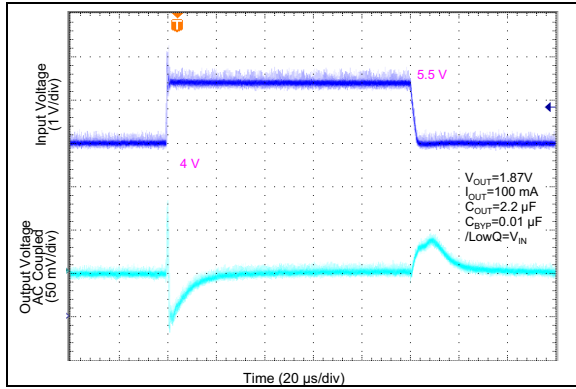


FIGURE 2-31: LDO2 Line Transient Normal Mode.

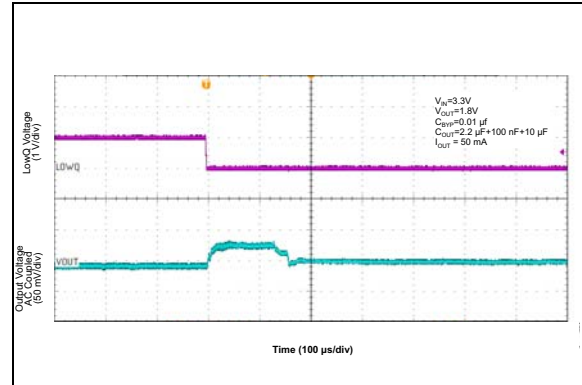


FIGURE 2-34: DC/DC PWM Mode to LowQ Mode Transition.

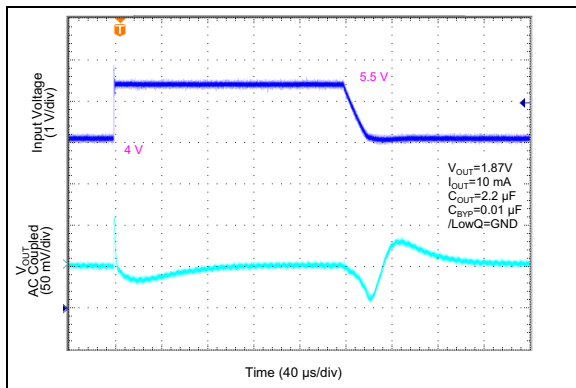


FIGURE 2-32: LDO2 Line Transient LowQ Mode.

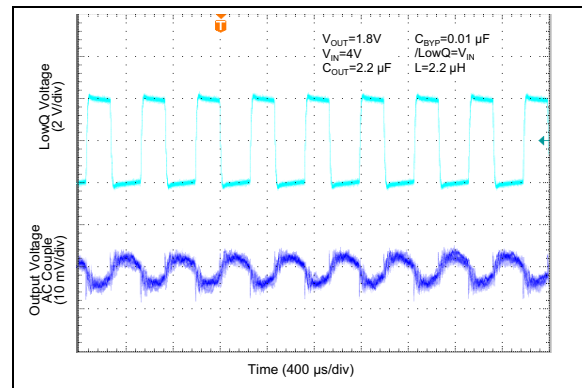


FIGURE 2-35: DC/DC PWM Waveform.

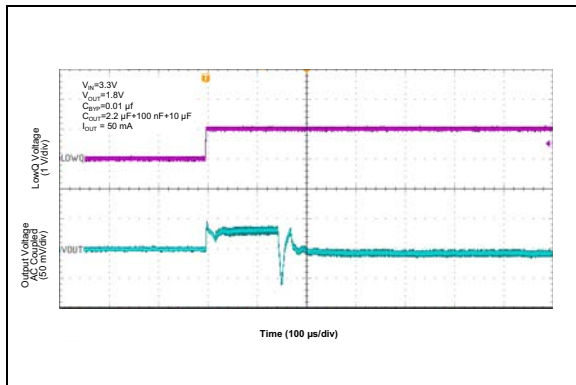


FIGURE 2-33: DC/DC LowQ Mode to PWM Mode Transition.

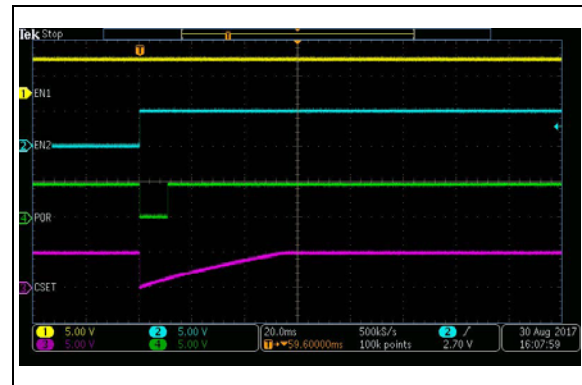


FIGURE 2-36: POR Behavior, EN1 = High, Low-to-High Transition on EN2.

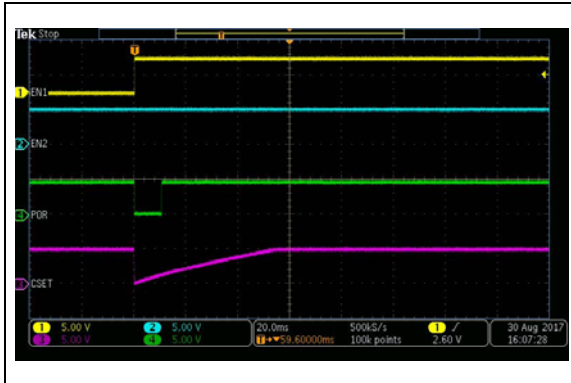


FIGURE 2-37: POR Behavior, EN2 = High, Low-to-High Transition on EN1.



FIGURE 2-38: C_{SET} Pin Voltage and POR Delay Time Behavior for Correct Sequencing.

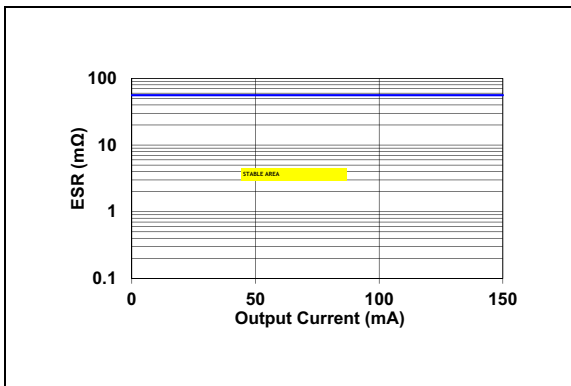


FIGURE 2-39: ESR vs. Load - LDO.

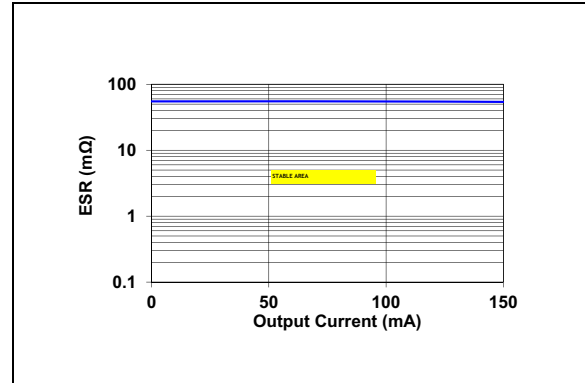


FIGURE 2-40: ESR vs. Load - LDO1.

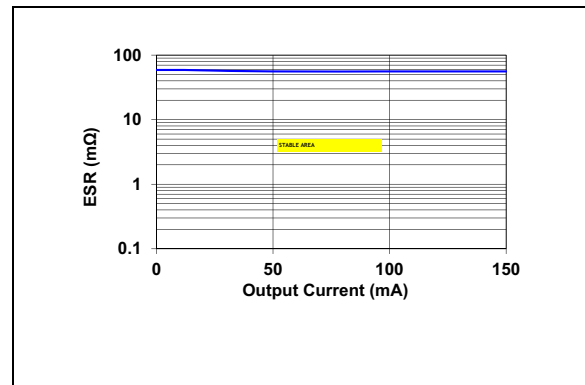


FIGURE 2-41: ESR vs. Load - LDO2.

MIC2800

NOTES:

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

Pin Number 16-Pin QFN	Pin Name	Description
1	LOWQ	LOWQ Mode. Active Low Input. Logic High = Full Power Mode; Logic Low = LOWQ Mode; Do not leave floating.
2	BIAS	Internal circuit bias supply. It must be decoupled to signal ground with a 0.1 μ F capacitor and should not be loaded.
3	SGND	Signal ground
4	PGND	Power ground
5	SW	Switch (Output): Internal power MOSFET output switches.
6	V _{IN}	Supply Input – DC/DC. Must be tied to PIN7 externally.
7	V _{IN}	Supply Input – LDO2. Must be tied to PIN6 externally.
8	LDO2	Output of LDO regulator 2.
9	FB	Feedback. Input to the error amplifier for DC/DC converter. For fixed output voltages connect directly to V _{OUT} and an internal resistor network sets the output voltage.
10	LDO	LDO Output: Connect to V _{OUT} of the DC/DC for LOWQ mode operation.
11	LDO1	Output of LDO regulator 1.
12	POR	Power-on Reset Output: Open-drain output. Active low indicates an output undervoltage condition on either one of the three regulated outputs.
13	C _{SET}	Delay Set Input: connect external capacitor to GND to set the internal delay for the POR output. When left open, there is a minimum delay. This pin cannot be grounded.
14	C _{BYP}	Reference Bypass: connect external 0.1 μ F to GND to reduce output noise. May be left open.
15	EN1	Enable Input (DC/DC and LDO1). Active High Input. Logic high = On; Logic low = Off; do not leave floating.
16	EN2	Enable Input (LDO 2). Active High Input. Logic high = On; Logic low = Off; do not leave floating.

3.1 LOWQ

The LOWQ pin provides a logic level control between the internal PWM mode and the low noise linear regulator mode. With LOWQ pulled low (<0.2V), quiescent current of the device is greatly reduced by switching to a low noise linear regulator mode that has a typical IQ of 20 μ A (LDO2 ON only). In LowQ mode the LDO output can deliver 60 mA of current to the output. By placing LOWQ high (>1V), the device transitions into a constant frequency PWM buck regulator mode. This allows the device the ability to efficiently deliver up to 600 mA of output current at the same output voltage, and to support load transients generated by processor activity.

LOWQ mode also limits the output load of both LDO1 and LDO2 to 10 mA.

The ESD protection of the LOWQ pin is free from clamping diodes to the input supply rails, therefore the LOWQ signal can be driven by host I/Os under backup power domains without the risk of parasitic leakage, even if the main power to the MIC2800 is removed.

3.2 BIAS

The BIAS pin supplies the power to the internal control and reference circuitry. The bias is powered from AVIN through an internal 6 Ω resistor. A small 0.1 μ F ceramic capacitor is required for bypassing.

3.3 SGND

Signal ground (SGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be as small as possible.

3.4 PGND

Power ground (PGND) is the ground path for the high current PWM mode. The current loop for the power ground should be as small as possible.

3.5 SW

The switch (SW) pin is the common connection between the internal power MOSFETs and connects directly to the inductor. Due to the high-speed switching on this pin, the switch node should be routed away from sensitive nodes.

3.6 V_{IN}

Two input voltage pins provide power to the switch mode DC/DC and LDO2 separately. The LDO1 input voltage is provided by the DC/DC LDO pin. VIN provides power to the LDO section and the bias through an internal 6Ω resistor. Both V_{IN} pins must be tied together.

For the switch mode DC/DC regulator, VIN provides power to the MOSFET along with current limiting sensing. Due to the high switching speeds, a 4.7 μF minimum ceramic capacitor is recommended close to VIN and the power ground (PGND) pin for bypassing.

3.7 LDO2

Regulated output voltage of LDO2. Power is provided by VIN. The minimum recommended output capacitance is 2.2 μF ceramic.

3.8 FB

Connect the feedback pin to V_{OUT} for fixed output voltage versions. For adjustable output version, an external resistor divider is used to program the output voltage.

3.9 LDO

The LDO pin is the output of the LOWQ mode linear regulator and should be connected to the output of the DC/DC converter. In LOWQ mode (LOWQ < 0.2V), the LDO supplies the output current and supports the output voltage in place of the DC/DC stage. In PWM mode (LOWQ > 1V) the LDO pin provides power to LDO1.

3.10 LDO1

Regulated output voltage of LDO1. Input power is provided by the DC/DC switching regulator. The minimum recommended output capacitance is 2.2 μF ceramic.

3.11 Power-on Reset (POR)

The Power-on Reset (POR) output is an open-drain N-channel device, requiring a pull-up resistor to either the input voltage or output voltages for proper voltage levels. The POR output has a delay time that is

programmable with a capacitor from the C_{SET} pin to ground. The delay time can be programmed to be as long as 1 second.

In steady-state conditions, the POR output is high if at least one channel (LDO2 and DC-DC, LDO1) is enabled and has reached regulation. This is equivalent to performing a logic OR operation on the status of the output voltages.

If any of the outputs is subsequently pulled out of regulation (e.g., due to a momentary overload), the POR signal goes low and it remains low as long as the affected output is out of regulation. If the affected output returns in regulation, POR is asserted high after the delay time programmed with the capacitor at the C_{SET} pin.

The ESD protection of the POR pin is free from clamping diodes to the input supply rails. Therefore, the POR signal can be asserted to host I/Os under backup power domains or pulled up to backup power sources without the risk of parasitic leakage, even if the main power to the MIC2800 is removed.

3.12 C_{SET}

The C_{SET} pin is a current source output that charges a capacitor that sets the delay time for the Power-on Reset output from low-to-high. The delay for POR high-to-low (detecting an undervoltage on any of the outputs) is always minimal. The current source of 1.25 μA charges a capacitor up from 0V. When the capacitor reaches 1.25V, the output of the POR is allowed to go high. The delay time in microseconds is equal to the C_{SET} capacitor value in picofarads.

EQUATION 3-1:

$$PORDelay(\mu s) = C_{SET}(pF)$$

3.13 C_{BYP}

The internal reference voltage can be bypassed with a capacitor to ground to reduce output noise and increase power supply rejection (PSRR). A quick-start feature allows for quick turn on of the output voltage. The recommended nominal bypass capacitor is 0.1 μF, but it can be increased, which will also result in an increase to the start-up time.

3.14 EN1, EN2

Both enable inputs are active high, requiring 1.0V for guaranteed logic HIGH level detection (V_{IH}=1.0V MIN). EN1 provides logic control of both the DC/DC regulator and LDO1. EN2 provides logic control for LDO2 only. The enable inputs are CMOS logic and cannot be left floating.

The enable pins provide logic level control of the specified outputs. When both enable pins are in the OFF state, supply current of the device is greatly reduced (typically $< 1 \mu\text{A}$). When the DC/DC regulator is in the OFF state, the output drive is placed in a “tri-stated” condition, where both the high side P-channel MOSFET and the low-side N-channel are in an OFF or nonconducting state. Do not drive either of the enable pins above the supply voltage.

4.0 APPLICATION INFORMATION

The MIC2800 is a digital power management IC with a single integrated buck regulator and two low dropout regulators. LDO1 is a 300 mA low dropout regulator that uses power supplied by the onboard buck regulator. LDO2 is a 300 mA low dropout regulator using the supply from the input pin. The buck regulator is a 600 mA PWM power supply that utilizes a LOWQ light load mode to maximize battery efficiency in light load conditions. This is achieved with a LOWQ control pin that, when pulled low, shuts down all the biasing and drive current for the PWM regulator, drawing only 20 μ A of operating current. This allows the output to be regulated through the LDO output, capable of providing 60 mA of output current. This method has the advantage of producing a clean, low-current, ultra-low-noise output in LOWQ mode. During LOWQ mode, the SW node becomes high-impedance, blocking current flow. Other methods of reducing quiescent current, such as Pulse Frequency Modulation (PFM) or bursting techniques may create large-amplitude, low-frequency ripple voltages that can be detrimental to system operation.

When more than 60 mA is required, the LOWQ pin can be forced high, causing the MIC2800 to enter in PWM mode. In this case, the LDO output makes a “hand-off” to the PWM regulator with virtually no variation in output voltage. The LDO output then turns off, allowing up to 600 mA of current to be efficiently supplied through the PWM output to the load.

4.1 Output Capacitor

LDO1 and LDO2 outputs require at least a 2.2 μ F ceramic output capacitor for stability. The DC/DC switch mode regulator requires at least a 2.2 μ F ceramic output capacitor to be stable. All output capacitor values can be increased to improve transient response. X7R/X5R dielectric type ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% to 60% respectively over their operating temperature ranges and are therefore not recommended.

4.2 Input Capacitor

A minimum 1 μ F ceramic is recommended on the V_{IN} pin for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended. A minimum 1 μ F is recommended close to the V_{IN} and PGND pins for high frequency filtering. Smaller-case-size capacitors are recommended due to their lower ESR and ESL. The

value of the input capacitor can be increased as needed to better suppress the input ripple generated by the DC/DC converter.

4.3 Inductor Selection

The MIC2800 is designed for use with a 2.2 μ H inductor. Proper selection should ensure the inductor can handle the maximum average and peak currents required by the load. Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure that the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. Peak inductor current can be calculated as follows:

EQUATION 4-1:

$$I_{PK} = I_{OUT} + \frac{V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}{2 \times f \times L}$$

4.4 POR Delay Time

The POR signal also goes low for the duration of the delay time given by Eq. 3.1 when only one of the enable inputs (EN1, EN2) transitions from low to high, with the other being already high and the corresponding output being in regulation. This is shown in Fig. 2-36 and Fig. 2-37. At the low-to-high transition of either enable input, the C_{SET} pin capacitor is discharged to ground, and the POR delay time is restarted.

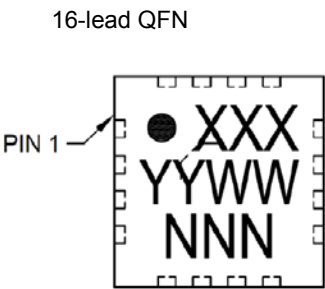
At start-up, in order to prevent a momentary high glitch of the POR signal between the first and the second enable, it is recommended to set the POR delay time longer than the maximum delay expected between the enable signals plus the turn-on time $t_{TURN-ON}$.

For a given delay between the enable signals, an example of correct POR delay time design is shown in Fig. 2-38. It can be seen that the C_{SET} voltage is reset to ground by the latter low-to-high enable transition before it reaches the $V_{TH_{CSET}}$ voltage (1.25V TYP).

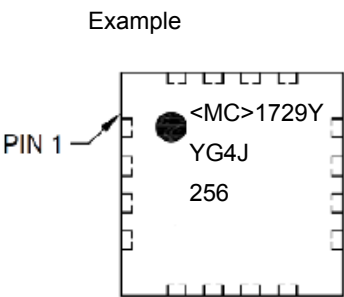
NOTES:

5.0 PACKAGING INFORMATION

5.1 Package Marking Information



Part Number	Code
MIC2800-A4SYML-TR	YA4S
MIC2800-D24MYML-TR	YD24M
MIC2800-D2FMYML-TR	YD2FM
MIC2800-G2SYML-TR	YG2S
MIC2800-G4JYML-TR	YG4J
MIC2800-G4KYML-TR	YG4K
MIC2800-G4MYML-TR	YG4M
MIC2800-G4SYML-TR	YG4S
MIC2800-G7SYML-TR	YG7S
MIC2800-G1JJYML-TR	G1JJ
MIC2800-G1JSYML-TR	G1JS
MIC2800-GFMYML-TR	YGFM
MIC2800-GFSYML-TR	YGFS
MIC2800-G4SYML-TR	YG4S



Refer to the [Product Identification System](#) section for information on the output voltage for each device.

Legend: XX...X Product code or customer-specific information
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code
(e3) Pb-free JEDEC® designator for Matte Tin (Sn)
* This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

●, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).

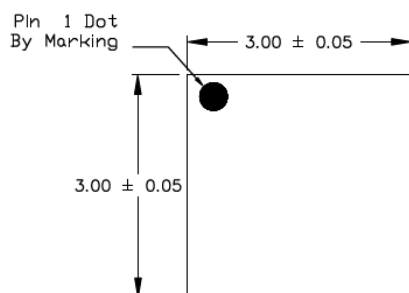
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

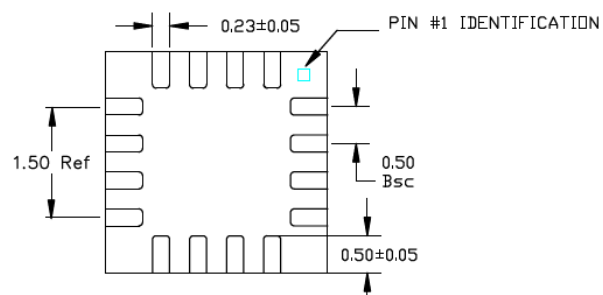
TITLE

16 LEAD QFN 3.0x3.0mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

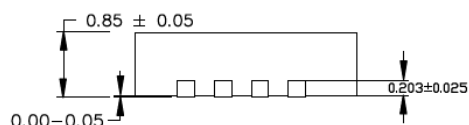
DRAWING #	CQFN33-16LD-PL-1	UNIT	MM
Lead Frame	NiPdAu	Lead Finish	NiPdAu



TOP VIEW



BOTTOM VIEW



SIDE VIEW

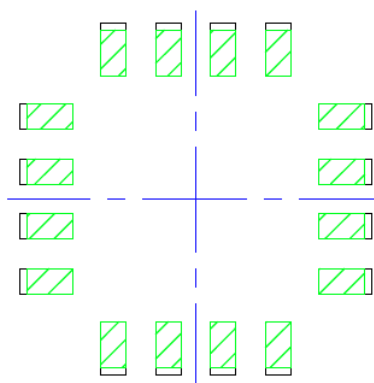
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
N IS THE TOTAL NUMBER OF TERMINALS.
2. MAX PACKAGE WARPAGE IS 0.05mm, MAX ALLOWABLE BURRS IS 0.076 mm
IN ALL DIRECTIONS.
3. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

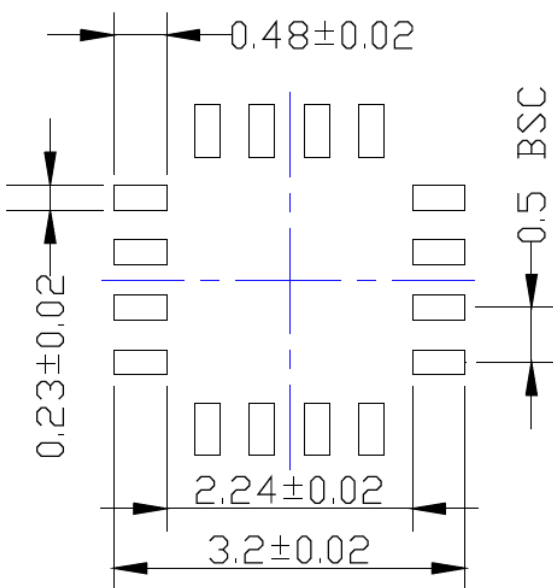
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

POD-Land Pattern drawing #CQFN33-16LD-PL-1

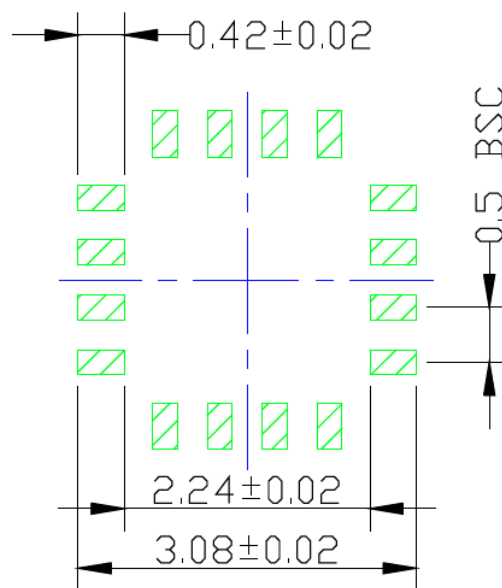
RECOMMENDED LAND PATTERN



STACKED-UP



EXPOSED METAL TRACE



SOLDER STENCIL OPENING

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2017)

Original Release of this Document.

MIC2800

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.		-	XX	X	X	-	XX ⁽¹⁾
Device			Output Voltage	Temperature	Package		Tape and Reel Option
Device:		MIC2800: Digital Power Management IC 2 MHz, 600 mA DC/DC with Dual 300 mA/300 mA Low VIN LDOs					
Output Voltages: (DC/DC, LDO1, LDO2)		A4S = Adjustable/1.2V/3.3V D24M= 1.87V/1.2V/2.8V D2FM= 1.87V/1.5V/2.8V G2S = 1.8V/1.05V/3.3V G4J = 1.8V/1.2V/2.5V G4K = 1.8V/1.2V/2.6V G4M= 1.8V/1.2V/2.8V G4S = 1.8V/1.2V/3.3V G7S = 1.8V/1.575V/3.3V G1JJ= 1.8V/1.25V/2.5V G1JS= 1.8V/1.25V/3.3V G4S = 1.8V/1.2V/3.3V					
Temperature:		Y = Pb-Free with Industrial Temperature Grade (-40°C to +125°C)					
Package:		ML = 16-lead, 3x3 mm QFN, 0.85 mm thickness					
Tape and Reel:		TR = Tape and Reel					

Examples:	
a) MIC2800-A4SYML-TR:	Digital Power Management IC 2 MHz, 600 mA DC/DC with Dual 300 mA/300 mA Low VIN LDOs, Adjustable/1.2V/3.3V Output Voltage, -40°C to +125°C, 16LD QFN Package, Tape and Reel
b) MIC2800-D24MYML-TR:	Digital Power Management IC 2 MHz, 600 mA DC/DC with Dual 300 mA/300 mA Low VIN LDOs, 1.87V/1.2V/2.8V Output Voltage, -40°C to +125°C 16LD QFN Package, Tape and Reel
c) MIC2800-D2FMYML-TR:	Digital Power Management IC 2 MHz, 600 mA DC/DC with Dual 300 mA/300 mA Low VIN LDOs, 1.87V/1.5V/2.8V Output Voltage, -40°C to +125°C 16LD QFN Package, Tape and Reel
d) MIC2800-G2SYML-TR:	Digital Power Management IC 2 MHz, 600 mA DC/DC with Dual 300 mA/300 mA Low VIN LDOs, 1.8V/1.05V/3.3V Output Voltage, -40°C to +125°C 16LD QFN Package, Tape and Reel
e) MIC2800-G4JYML-TR:	Digital Power Management IC 2 MHz, 600 mA DC/DC with Dual 300 mA/300 mA Low VIN LDOs, 1.8V/1.2V/2.5V Output Voltage, -40°C to +125°C 16LD QFN Package, Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

MIC2800

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BeaconThings, BitCloud, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Helder, JukeBlox, KEELOQ, KEELOQ logo, Klear, LANCheck, LINK MD, maxStylus, maxTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, RightTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, CryptoAuthentication, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PureSilicon, QMatrix, RightTouch logo, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2017, Microchip Technology Incorporated, All Rights Reserved.
ISBN: 978-1-5224-2210-5

Worldwide Sales and Service

AMERICAS

Corporate Office
 2355 West Chandler Blvd.
 Chandler, AZ 85224-6199
 Tel: 480-792-7200
 Fax: 480-792-7277
 Technical Support:
<http://www.microchip.com/support>
 Web Address:
www.microchip.com

Atlanta
 Duluth, GA
 Tel: 678-957-9614
 Fax: 678-957-1455

Austin, TX
 Tel: 512-257-3370

Boston
 Westborough, MA
 Tel: 774-760-0087
 Fax: 774-760-0088

Chicago
 Itasca, IL
 Tel: 630-285-0071
 Fax: 630-285-0075

Dallas
 Addison, TX
 Tel: 972-818-7423
 Fax: 972-818-2924

Detroit
 Novi, MI
 Tel: 248-848-4000

Houston, TX
 Tel: 281-894-5983

Indianapolis
 Noblesville, IN
 Tel: 317-773-8323
 Fax: 317-773-5453
 Tel: 317-536-2380

Los Angeles
 Mission Viejo, CA
 Tel: 949-462-9523
 Fax: 949-462-9608
 Tel: 951-273-7800

Raleigh, NC
 Tel: 919-844-7510

New York, NY
 Tel: 631-435-6000

San Jose, CA
 Tel: 408-735-9110
 Tel: 408-436-4270

Canada - Toronto
 Tel: 905-695-1980
 Fax: 905-695-2078

ASIA/PACIFIC

Asia Pacific Office
 Suites 3707-14, 37th Floor
 Tower 6, The Gateway
 Harbour City, Kowloon

Hong Kong
 Tel: 852-2943-5100
 Fax: 852-2401-3431

Australia - Sydney
 Tel: 61-2-9868-6733
 Fax: 61-2-9868-6755

China - Beijing
 Tel: 86-10-8569-7000
 Fax: 86-10-8528-2104

China - Chengdu
 Tel: 86-28-8665-5511
 Fax: 86-28-8665-7889

China - Chongqing
 Tel: 86-23-8980-9588
 Fax: 86-23-8980-9500

China - Dongguan
 Tel: 86-769-8702-9880

China - Guangzhou
 Tel: 86-20-8755-8029

China - Hangzhou
 Tel: 86-571-8792-8115
 Fax: 86-571-8792-8116

China - Hong Kong SAR
 Tel: 852-2943-5100
 Fax: 852-2401-3431

China - Nanjing
 Tel: 86-25-8473-2460
 Fax: 86-25-8473-2470

China - Qingdao
 Tel: 86-532-8502-7355
 Fax: 86-532-8502-7205

China - Shanghai
 Tel: 86-21-3326-8000
 Fax: 86-21-3326-8021

China - Shenyang
 Tel: 86-24-2334-2829
 Fax: 86-24-2334-2393

China - Shenzhen
 Tel: 86-755-8864-2200
 Fax: 86-755-8203-1760

China - Wuhan
 Tel: 86-27-5980-5300
 Fax: 86-27-5980-5118

China - Xian
 Tel: 86-29-8833-7252
 Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
 Tel: 86-592-2388138
 Fax: 86-592-2388130

China - Zhuhai
 Tel: 86-756-3210040
 Fax: 86-756-3210049

India - Bangalore
 Tel: 91-80-3090-4444
 Fax: 91-80-3090-4123

India - New Delhi
 Tel: 91-11-4160-8631
 Fax: 91-11-4160-8632

India - Pune
 Tel: 91-20-3019-1500

Japan - Osaka
 Tel: 81-6-6152-7160
 Fax: 81-6-6152-9310

Japan - Tokyo
 Tel: 81-3-6880-3770
 Fax: 81-3-6880-3771

Korea - Daegu
 Tel: 82-53-744-4301
 Fax: 82-53-744-4302

Korea - Seoul
 Tel: 82-2-554-7200
 Fax: 82-2-558-5932 or
 82-2-558-5934

Malaysia - Kuala Lumpur
 Tel: 60-3-6201-9857
 Fax: 60-3-6201-9859

Malaysia - Penang
 Tel: 60-4-227-8870
 Fax: 60-4-227-4068

Philippines - Manila
 Tel: 63-2-634-9065
 Fax: 63-2-634-9069

Singapore
 Tel: 65-6334-8870
 Fax: 65-6334-8850

Taiwan - Hsin Chu
 Tel: 886-3-5778-366
 Fax: 886-3-5770-955

Taiwan - Kaohsiung
 Tel: 886-7-213-7830

Taiwan - Taipei
 Tel: 886-2-2508-8600
 Fax: 886-2-2508-0102

Thailand - Bangkok
 Tel: 66-2-694-1351
 Fax: 66-2-694-1350

EUROPE

Austria - Wels
 Tel: 43-7242-2244-39
 Fax: 43-7242-2244-393

Denmark - Copenhagen
 Tel: 45-4450-2828
 Fax: 45-4485-2829

Finland - Espoo
 Tel: 358-9-4520-820

France - Paris
 Tel: 33-1-69-53-63-20
 Fax: 33-1-69-30-90-79

Germany - Garching
 Tel: 49-8931-9700

Germany - Haan
 Tel: 49-2129-3766400

Germany - Heilbronn
 Tel: 49-7131-67-3636

Germany - Karlsruhe
 Tel: 49-721-625370

Germany - Munich
 Tel: 49-89-627-144-0
 Fax: 49-89-627-144-44

Germany - Rosenheim
 Tel: 49-8031-354-560

Israel - Ra'anana
 Tel: 972-9-744-7705

Italy - Milan
 Tel: 39-0331-742611
 Fax: 39-0331-466781

Italy - Padova
 Tel: 39-049-7625286

Netherlands - Drunen
 Tel: 31-416-690399
 Fax: 31-416-690340

Norway - Trondheim
 Tel: 47-7289-7561

Poland - Warsaw
 Tel: 48-22-3325737

Romania - Bucharest
 Tel: 40-21-407-87-50

Spain - Madrid
 Tel: 34-91-708-08-90
 Fax: 34-91-708-08-91

Sweden - Gothenberg
 Tel: 46-31-704-60-40

Sweden - Stockholm
 Tel: 46-8-5090-4654

UK - Wokingham
 Tel: 44-118-921-5800
 Fax: 44-118-921-5820

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Microchip:

[MIC2800-GFSYML TR](#) [MIC2800-D2FMYML TR](#) [MIC2800-D24MYML TR](#) [MIC2800-G4JYML TR](#) [MIC2800-G4MYML TR](#) [MIC2800-G4KYML TR](#) [MIC2800-GFMYML TR](#) [MIC2800-A4SYML TR](#) [MIC2800-G7SYML TR](#) [MIC2800-G4SYML TR](#) [MIC2800-D24MYML-TR](#) [MIC2800-GFSYML-TR](#) [MIC2800-G4MYML-TR](#) [MIC2800-GFMYML-TR](#) [MIC2800-A4SYML-TR](#) [MIC2800-G4KYML-TR](#) [MIC2800-G4JYML-TR](#) [MIC2800-D2FMYML-TR](#) [MIC2800-G4SYML-TR](#) [MIC2800-G7SYML-TR](#) [MIC2800-G2SYML-TR](#) [MIC2800-G8SYML-TR](#) [MIC2800-G1JSYML-TR](#) [MIC2800-G1JJYML-TR](#)

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9