

LI-OV8865-MIPI-AF SPECIFICATION

**Rev 1.0
Leopard Imaging Inc.**

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Version History

Version	Description	Release Date
1.0	First Release	31. Dec. 2014



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Key Information

Module Part#		LI-OV8865-MIPI-AF
Module Size		27.75 mm (L) x 8.50 mm (W) x 5.60 mm(H)
Sensor Type		OV8865
Array Size		3264 x 2448
Power Supply	core	1.2V
	analog	2.8V
	I/O	1.8V , 2.8V
Lens Size		1/3.2"
Focus(F.NO)		2.2
FOV (D)		70°
Focal Length		3.85 mm
Focusing Range		10cm to infinity
TV Distortion		< 1.5 %
Sensitivity		940 mV/ Lux-sec
Pixel size		1.4 um x 1.4 um
IR Cutter		650 nm
Sensor Temperature Range	Operating	-30 ℃ to +85 ℃
	Stable Image	0 ℃ to +60 ℃
Output Formats		10-bit RAW RGB data
Maximum Image Transfer Rate		3264 x 2448: 30 fps; 3264 x 1836: 30 fps; 2816 x 1584: 30 fps; 1632 x 1224: 30 fps; 1408 x 792: 60 fps;
Dynamic Range		68.8 dB
Max S/N ratio		36.7 dB
Scan mode		Progressive
Power Requirement	Active	196 mW (Full resolution @ 30 fps)
	XSHUTDOWN	5 uW
Image area		4614.4 um x 3472 um
Dark Current		20 e ⁻ /sec @ 60 ℃ junction temperature
Die Dimensions		5850um x 5700um (COB), 5900 um x 5750um (RW)



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Pin Assignment

No.	Name	Pin type	Description
1	SDA	I/O	SCCB data
2	SCL	Input	SCCB input clock
3	DOVDD1.8V/2.8V	Power	Power for I/O circuit
4	MCP	Output	MIPI clock positive output
5	MCN	Output	MIPI clock negative output
6	GND	Ground	
7	MDP1	Output	MIPI data positive output
8	MDN1	Output	MIPI data negative output
9	GND	Ground	
10	MDP2	Output	MIPI data positive output
11	MDN2	Output	MIPI data negative output
12	GND	Ground	
13	MDP3	Output	MIPI data positive output
14	MDN3	Output	MIPI data negative output
15	GND	Ground	
16	MDP4	Output	MIPI data positive output
17	MDN4	Output	MIPI data negative output
18	DVDD1.2V	Power	Power for digital core
19	XCLK	Input	System input clock
20	PWDN	Input	Power down (active high with internal pull-down resistor)
21	RESET	Input	Reset (active low with internal pull-up resistor)
22	AVDD2.8	Power	Analog power
23	AF-VCC2.8V	Power	Power for analog circuit
24	AF-AGND	Ground	Ground for analog circuit



Electrical Characteristics

1. Absolute Maximum Ratings

parameter		absolute maximum rating ^a
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V _{DD-A}	4.5V
	V _{DD-D}	3V
	V _{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V _{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2. Functional temperature

parameter	range
operating temperature (for applications up to 90 fps) ^a	-30°C to +85°C junction temperature
stable image temperature ^b	0°C to +60°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range



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3. DC Characteristics (-30 °C < T_J < 85 °C)

symbol	parameter	min	typ	max ^a	unit
supply					
V _{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V _{DD-D}	supply voltage (digital core for 4-lane MIPI up to 1000 Mbps/lane)	1.1	1.2	1.3	V
V _{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.0	V
I _{DD-A}	active (operating) current ^b		23	30	mA
I _{DD-IO}			3.3	4.5	mA
I _{DD-CORE}			105	125	mA
I _{DDS-SCCB}			300	3000	μA
I _{DDS-PWDN}	standby current ^c		300	3000	μA
I _{DDS-XSHUTDOWN}			6	30	μA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.2V, DOVDD = 1.8V)					
V _{IL}	input voltage LOW			0.54	V
V _{IH}	input voltage HIGH	1.26			V
C _{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V _{OH}	output voltage HIGH	1.62			V
V _{OL}	output voltage LOW			0.18	V
serial interface inputs					
V _{IL} ^d	SIOC and SIOD	-0.5	0	0.54	V
V _{IH}	SIOC and SIOD	1.28	1.8	3.0	V

- a. maximum active current is measured under typical supply voltage
- b. operating current is measured at full size and 30 fps with all sensor functions on and DOVDD = 1.8V and EVDD tied to DVDD
- c. standby current is measured at room temperature with external clock off
- d. based on DOVDD = 1.8V



4. Timing Characteristics

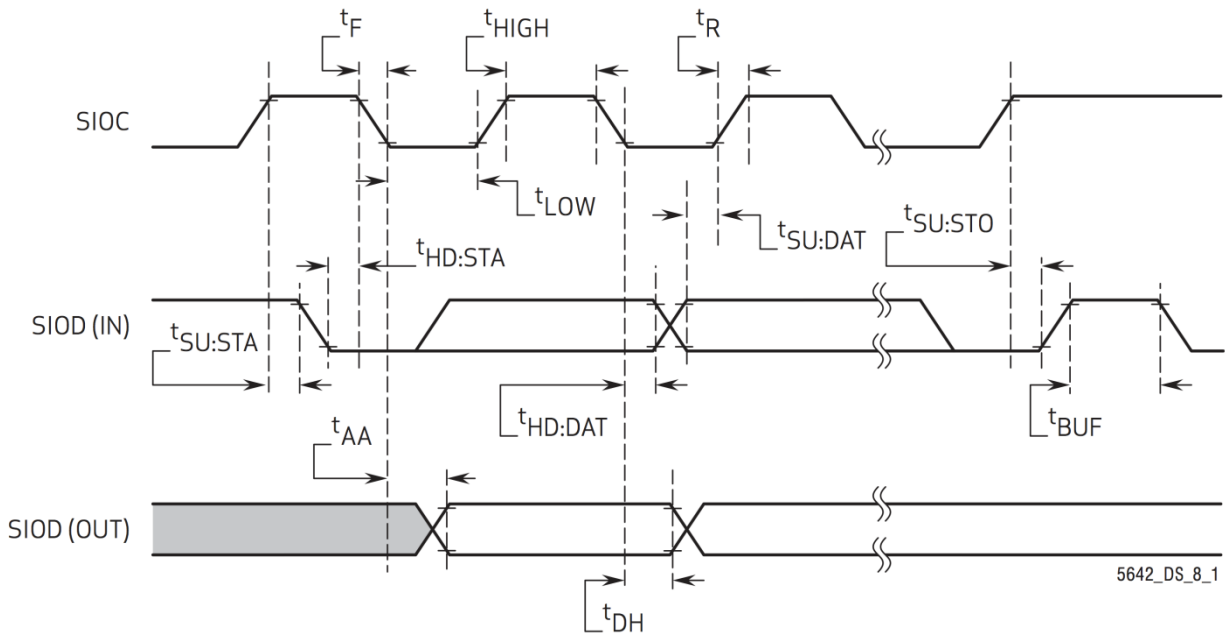
symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (EXTCLK) ^a	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5 (10 ^b)	ns
	clock input duty cycle	45	50	55	%

a. for input clock range 6~27MHz, the OV8865 can tolerate input clock period jitter up to 600ps peak-to-peak

b. if using internal PLL

5. SCCB timing

a. SCCB interface timing



5642_DS_8_1

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b. SCCB interface timing Specification^{ab}

symbol	parameter	min	typ	max	unit
f _{SIOC}	clock frequency			400	kHz
t _{LOW}	clock low period	1.3			μs
t _{HIGH}	clock high period	0.6			μs
t _{AA}	SIOC low to data out valid	0.1		0.9	μs
t _{BUF}	bus free time before new start	1.3			μs
t _{HD:STA}	start condition hold time	0.6			μs
t _{SU:STA}	start condition setup time	0.6			μs
t _{HD:DAT}	data in hold time	0			μs
t _{SU:DAT}	data in setup time	0.1			μs
t _{SU:STO}	stop condition setup time	0.6			μs
t _R , t _F	SCCB rise/fall times			0.3	μs
t _{DH}	data out hold time	0.05			μs

- a. SCCB timing is based on 400kHz mode
- b. timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 30%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 70%

6. Format and frame rate

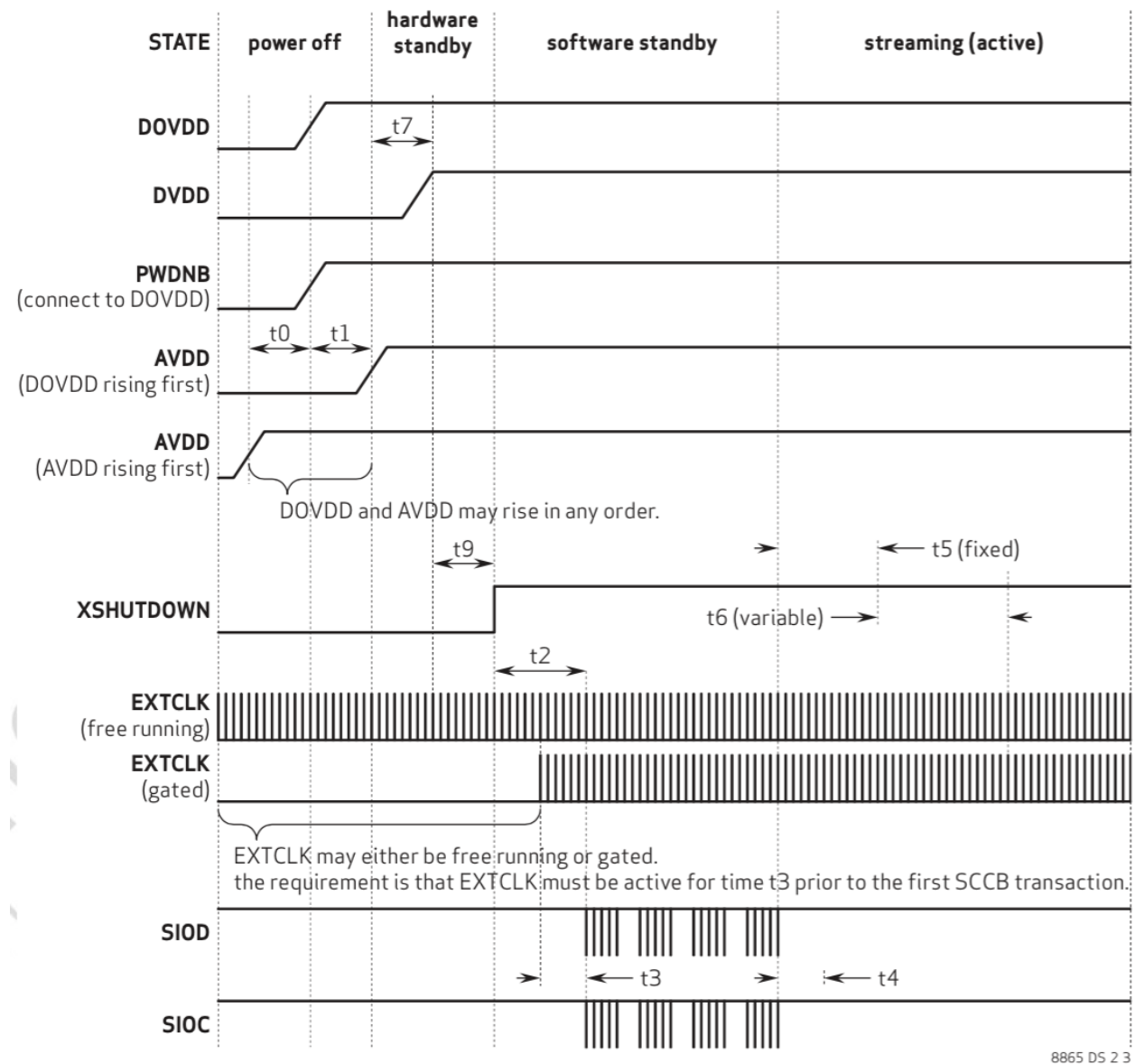
resolution	10-bit output	methodology	10-bit output MIPI data rate
3264x2448	30 fps	full	4-lane @ 720 Mbps/lane
3264x2448	30 fps	full	2-lane @ 1.23 Gbps/lane
3264x1836	30 fps	cropping	4-lane @ 720 Mbps/lane
2816x1584	30 fps	cropping	2-lane @ 720 Mbps/lane
1632x1224	30 fps	2x2 fast binning	2-lane @ 672 Mbps/lane
1408x792	60 fps	2x2 fast binning	2-lane @ 384 Mbps/lane



7. Power Up Sequence

case	XSHUTDOWN	PWDNB	power up sequence requirement
1	GPIO	DOVDD	Refer to figure 2-3 1. DOVDD rising must occur before DVDD rising 2. AVDD rising can occur before or after DOVDD rising 3. AVDD must occur before DVDD 4. XSHUTDOWN rising must occur after AVDD, DOVDD and DVDD are stable
2	DOVDD	GPIO	Refer to figure 2-4 1. AVDD rising occurs before DOVDD rising 2. DOVDD rising occurs before DVDD 3. PWDNB rising occurs after DVDD rising

a. Power Up Sequence (case 1)



8865_DS_2_3

Figure 2-3



b. Power Up Sequence (case 2)

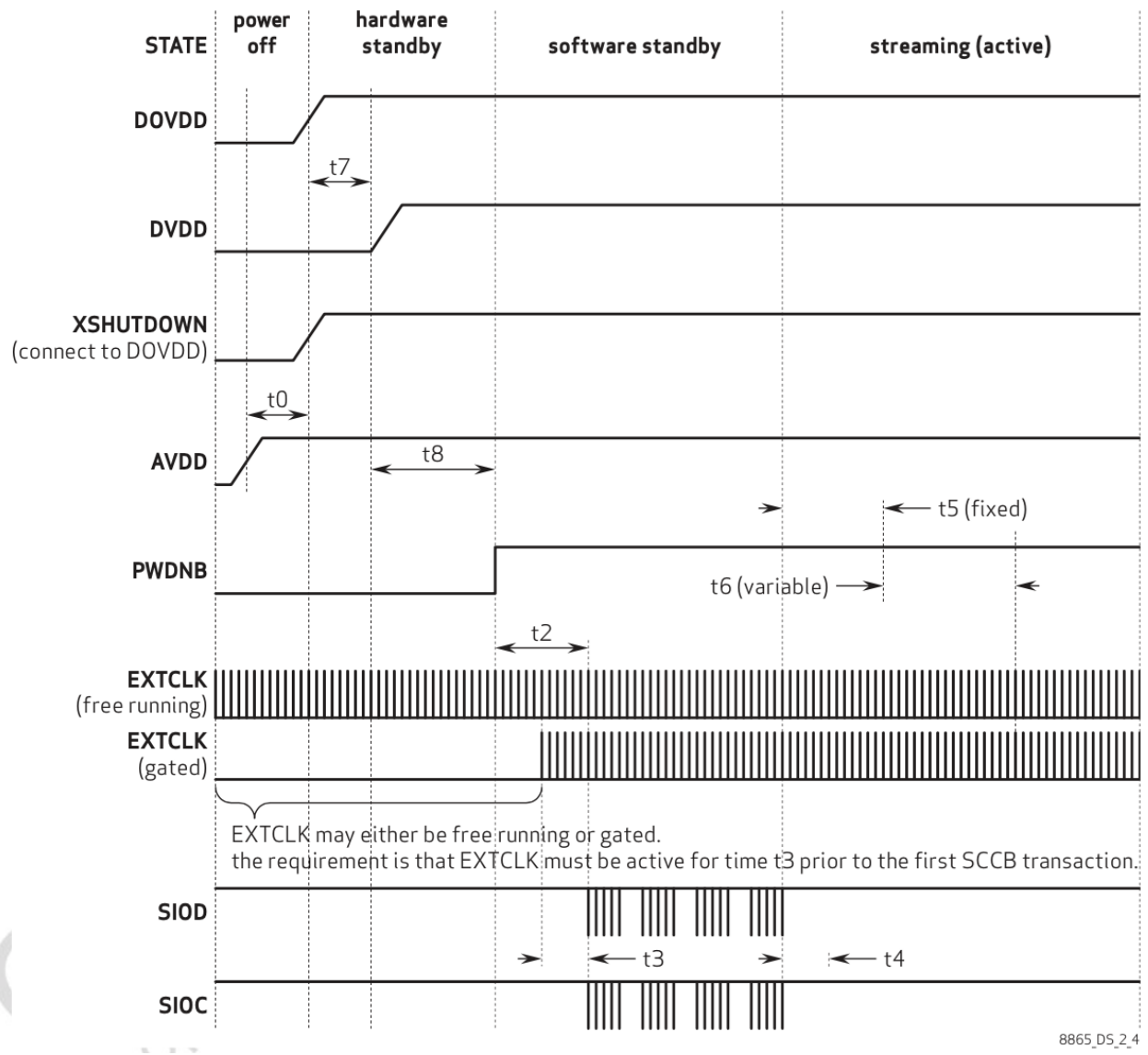


Figure 2-4

c. Power Up Sequence Timing Constraints

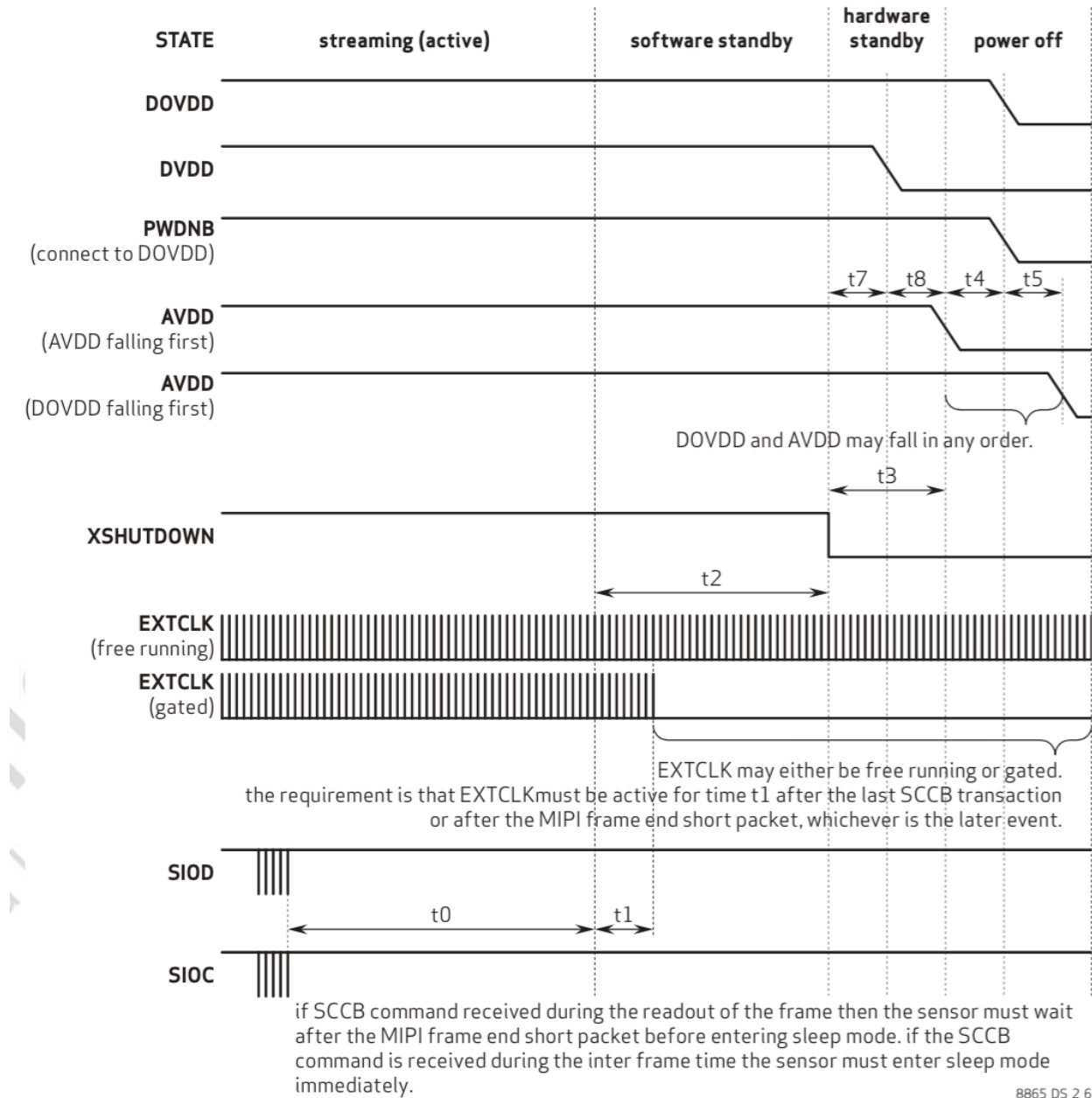
constraint	label	min	max	unit
AVDD rising – DOVDD rising	t0	0	∞	ns
DOVDD rising – AVDD rising	t1			ns
XSHUTDOWN rising – first SCCB transaction	t2	8192		EXTCLK cycles
minimum number of EXTCLK cycles prior to the first SCCB transaction	t3	8192		EXTCLK cycles
PLL start up/lock time	t4		0.2	ms
entering streaming mode – first frame start sequence (fixed part)	t5		10	ms
entering streaming mode – first frame start sequence (variable part)	t6	delay is the exposure time value		lines
AVDD or DOVDD, whichever is last – DVDD	t7	0	∞	ns
DVDD – PWDNB rising	t8	0	∞	ns
DVDD – XSHUTDOWN rising	t9	0	∞	ns

8. Power Down Sequence

case	XSHUTDOWN	PWDNB	power down sequence requirement
1	GPIO	DOVDD	Refer to figure 2-6 1. software standby recommended 2. pull XSHUTDOWN low for minimum power consumption 3. cut off DVDD 4. pull AVDD and DOVDD low in any order
2	DOVDD	GPIO	Refer to figure 2-7 1. software standby recommended 2. pull PWDNB low for minimum power consumption 3. cut off DVDD 4. pull DOVDD low (XSHUTDOWN connected to DOVDD) 5. pull AVDD low

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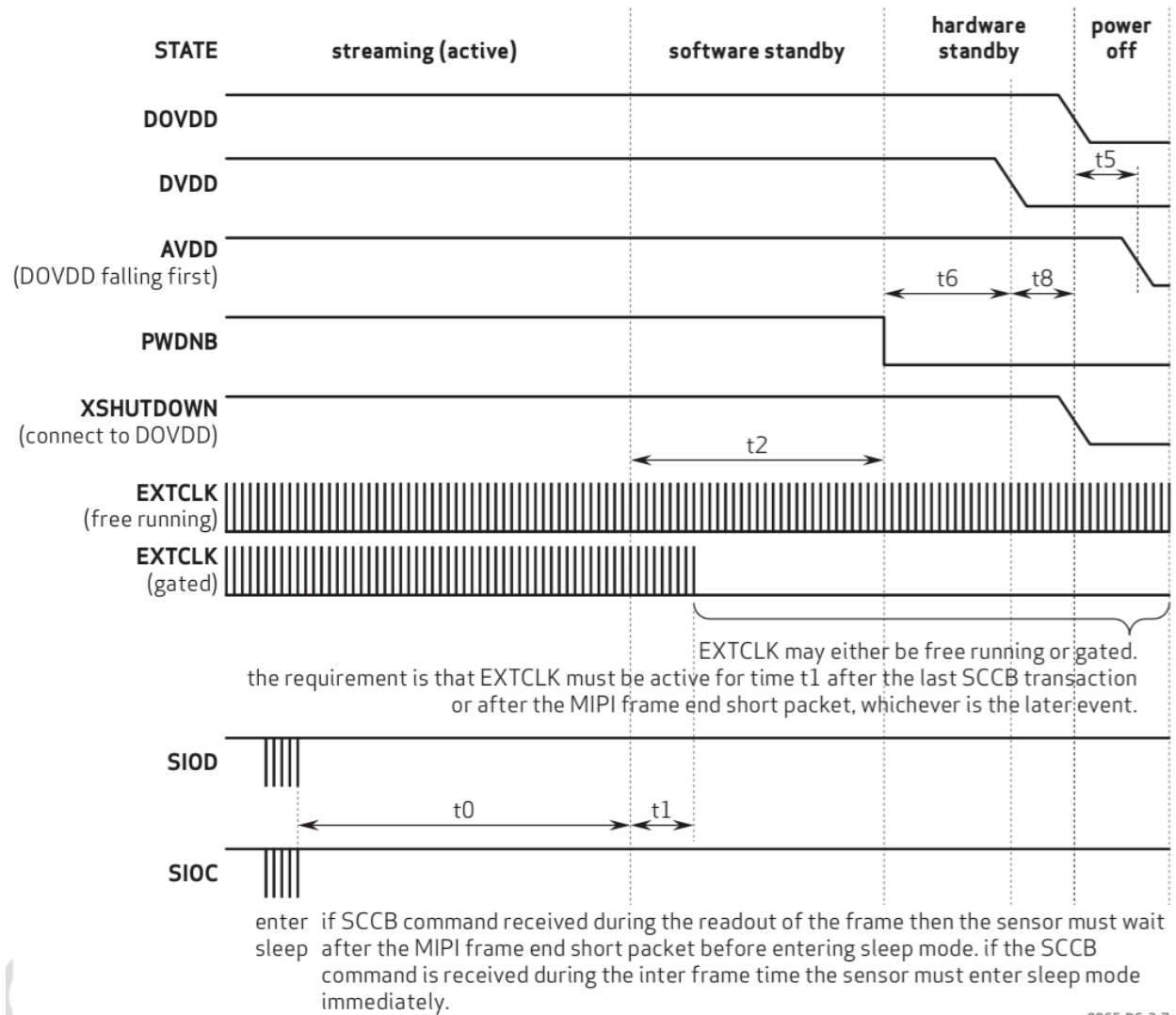
a. Power Down Sequence (case 1)



8865_DS_2_6

Figure 2-6

b. Power Down Sequence (case 2)



8865_DS_2_7

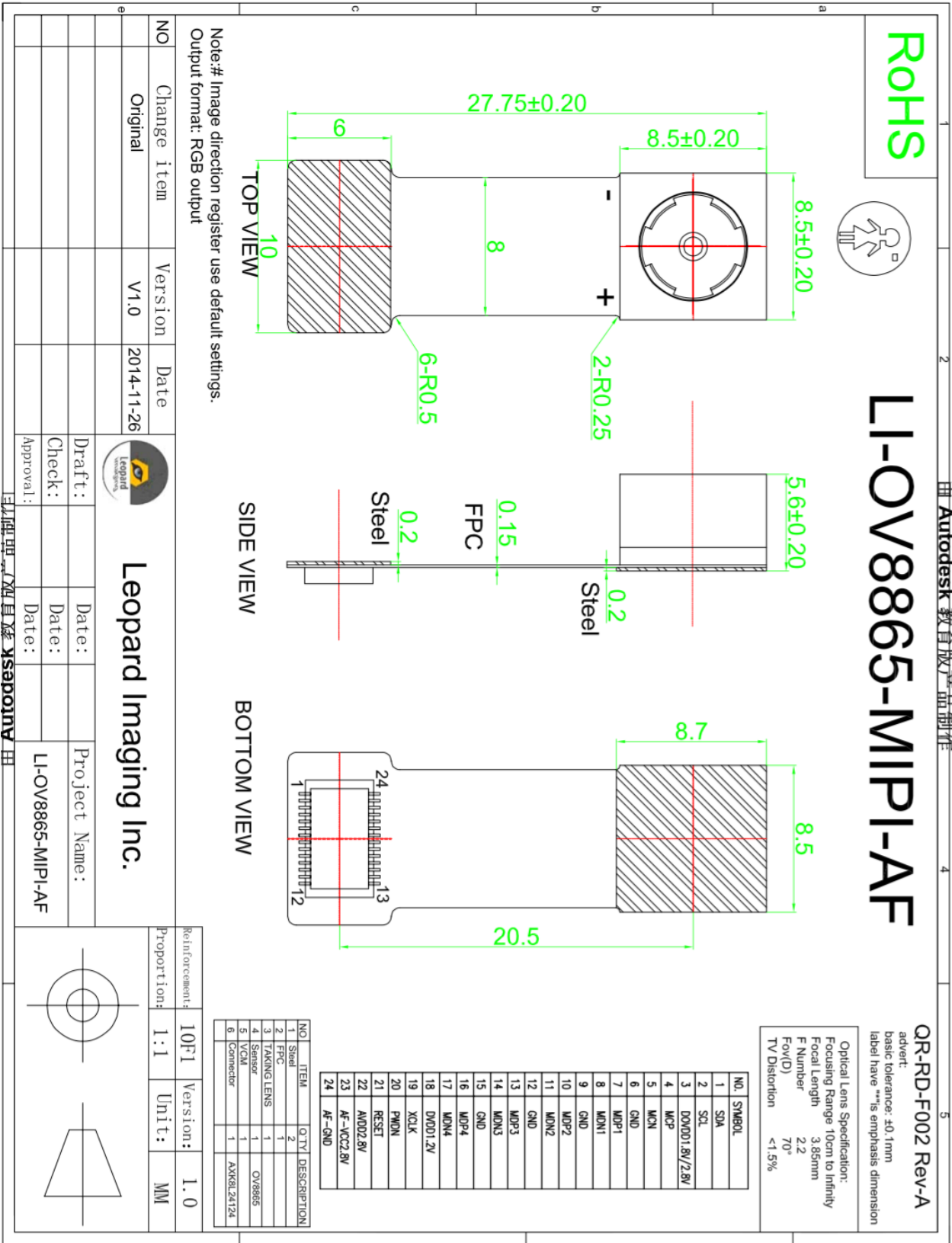
Figure 2-7

c. Power Down Sequence Timing Constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of MIPI data is output, wait for the MIPI end code before entering the software for standby; otherwise, enter the software standby mode immediately		
minimum of EXTCLK cycles after the last SCCB transaction or MIPI frame end	t1	512		EXTCLK cycles
last SCCB transaction or MIPI frame end, XSHUTDOWN falling	t2	512		EXTCLK cycles
XSHUTDOWN falling – AVDD falling or DOVDD falling whichever is first	t3	0.0		ns
AVDD falling – DOVDD falling	t4	AVDD and DOVDD may fall in any order, the falling separation can vary from 0 ns to infinity		ns
DOVDD falling – AVDD falling	t5			ns
PWDNB falling – DOVDD falling	t6	0.0		ns
XSHUTDOWN falling – DVDD falling	t7	0.0		ns
DVDD falling – AVDD falling or DOVDD falling whichever is first	t8	0.0		ns
PWDNB falling – DVDD falling	t9	0.0		ns



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