Low Noise, High Throughput 24-Bit Sigma-Delta ADC

AD7731

FEATURES
24-Bit Sigma-Delta ADC
16 Bits p-p Resolution at 800 Hz Output Rate
Programmable Output Rates up to 6.4 kHz
Programmable Gain Front End
±0.0015% Nonlinearity
Buffered Differential Inputs
Programmable Filter Cutoffs
***FAST*Step™* Mode for Channel Sequencing**
Single Supply Operation

APPLICATIONS
Process Control
PLCs/DCS
Industrial Instrumentation

GENERAL DESCRIPTION

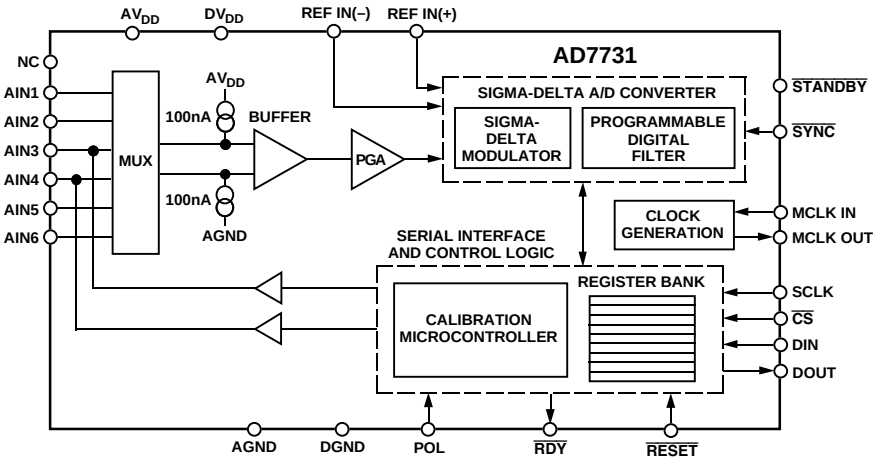
The AD7731 is a complete analog front-end for process control applications. The device has a proprietary programmable gain front end that allows it to accept a range of input signal ranges, including low level signals, directly from a transducer. The sigma-delta architecture of the part consists of an analog modulator and a low pass programmable digital filter, allowing adjustment of filter cutoff, output rate and settling time.

The part features three buffered differential programmable gain analog inputs (which can be configured as five pseudo-differential inputs), as well as a differential reference input. The part operates from a single +5 V supply and accepts seven unipolar analog input ranges: 0 to +20 mV, +40 mV, +80 mV, +160 mV, +320 mV, +640 mV and +1.28 V, and seven bipolar ranges: ±20 mV, ±40 mV, ±80 mV, ±160 mV, ±320 mV, ±640 mV and ±1.28 V. The peak-to-peak resolution achievable directly from the part is 16 bits at an 800 Hz output rate. The part can switch between channels with 1 ms settling time and maintain a performance level of 13 bits of peak-to-peak resolution.

The serial interface on the part can be configured for three-wire operation and is compatible with microcontrollers and digital signal processors. The AD7731 contains self-calibration and system calibration options and features an offset drift of less than 5 nV/°C and a gain drift of less than 2 ppm/°C.

The part is available in a 24-lead plastic DIP, a 24-lead SOIC and 24-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAM



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REV. A

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AD7731–SPECIFICATIONS (AV_{DD} = +5 V, DV_{DD} = +3 V or +5 V; REF IN(+) = +2.5 V; REF IN(–) = AGND; AGND = DGND = 0 V; $f_{CLK\ IN}$ = 4.9152 MHz. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version[1]	Units	Conditions/Comments
STATIC PERFORMANCE (CHP = 0)			
No Missing Codes[2]	24	Bits min	SKIP = 0[3]
Output Noise and Update Rates[2]	See Tables I and II		
Integral Nonlinearity	15	ppm of FSR max	
Offset Error[2]	See Note 4		Offset Error and Offset Drift Refer to Both
Offset Drift vs. Temperature[2]	0.5	µV/°C typ	Input Range = 20 mV, 40 mV, 80 mV, 160 mV
	1/2/5	µV/°C typ	Input Range = 320 mV/640 mV/1.28 V
Offset Drift vs. Time[5]	2.5	µV/1000 Hr	
Positive Full-Scale Error[2, 6]	See Note 4		
Positive Full-Scale Drift vs. Temp[2, 7, 8]	0.6	µV/°C typ	Input Range = 20 mV, 40 mV, 80 mV, 160 mV
	1.5/3/6	µV/°C typ	Input Range = 320 mV/640 mV/1.28 V
Positive Full-Scale Drift vs. Time[5]	3	µV/1000 Hr	
Gain Error[2, 9]	See Note 4		
Gain Drift vs. Temperature[2, 7, 10]	2	ppm/°C typ	
Gain Drift vs. Time[5]	10	ppm/1000 Hr	
Bipolar Negative Full-Scale Error[2]	See Note 4		
Negative Full-Scale Drift vs. Temp[2, 7]	1	µV/°C typ	
Power Supply Rejection[11]	90	dB typ	Input Range = 20 mV
Power Supply Rejection[11]	60	dB typ	Input Range = 1.28 V
Common-Mode Rejection (CMR)[11]			
On AIN	95	dB typ	At DC. Input Range = 20 mV
On AIN	85	dB typ	At DC. Input Range = 1.28 V
On REF IN	120	dB typ	
Analog Input DC Bias Current[2]	60	nA max	
Analog Input DC Bias Current Drift[2]	150	pA/°C typ	
Analog Input DC Offset Current[2]	30	nA max	
Analog Input DC Offset Current Drift[2]	100	pA/°C typ	
STATIC PERFORMANCE (CHP = 1)[2]			
No Missing Codes	24	Bits min	
Output Noise and Update Rates	See Tables III and IV		
Integral Nonlinearity	15	ppm of FSR max	
Offset Error	See Note 4		Offset Error and Offset Drift Refer to Both
Offset Drift vs. Temperature	5	nV/°C typ	Unipolar Offset and Bipolar Zero Errors
Offset Drift vs. Time[5]	25	nV/1000 Hr typ	
Positive Full-Scale Error[6]	See Note 4		
Positive Full-Scale Drift vs. Temp[7, 8]	2	ppm of FS/°C max	
Positive Full-Scale Drift vs. Time[5]	10	ppm of FS/1000 Hr	
Gain Error[9]	See Note 4		
Gain Drift vs. Temperature[7, 10]	2	ppm/°C max	
Gain Drift vs. Time[5]	10	ppm/1000 Hr	
Bipolar Negative Full-Scale Error	See Note 4		
Negative Full-Scale Drift vs. Temp	2	ppm of FS/°C max	
Power Supply Rejection[11]	110	dB typ	Input Range = 20 mV
Power Supply Rejection[11]	85	dB typ	Input Range = 1.28 V
Common-Mode Rejection (CMR)[11]			
On AIN	110	dB typ	At DC. Input Range = 20 mV
On AIN	85	dB typ	At DC. Input Range = 1.28 V
On REF IN	120	dB typ	
Analog Input DC Bias Current	50	nA max	
Analog Input DC Bias Current Drift	100	pA/°C typ	
Analog Input DC Offset Current	10	nA max	
Analog Input DC Offset Current Drift	50	pA/°C typ	
ANALOG INPUTS/REFERENCE INPUTS			
Normal Mode 50 Hz/60 Hz Rejection[2]	88	dB min	50 Hz/60 Hz ±1 Hz. SKIP = 0
Common-Mode 50 Hz/60 Hz Rejection[2]	120	dB min	50 Hz/60 Hz ±1 Hz. SKIP = 0
Analog Inputs			
Differential Input Voltage Ranges[12]			Assuming 2.5 V or 5 V Reference with HIREF Bit Set Appropriately
	0 to +20 or ±20	mV nom	RN2, RN1, RN0 of Mode Register = 0, 0, 1
	0 to +40 or ±40	mV nom	RN2, RN1, RN0 of Mode Register = 0, 1, 0
	0 to +80 or ±80	mV nom	RN2, RN1, RN0 of Mode Register = 0, 1, 1
	0 to +160 or ±160	mV nom	RN2, RN1, RN0 of Mode Register = 1, 0, 0
	0 to +320 or ±320	mV nom	RN2, RN1, RN0 of Mode Register = 1, 0, 1
	0 to +640 or ±640	mV nom	RN2, RN1, RN0 of Mode Register = 1, 1, 0
	0 to +1.28 or ±1.28	V nom	RN2, RN1, RN0 of Mode Register = 1, 1, 1

Parameter	B Version[1]	Units	Conditions/Comments
Absolute/Common-Mode Voltage[13]	AGND + 1.2 V	V min	
	AV_{DD} – 0.95 V	V max	
Reference Input			
REF IN(+) – REF IN (–) Voltage	+2.5	V nom	HIREF Bit of Mode Register = 0
REF IN(+) – REF IN (–) Voltage	+5	V nom	HIREF Bit of Mode Register = 1
Reference DC Input Current	5.5	µA max	HIREF Bit of Mode Register = 0
Reference DC Input Current	10	µA max	HIREF Bit of Mode Register = 1
Absolute/Common-Mode Voltage[14]	AGND – 30 mV	V min	
	AV_{DD} + 30 mV	V max	
NO REF Trigger Voltage	0.3	V min	NO REF Bit Active If VREF Below This Voltage
	0.65	V max	NO REF Bit Inactive If VREF Above This Voltage
LOGIC INPUTS			
Input Current	±10	µA max	
All Inputs Except SCLK and MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = +5 V
V_{INL}, Input Low Voltage	0.4	V max	DV_{DD} = +3 V
V_{INH}, Input High Voltage	2.0	V min	
SCLK Only (Schmitt Triggered Input)			
V_{T+}	1.4/3	V min/V max	DV_{DD} = +5 V
V_{T+}	0.95/2.5	V min/V max	DV_{DD} = +3 V
V_{T-}	0.8/1.4	V min/V max	DV_{DD} = +5 V
V_{T-}	0.4/1.1	V min/V max	DV_{DD} = +3 V
$V_{T+} - V_{T-}$	0.4/0.85	V min/V max	DV_{DD} = +5 V
$V_{T+} - V_{T-}$	0.4/0.8	V min/V max	DV_{DD} = +3 V
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = +5 V
V_{INL}, Input Low Voltage	0.4	V max	DV_{DD} = +3 V
V_{INH}, Input High Voltage	3.5	V min	DV_{DD} = +5 V
V_{INH}, Input High Voltage	2.5	V min	DV_{DD} = +3 V
LOGIC OUTPUTS (Including MCLK OUT)			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 800 µA Except for MCLK OUT[15]. V_{DD}[16] = +5 V
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 100 µA Except for MCLK OUT[15]. V_{DD}[16] = +3 V
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 200 µA Except for MCLK OUT[15]. V_{DD}[16] = +5 V
V_{OH}, Output High Voltage	DV_{DD} – 0.6 V	V min	I_{SOURCE} = 100 µA Except for MCLK OUT[15]. V_{DD}[16] = +3 V
Floating State Leakage Current	±10	µA max	
Floating State Output Capacitance[3]	6	pF typ	
TRANSDUCER BURNOUT[17]			
AIN1(+) Current	–100	nA nom	
AIN1(–) Current	100	nA nom	
Initial Tolerance @ 25°C	±10	% typ	
Drift	0.1	%/°C typ	
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit[18]	1.05 × FS	V max	FS Is the Nominal Full-Scale Voltage (20 mV, 40 mV, 80 mV, 160 mV, 320 mV, 640 mV, 1.28 V)
Negative Full-Scale Calibration Limit[18]	–1.05 × FS	V max	
Offset Calibration Limit[19]	–1.05 × FS	V min	
Input Span[19]	0.8 × FS	V min	
	2.1 × FS	V max	
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} – AGND Voltage	+5	V nom	
DV_{DD} Voltage	+2.7 to +5.25	V min to V max	With AGND = 0 V
Power Supply Currents			External MCLK. Digital I/Ps = 0 V or DV_{DD}
AV_{DD} Current (Normal Mode)	10.3	mA max	
DV_{DD} Current (Normal Mode)	1.7	mA max	DV_{DD} of 2.7 V to 3.3 V
DV_{DD} Current (Normal Mode)	3.2	mA max	DV_{DD} of 4.75 V to 5.25 V
AV_{DD} + DV_{DD} Current (Standby Mode)	25	µA max	Typically 10 µA. External MCLK IN = 0 V or DV_{DD}
Power Dissipation			AV_{DD} = DV_{DD} = +5 V. Digital I/Ps = 0 V or DV_{DD}
Normal Mode	67.5	mW max	
Standby Mode	125	µW max	Typically 50 µW. External MCLK IN = 0 V or DV_{DD}

NOTES
[1] Temperature Range: –40°C to +85°C.
[2] Sample tested during initial release.
[3] No missing codes performance with CHP = 0 and SKIP = 1 is 22 bits.
[4] The offset (or zero) numbers with CHP = 0 can be up to 1 mV precalibration. Internal zero-scale calibration reduces this to 2 µV typical. Offset numbers with CHP = 1 are typically 3 µV precalibration. Internal zero-scale calibration reduces this by about 1 µV. System zero-scale calibration reduces offset numbers with CHP = 0 and CHP = 1 to the order of the noise. Gain errors can be up to 3000 ppm precalibration with CHP = 0 and CHP = 1. Performing internal full-scale calibrations on all input ranges except the 20 mV and 40 mV input range reduces the gain error to less than 100 ppm. When operating on the 20 mV or 40 mV range, an internal full-scale calibration should be performed on the 80 mV input range with a resulting gain error of less than 250 ppm. System full-scale calibration reduces the gain error on all input ranges to the order of the noise. Positive and Negative Full-Scale Errors can be calculated from the offset and gain errors.
[5] These numbers are generated during life testing of the part.
[6] Positive Full-Scale Error includes Zero-Scale Errors (Unipolar Offset Error or Bipolar Zero Error) and applies to both unipolar and bipolar input ranges. See Terminology.
[7] Recalibration at any temperature will remove these errors.
[8] Full-scale drift includes Zero-Scale Drift (Unipolar Offset Drift or Bipolar Zero Drift) and applies to both unipolar and bipolar input ranges.
[9] Gain Error is a measure of the difference between the measured and the ideal span between any two points in the transfer function. The two points use to calculate the gain error are positive full-scale and negative full-scale. See Terminology.
[10] Gain Error Drift is a span drift and is effectively the drift of the part if zero-scale calibrations only were performed.
[11] Power Supply Rejection and Common-Mode Rejection are given here for the upper and lower input voltage ranges. The rejection can be approximated to varying linearly (in dBs) between these values for the other input ranges.
[12] The analog input voltage range on the AIN(+) inputs is given here with respect to the voltage on the respective AIN(–) input.
[13] The common-mode voltage range on the input pairs applies provided the absolute input voltage specification is obeyed.
[14] The common-mode voltage range on the reference input pair (REF IN(+) and REF IN(–)) applies provided the absolute input voltage specification is obeyed.
[15] These logic output levels apply to the MCLK OUT output only when it is loaded with a single CMOS load.
[16] V_{DD} refers to DV_{DD} for all logic outputs expect D0 and D1 where it refers to AV_{DD}. In other words, the output logic high for these two outputs is determined by AV_{DD}.
[17] See Burnout Current section.
[18] After calibration, if the input voltage exceeds positive full scale, the converter will output all 1s. If the input is less than negative full scale, then the device outputs all 0s.
[19] These calibration and span limits apply provided the absolute input voltage specification is obeyed. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2]

(AV_{DD} = +4.75 V to +5.25 V; DV_{DD} = +2.7 V to +5.25 V; AGND = DGND = 0 V; $f_{CLK\ IN}$ = 4.9152 MHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD} unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
Master Clock Range	1	MHz min	For Specified Performance
	5	MHz max	
t_1	50	ns min	$\overline{SYNC}$ Pulse Width
t_2	50	ns min	$\overline{RESET}$ Pulse Width
Read Operation			
t_3	0	ns min	$\overline{RDY}$ to $\overline{CS}$ Setup Time
t_4	0	ns min	$\overline{CS}$ Falling Edge to SCLK Active Edge Setup Time[3]
t_5[4]	0	ns min	SCLK Active Edge to Data Valid Delay[3]
	60	ns max	DV_{DD} = +4.75 V to +5.25 V
	80	ns max	DV_{DD} = +2.7 V to +3.3 V
t_{5A}[4, 5]	0	ns min	$\overline{CS}$ Falling Edge to Data Valid Delay[3]
	60	ns max	DV_{DD} = +4.75 V to +5.25 V
	80	ns max	DV_{DD} = +2.7 V to +3.3 V
t_6	100	ns min	SCLK High Pulse Width
t_7	100	ns min	SCLK Low Pulse Width
t_8	0	ns min	$\overline{CS}$ Rising Edge to SCLK Inactive Edge Hold Time[3]
t_9[6]	10	ns min	Bus Relinquish Time after SCLK Inactive Edge[3]
	80	ns max	
t_{10}	100	ns max	SCLK Active Edge to $\overline{RDY}$ High[3, 7]
Write Operation			
t_{11}	0	ns min	$\overline{CS}$ Falling Edge to SCLK Active Edge Setup Time[3]
t_{12}	30	ns min	Data Valid to SCLK Edge Setup Time
t_{13}	25	ns min	Data Valid to SCLK Edge Hold Time
t_{14}	100	ns min	SCLK High Pulse Width
t_{15}	100	ns min	SCLK Low Pulse Width
t_{16}	0	ns min	$\overline{CS}$ Rising Edge to SCLK Edge Hold Time

NOTES
[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.
[2] See Figures 15 and 16.
[3] SCLK active edge is falling edge of SCLK with POL = 1; SCLK active edge is rising edge of SCLK with POL = 0.
[4] These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[5] This specification only comes into play if $\overline{CS}$ goes low while SCLK is low (POL = 1) or if $\overline{CS}$ goes low while SCLK is high (POL = 0). It is required primarily for interfacing to DSP machines.
[6] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.
[7] $\overline{RDY}$ returns high after the first read from the device after an output update. The same data can be read again, if required, while $\overline{RDY}$ is high, although care should be taken that subsequent reads do not occur close to the next output update.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
AV_{DD} to DGND ..... –0.3 V to +7 V
DV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
AGND to DGND ..... –5 V to +0.3 V
AV_{DD} to DV_{DD} ..... –2 V to +5 V
Analog Input Voltage to AGND ..... –0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND ..... –0.3 V to AV_{DD} + 0.3 V
AIN/REF IN Current (Indefinite) ..... 30 mA
Digital Input Voltage to DGND ..... –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND ..... –0.3 V to DV_{DD} + 0.3 V
Output Voltage (D0, D1) to DGND ..... –0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 105°C/W
Lead Temperature (Soldering, 10 sec) ..... +260°C
TSSOP Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 128°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C
SOIC Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model (Z = RoHS)	Temperature Range	Package Description	Package Option	RoHS Compliant
AD7731BN	–40°C to +85°C	24-Lead PDIP	N-24-1	No
AD7731BNZ	–40°C to +85°C	24-Lead PDIP	N-24-1	Yes
AD7731BR	–40°C to +85°C	24-Lead SOIC_W	RW-24	No
AD7731BR-REEL	–40°C to +85°C	24-Lead SOIC_W	RW-24	No
AD7731BR-REEL7	–40°C to +85°C	24-Lead SOIC_W	RW-24	No
AD7731BRZ	–40°C to +85°C	24-Lead SOIC_W	RW-24	Yes
AD7731BRZ-REEL	–40°C to +85°C	24-Lead SOIC_W	RW-24	Yes
AD7731BRZ-REEL7	–40°C to +85°C	24-Lead SOIC_W	RW-24	Yes
AD7731BRU	–40°C to +85°C	24-Lead TSSOP	RU-24	No
AD7731BRU-REEL	–40°C to +85°C	24-Lead TSSOP	RU-24	No
AD7731BRU-REEL7	–40°C to +85°C	24-Lead TSSOP	RU-24	No
AD7731BRUZ	–40°C to +85°C	24-Lead TSSOP	RU-24	Yes
AD7731BRUZ-REEL	–40°C to +85°C	24-Lead TSSOP	RU-24	Yes
AD7731BRUZ-REEL7	–40°C to +85°C	24-Lead TSSOP	RU-24	Yes
EVAL-AD7731EBZ		Evaluation Board		Yes

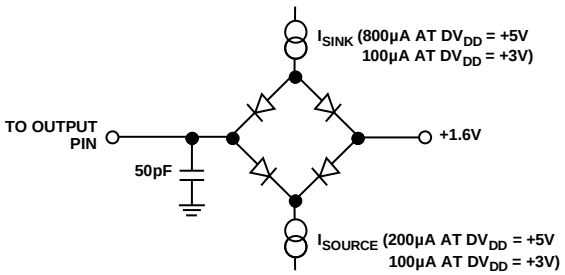
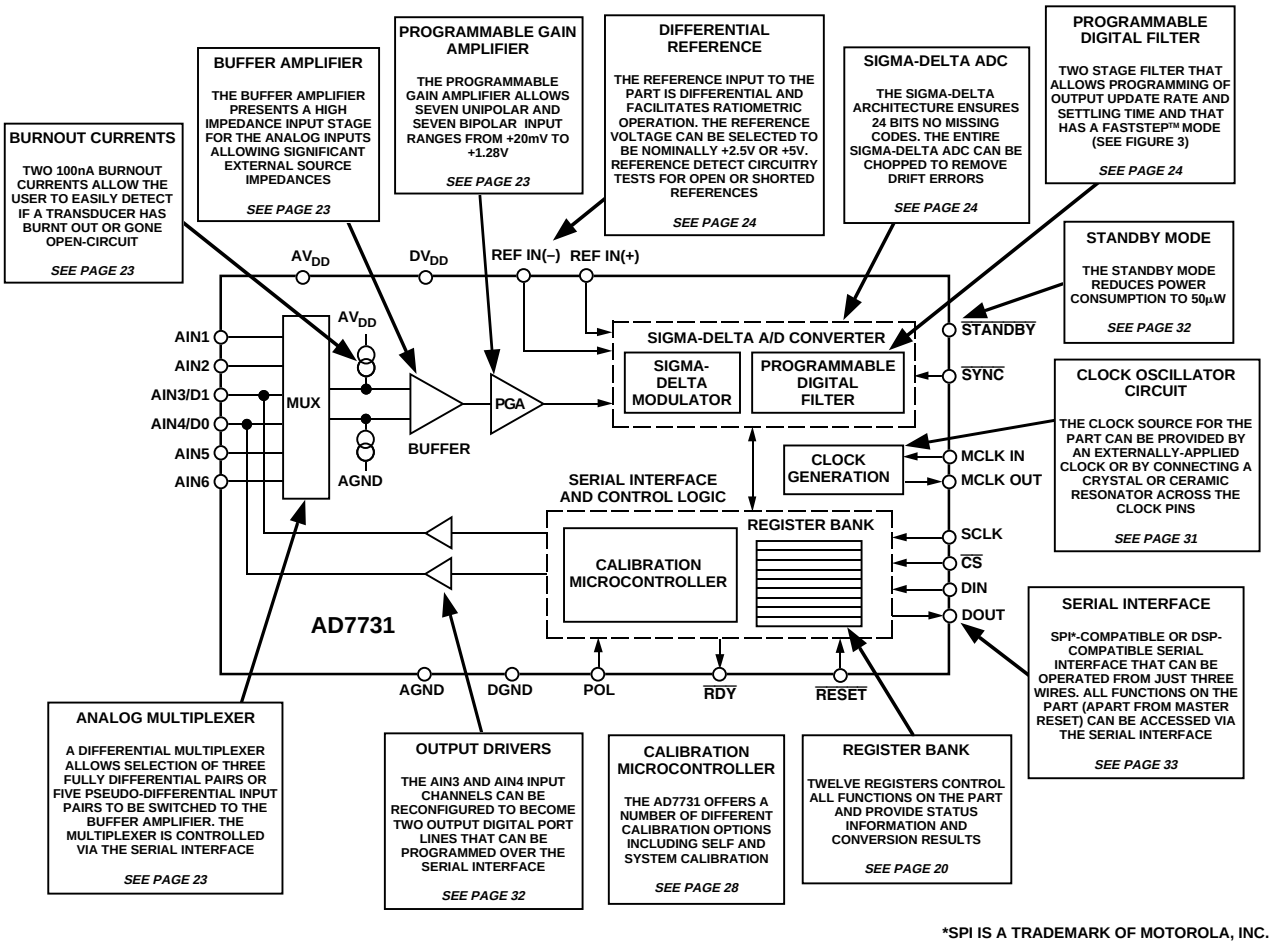


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



*SPI IS A TRADEMARK OF MOTOROLA, INC.

Figure 2. Detailed Functional Block Diagram

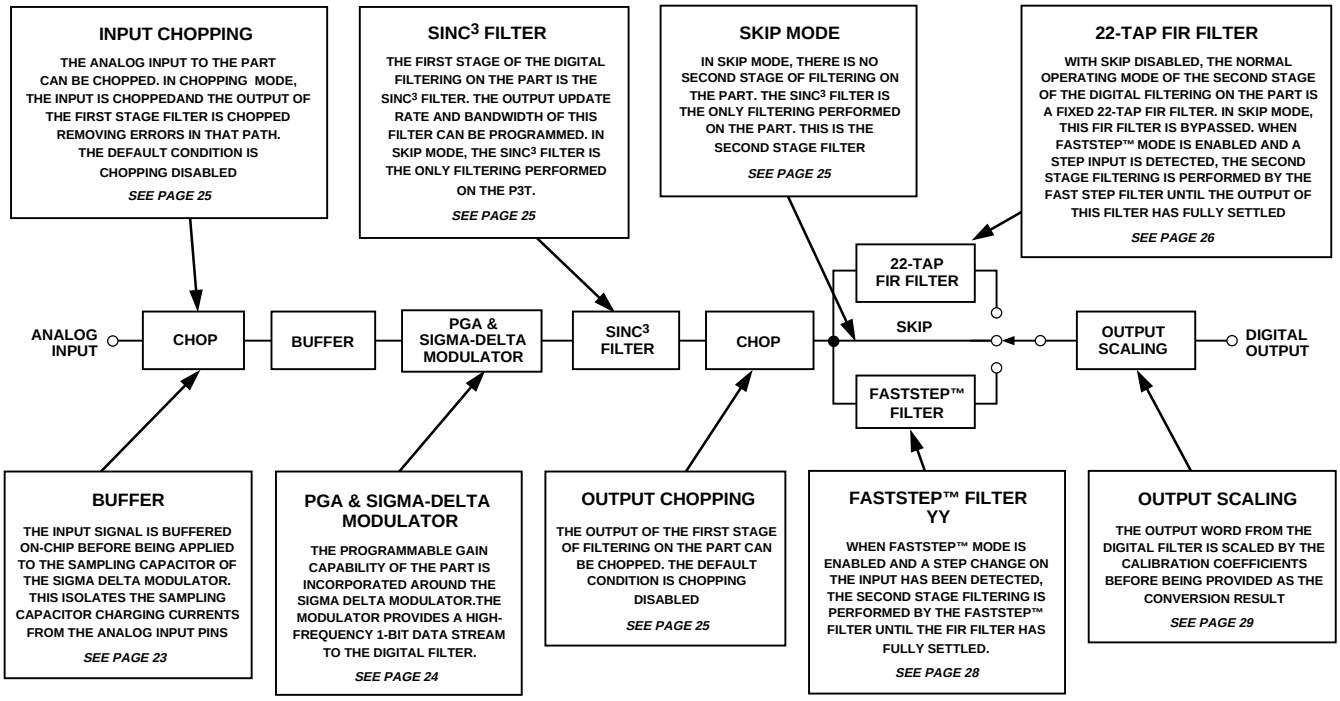
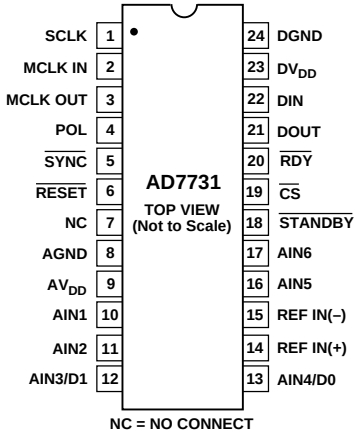


Figure 3. Signal Processing Chain

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Pin Mnemonic	Function
1	SCLK	Serial Clock. Schmitt-Triggered Logic Input. An external serial clock is applied to this input to transfer serial data to or from the AD7731. This serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the AD7731 in smaller batches of data.
2	MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal/resonator or external clock. A crystal/resonator can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The part is specified with a clock input frequency of 4.9152 MHz.

PIN FUNCTION DESCRIPTIONS (Continued)

Pin No.	Pin Mnemonic	Function
3	MCLK OUT	When the master clock for the device is a crystal/resonator, the crystal/resonator is connected between MCLK IN and MCLK OUT. If an external clock is applied to the MCLK IN, MCLK OUT provides an inverted clock signal. This clock can be used to provide a clock source for external circuits and MCLK OUT is capable of driving one CMOS load.
4	POL	Clock Polarity. Logic Input. This determines the polarity of the serial clock. If the active edge for the processor is a high-to-low SCLK transition, this input should be low. In this mode, the AD7731 puts out data on the DATA OUT line in a read operation on a low-to-high transition of SCLK and clocks in data from the DATA IN line in a write operation on a high-to-low transition of SCLK. In applications with a noncontinuous serial clock (such as most microcontroller applications), this means that the serial clock should idle low between data transfers. If the active edge for the processor is a low-to-high SCLK transition, this input should be high. In this mode, the AD7731 puts out data on the DATA OUT line in a read operation on a high-to-low transition of SCLK and clocks in data from the DATA IN line in a write operation on a low-to-high transition of SCLK. In applications with a noncontinuous serial clock (such as most microcontroller applications), this means that the serial clock should idle high between data transfers.
5	$\overline{\text{SYNC}}$	Logic Input that allows for synchronization of the digital filters and analog modulators when using a number of AD7731s. While $\overline{\text{SYNC}}$ is low, the nodes of the digital filter, the filter control logic and the calibration control logic are reset and the analog modulator is also held in its reset state. $\overline{\text{SYNC}}$ does not affect the digital interface but does reset $\overline{\text{RDY}}$ to a high state if it is low. While $\overline{\text{SYNC}}$ is asserted, the Mode Bits may be set up for a subsequent operation that will commence when the $\overline{\text{SYNC}}$ pin is deasserted.
6	$\overline{\text{RESET}}$	Logic Input. Active low input that resets the control logic, interface logic, digital filter, analog modulator and all on-chip registers of the part to power-on status. Effectively, everything on the part except for the clock oscillator is reset when the $\overline{\text{RESET}}$ pin is exercised.
7	NC	No Connect. The user is advised not to connect anything to this pin.
8	AGND	Ground reference point for analog circuitry.
9	AV_{DD}	Analog Positive Supply Voltage. The AV_{DD} to AGND differential is 5 V nominal.
10	AIN1	Analog Input Channel 1. Programmable-gain analog input that can be used as a pseudo-differential input when used with AIN6 or as the positive input of a differential pair when used with AIN2.
11	AIN2	Analog Input Channel 2. Programmable-gain analog input that can be used as a pseudo-differential input when used with AIN6 or as the negative input of a differential pair when used with AIN1.
12	AIN3/D1	Analog Input Channel 3 or Digital Output 1. This pin can be used as either an analog input or a digital output bit as determined by the DEN bit of the Mode Register. When selected as a programmable-gain analog input, it can be used as a pseudo-differential input when used with AIN6 or as the positive input of a differential pair when used with AIN4. When selected as a digital output, this output can be programmed over the serial interface using bit D1 of the Mode Register.
13	AIN4/D0	Analog Input Channel 4 or Digital Output 0. This pin can be used as either an analog input or a digital output bit as determined by the DEN bit of the Mode Register. When selected as a programmable-gain analog input, it can be used as a pseudo-differential input when used with AIN6 or as the negative input of a differential pair when used with AIN3. When selected as a digital output, this output can be programmed over the serial interface using bit D0 of the Mode Register.
14	REF IN(+)	Reference Input. Positive terminal of the differential reference input to the AD7731. REF IN(+) can lie anywhere between AV_{DD} and AGND. The nominal reference voltage (i.e., the differential voltage between REF IN(+) and REF IN(–)) should be +2.5 V when the HIREF bit of the Mode Register is 0 and is +5 V when the HIREF bit of the Mode Register is 1.
15	REF IN(–)	Reference Input. Negative terminal of the differential reference input to the AD7731. The REF IN(–) can lie anywhere between AV_{DD} and AGND.
16	AIN5	Analog Input Channel 5. Programmable-gain analog input which can be used is the positive input of a differential pair when used with AIN6.
17	AIN6	Analog Input Channel 6. Reference point for AIN1 through AIN4 in pseudo-differential mode or as the negative input of a differential input pair when used with AIN5.
18	$\overline{\text{STANDBY}}$	Logic Input. Taking this pin low shuts down the analog and digital circuitry, reducing current consumption to the 10 μA range. The on-chip registers retain all their values when the part is in standby mode.
19	$\overline{\text{CS}}$	Chip Select. Active low Logic Input used to select the AD7731. With this input hardwired low, the AD7731 can operate in its three-wire interface mode with SCLK, DIN and DOUT used to interface to the device. $\overline{\text{CS}}$ can be used to select the device in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the AD7731.

PIN FUNCTION DESCRIPTIONS (Continued)

Pin No.	Pin Mnemonic	Function
20	$\overline{RDY}$	Logic output. Used as a status output in both conversion mode and calibration mode. In conversion mode, a logic low on this output indicates that a new output word is available from the AD7731 data register. The $\overline{RDY}$ pin will return high upon completion of a read operation of a full output word. If no data read has taken place after an output update, the $\overline{RDY}$ line will return high prior to the next output update, remain high while the update is taking place and return low again. This gives an indication of when a read operation should not be initiated to avoid initiating a read from the data register as it is being updated. In calibration mode, $\overline{RDY}$ goes high when calibration is initiated and returns low to indicate that calibration is complete. A number of different events on the AD7731 set the $\overline{RDY}$ high and these are outlined in Table XVII.
21	DOUT	Serial Data Output with serial data being read from the output shift register on the part. This output shift register can contain information from the calibration registers, mode register, status register, filter register or data register depending on the register selection bits of the Communications Register.
22	DIN	Serial Data Input with serial data being written to the input shift register on the part. Data from this input shift register is transferred to the calibration registers, mode register, communications register or filter register depending on the register selection bits of the Communications Register.
23	DV_{DD}	Digital Supply Voltage, +3 V or +5 V nominal.
24	DGND	Ground reference point for digital circuitry.

TERMINOLOGY

INTEGRAL NONLINEARITY

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

POSITIVE FULL-SCALE ERROR

Positive Full-Scale Error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal AIN(+) voltage (AIN(–) + V_{REF}/GAIN – 3/2 LSBs). It applies to both unipolar and bipolar analog input ranges.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(–) + 0.5 LSB) when operating in the unipolar mode.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal AIN(+) voltage (AIN(–) – 0.5 LSB) when operating in the bipolar mode.

GAIN ERROR

This is a measure of the span error of the ADC. It is a measure of the difference between the measured and the ideal span between any two points in the transfer function. The two points used to calculate the gain error are positive full scale and negative full scale.

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(–) – V_{REF}/GAIN + 0.5 LSB) when operating in the bipolar mode. Negative full-scale error is a summation of zero error and gain error.

POSITIVE FULL-SCALE OVERRANGE

Positive Full-Scale Overrange is the amount of overhead available to handle input voltages on AIN(+) input greater than AIN(–) + V_{REF}/GAIN (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages on AIN(+) below AIN(–) – V_{REF}/GAIN without overloading the analog modulator or overflowing the digital filter.

OFFSET CALIBRATION RANGE

In the system calibration modes, the AD7731 calibrates its offset with respect to the analog input. The Offset Calibration Range specification defines the range of voltages the AD7731 can accept and still accurately calibrate offset.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7731 can accept in the system calibration mode and still accurately calibrate full scale.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7731's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full scale that the AD7731 can accept and still accurately calibrate gain.

OUTPUT NOISE AND RESOLUTION SPECIFICATION

The AD7731 has a number of different modes of operation of the on-chip filter and chopping features. These options are discussed in more detail in later sections. The part can be programmed either to optimize the throughput rate and settling time or to optimize noise and drift performance. Noise tables for two of the primary modes of operation of the part are outlined below for a selection of output rates and settling times. The first mode, where the AD7731 is configured with CHP = 0 and SKIP mode enabled, provides fast settling time while still maintaining high resolution. The second mode, where CHP = 1 and the full second filter is included, provides very low noise numbers with lower output rates. Settling time refers to the time taken to get an output that is 100% settled to the new value after a channel change or exercising $\overline{\text{SYNC}}$.

Output Noise (CHP = 0, SKIP = 1)

Table I shows the output rms noise for some typical output update rates and –3 dB frequencies for the AD7731 when used in nonchop mode (CHP of Filter Register = 0) and with the second filter bypassed (SKIP of Filter Register = 1). The table is generated with a master clock frequency of 4.9152 MHz. These numbers are typical and generated at a differential analog input voltage of 0 V. The output update rate is selected via the SF0 to SF11 bits of the Filter Register. Table II, meanwhile, shows the output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for the same output update rates. It is important to note that the numbers in Table II represent the resolution for which there will be no code flicker within a six-sigma limit. They are not calculated based on rms noise but on peak-to-peak noise.

The numbers are generated for the bipolar input ranges. When the part is operated in unipolar mode, the output noise will be the same as the equivalent bipolar input range. As a result, the numbers in Table I will remain the same for unipolar ranges. To calculate the numbers for Table II for unipolar input ranges simply subtract one from the peak-to-peak resolution number in bits.

Table I. Output Noise vs. Input Range and Update Rate (CHP = 0, SKIP = 1)

Typical Output RMS Noise in μV

Output Data Rate	–3 dB Frequency	SF Word	Settling Time	Input Range ±1.28 V	±640 mV	±320 mV	±160 mV	±80 mV	±40 mV	±20 mV
150 Hz	39.3 Hz	2048	20 ms	2.6	1.45	0.87	0.6	0.43	0.28	0.2
200 Hz	52.4 Hz	1536	15 ms	3.0	1.66	1.02	0.69	0.48	0.32	0.22
300 Hz	78.6 Hz	1024	10 ms	3.7	2	1.26	0.84	0.58	0.41	0.28
400 Hz	104.8 Hz	768	7.5 ms	4.2	2.3	1.46	1.0	0.69	0.46	0.32
600 Hz	157 Hz	512	5 ms	5.2	2.9	1.78	1.2	0.85	0.58	0.41
800 Hz	209.6 Hz	384	3.75 ms	6	3.3	2.1	1.4	0.98	0.66	0.47
1200 Hz	314 Hz	256	2.5 ms	7.8	4.3	2.6	1.8	1.27	0.82	0.57
1600 Hz	419.2 Hz	192	1.87 ms	10.9	5.4	3.5	2.18	1.51	0.94	0.64
2400 Hz	629 Hz	128	1.25 ms	27.1	13.9	7.3	3.5	2.22	1.24	0.83
3200 Hz	838.4 Hz	96	0.94 ms	47	24.4	11.4	5.3	3.1	1.9	1.0
4800 Hz	1260 Hz	64	0.625 ms	99	50.3	24.5	12.5	6.5	3.3	1.7
6400 Hz	1676 Hz	48	0.47 ms	193	97	48	24	11.8	6.6	3.0

Table II. Peak-to-Peak Resolution vs. Input Range and Update Rate (CHP = 0, SKIP = 1)

Peak-to-Peak Resolution in Bits

Output Data Rate	–3 dB Frequency	SF Word	Settling Time	Input Range ±1.28 V	±640 mV	±320 mV	±160 mV	±80 mV	±40 mV	±20 mV
150 Hz	39.3 Hz	2048	20 ms	17.5	17	17	16.5	16	15.5	15
200 Hz	52.4 Hz	1536	15 ms	17	17	16.5	16.5	16	15.5	15
300 Hz	78.6 Hz	1024	10 ms	17	16.5	16.5	16	15.5	15	14.5
400 Hz	104.8 Hz	768	7.5 ms	16.5	16.5	16	15.5	15.5	15	14.5
600 Hz	157 Hz	512	5 ms	16.5	16	16	15.5	15	14.5	14
800 Hz	209.6 Hz	384	3.75 ms	16	16	15.5	15	14.5	14.5	14
1200 Hz	314 Hz	256	2.5 ms	15.5	15.5	15.5	15	14.5	14	13.5
1600 Hz	419.2 Hz	192	1.87 ms	15	15.5	15	14.5	14	14	13.5
2400 Hz	629 Hz	128	1.25 ms	14	14	14	14	13.5	13.5	13
3200 Hz	838.4 Hz	96	0.94 ms	13	13	13	13	13	13	12.5
4800 Hz	1260 Hz	64	0.625 ms	12	12	12	12	12	11.5	12
6400 Hz	1676 Hz	48	0.47 ms	11	11	11	11	11	11	11

Output Noise (CHP = 1, SKIP = 0)

Table III shows the output rms noise for some typical output update rates and –3 dB frequencies for the AD7731 when used in chopping mode (CHP of Filter Register = 1) and with the second filter included in the loop. The numbers are generated with a master clock frequency of 4.9152 MHz. These numbers are typical and generated at a differential analog input voltage of 0 V. The output update rate is selected via the SF0 to SF11 bits of the Filter Register. Table IV, meanwhile, shows the output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for the same output update rates. It is important to note that the numbers in Table IV represent the resolution for which there will be no code flicker within a six-sigma limit. They are not calculated based on rms noise but on peak-to-peak noise.

The numbers are generated for the bipolar input ranges. When the part is operated in unipolar mode, the output noise will be the same as the equivalent bipolar input range. As a result, the numbers in Table III will remain the same for unipolar ranges. To calculate the number for Table IV for unipolar input ranges simply subtract one from the peak-to-peak resolution number in bits.

Table III. Output Noise vs. Input Range and Update Rate (CHP = 1, SKIP = 0)

Typical Output RMS Noise in nV

Output Data Rate	–3 dB Frequency	SF Word	Settling Time		Input Range						
			Normal	Fast Step	±1.28 V	±640 mV	±320 mV	±160 mV	±80 mV	±40 mV	±20 mV
50 Hz	1.97 Hz	2048	440 ms	40 ms	700	425	265	170	120	85	55
100 Hz	3.95 Hz	1024	220 ms	20 ms	980	550	330	230	190	115	90
150 Hz	5.92 Hz	683	147 ms	13.3 ms	1230	700	445	270	210	140	100
200 Hz	7.9 Hz	512	110 ms	10 ms	1260	840	500	340	245	170	105
400 Hz	15.8 Hz	256	55 ms	5 ms	2000	1230	690	430	335	215	160
800 Hz	31.6 Hz	128	27.5 ms	2.5 ms	3800	2100	1400	760	590	345	220

Table IV. Peak-to-Peak Resolution vs. Input Range and Update Rate (CHP = 1, SKIP = 0)

Peak-to-Peak Resolution in Bits

Output Data Rate	–3 dB Frequency	SF Word	Settling Time		Input Range						
			Normal	Fast Step	±1.28 V	±640 mV	±320 mV	±160 mV	±80 mV	±40 mV	±20 mV
50 Hz	1.97 Hz	2048	440 ms	40 ms	19	19	18.5	18.5	18	17.5	17
100 Hz	3.95 Hz	1024	230 ms	30 ms	19	18.5	18.5	18	17	17	16
150 Hz	5.92 Hz	683	147 ms	13.3 ms	18.5	18	18	17.5	17	16.5	16
200 Hz	7.9 Hz	512	110 ms	10 ms	18.5	18	17.5	17.5	17	16.5	16
400 Hz	15.8 Hz	256	55 ms	5 ms	17.5	17.5	17	17	16.5	16	15.5
800 Hz	31.6 Hz	128	27.5 ms	2.5 ms	17	16.5	16	16	15.5	15	15

ON-CHIP REGISTERS

The AD7731 contains 12 on-chip registers that can be accessed via the serial port of the part. These registers are summarized in Figure 4 and in Table V, and described in detail in the following sections.

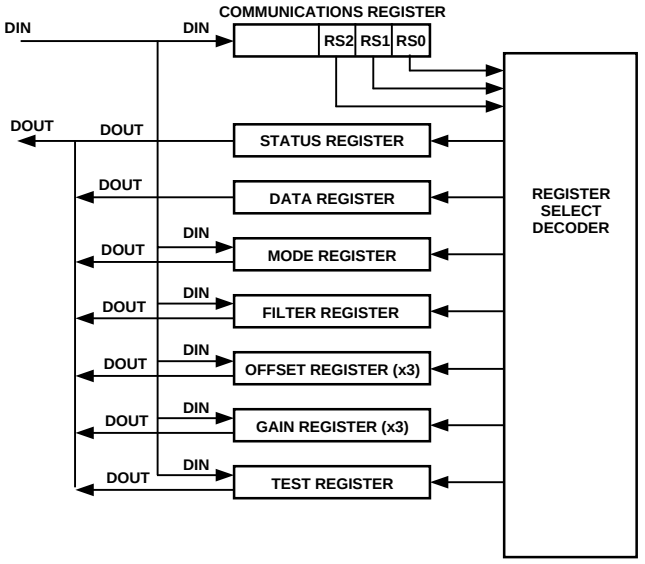


Figure 4. Register Overview

Table V. Summary of On-Chip Registers

Register Name	Type	Size	Power-On/Reset Default Value	Function
Communications Register $\overline{WEN}$ ZERO RW1 RW0 ZERO RS2 RS1 RS0	Write Only	8 Bits	Not Applicable	All operations to other registers are initiated through the Communications Register. This controls whether subsequent operations are read or write operations and also selects the register for that subsequent operation. Most subsequent operations return control to the Communications Register except for the continuous read mode of operation.
Status Register $\overline{RDY}$ $\overline{STDY}$ STBY NOREF MS3 MS2 MS1 MS0	Read Only	8 Bits	CX Hex	Provides status information on conversions, calibrations, settling to step inputs, standby operation and the validity of the reference voltage.
Data Register	Read Only	16 Bits or 24 Bits	000000 Hex	Provides the most up-to-date conversion result from the part. Register length can be programmed to be 16 bit or 24 bit.
Mode Register MD2 MD1 MD0 $\overline{B}$/U DEN D1 D0 WL HIREF RN2 RN1 RN0 BO CH2 CH1 CH0	Read/Write	16 Bits	0174 Hex	Controls functions such as mode of operation, unipolar/bipolar operation, controlling the function of AIN3/D1 and AIN4/D0, burnout current and Data Register word length. It also contains the reference selection bit, the range selection bits and the channel selection bits.
Filter Register SF11 SF10 SF9 SF8 SF7 SF6 SF5 SF4 SF3 SF2 SF1 SF0 ZERO CHP SKIP FAST	Read/Write	16 Bits	2002 Hex	Controls the amount of averaging in the first stage filter, selects the fast step and skip modes and controls the chopping modes on the part.
Offset Register	Read/Write	24 Bits		Contains a 24-bit word which is the offset calibration coefficient for the part. The contents of this register are used to provide offset correction on the output from the digital filter. There are three Offset Registers on the part and these are associated with input channel pairs as outlined in Table XIII.
Gain Register	Read/Write	24 Bits		Contains a 24-bit word which is the gain calibration coefficient for the part. The contents of this register are used to provide gain correction on the output from the digital filter. There are three Gain Registers on the part and these are associated with input channel pairs as outlined in Table XIII.
Test Register	Read/Write	24 Bits	000000 Hex	Controls the test modes of the part which are used when testing the part. **The user is advised not to change the contents of this register.**

Communications Register (RS2-RS0 = 0, 0, 0)

The Communications Register is an 8-bit write-only register. All communications to the part must start with a write operation to the Communications Register. The data written to the Communications Register determines whether the next operation is a read or write operation, the type of read operation and to which register this operation takes place. For single-shot read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the Communications Register. This is the default state of the interface, and on power-up or after a $\overline{\text{RESET}}$, the AD7731 is in this default state waiting for a write operation to the Communications Register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high, returns the AD7731 to this default state by resetting the part. Table VI outlines the bit designations for the Communications Register. CR0 through CR7 indicate the bit location, CR denoting the bits are in the Communications Register. CR7 denotes the first bit of the data stream.

Table VI. Communications Register

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$	ZERO	RW1	RW0	ZERO	RS2	RS1	RS0

Bit Location	Bit Mnemonic	Description
CR7	$\overline{\text{WEN}}$	Write Enable Bit. A 0 must be written to this bit so the write operation to the Communications Register actually takes place. If a 1 is written to this bit, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits will be loaded to the Communications Register.
CR6	ZERO	A zero **must** be written to this bit to ensure correct operation of the AD7731.
CR5, CR4	RW1, RW0	Read Write Mode Bits. These two bits determine the nature of the subsequent read/write operation. Table VII outlines the four options.

Table VII. Read/Write Mode

RW1	RW0	Read/Write Mode
0	0	Single Write to Specified Register
0	1	Single Read of Specified Register
1	0	Start Continuous Read of Specified Register
1	1	Stop Continuous Read Mode

With 0, 0 written to these two bits, the next operation is a write operation to the register specified by bits RS2, RS1, RS0. Once the subsequent write operation to the specified register has been completed, the part returns to where it is expecting a write operation to the Communications Register.

With 0, 1 written to these two bits, the next operation is a read operation of the register specified by bits RS2, RS1, RS0. Once the subsequent read operation to the specified register has been completed, the part returns to where it is expecting a write operation to the Communications Register.

Writing 1, 0 to these bits, sets the part into a mode of continuous reads from the register specified by bits RS2, RS1, RS0. The most likely registers which the user will want to use this function with are the Data Register and the Status Register. Subsequent operations to the part will consist of read operations to the specified register without any intermediate writes to the Communications Register. This means that once the next read operation to the specified register has taken place, the part will be in a mode where it is expecting another read from that specified register. The part will remain in this continuous read mode until 30 Hex has been written to bits RW1 and RW0.

When 1, 1 is written to these bits (and 0 written to bits CR3 through CR0), the continuous read mode is stopped and the part returns to where it is expecting a write operation to the Communications Register. Note, the part continues to look at the DIN line on each SCLK edge during the continuous read mode so that it can determine when to stop the continuous read mode. Therefore, the user must be careful not to inadvertently exit the continuous read mode or reset the part by writing a series of 1s to the part. The easiest way to avoid this is to place a logic 0 on the DIN line while the part is in continuous read mode.

Bit Location	Bit Mnemonic	Description
CR3	ZERO	A zero **must** be written to this bit to ensure correct operation of the AD7731.
CR2-CR0	RS2-RS0	Register Selection Bits. RS2 is the MSB of the three selection bits. The three bits select to which one of eight on-chip registers the next read or write operation takes place as shown in Table VIII.

Table VIII. Register Selection

RS2	RS1	RS0	Register
0	0	0	Communications Register (Write Operation)
0	0	0	Status Register (Read Operation)
0	0	1	Data Register
0	1	0	Mode Register
0	1	1	Filter Register
1	0	0	No Register Access
1	0	1	Offset Register
1	1	0	Gain Register
1	1	1	Test Register

Status Register (RS2-RS0 = 0, 0, 0); Power-On/Reset Status: CX Hex

The Status Register is an 8-bit read-only register. To access the Status Register, the user must write to the Communications Register selecting either a single-shot read or continuous read mode and load bits RS2, RS1, RS0 with 0, 0, 0. Table IX outlines the bit designations for the Status Register. SR0 through SR7 indicate the bit location, SR denoting the bits are in the Status Register. SR7 denotes the first bit of the data stream. Figure 5 shows a flowchart for reading from the registers on the AD7731. The number in brackets indicates the power-on/reset default status of that bit.

Table IX. Status Register

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
$\overline{\text{RDY}}$ (1)	$\overline{\text{STDY}}$ (1)	STBY (0)	NOREF (0)	MS3 (X)	MS2 (X)	MS1 (X)	MS0 (X)

Bit Location	Bit Mnemonic	Description
SR7	$\overline{\text{RDY}}$	Ready Bit. This bit provides the status of the $\overline{\text{RDY}}$ flag from the part. The status and function of this bit is the same as the $\overline{\text{RDY}}$ output pin. A number of events set the $\overline{\text{RDY}}$ bit high as indicated in Table XVII.
SR6	$\overline{\text{STDY}}$	Steady Bit. This bit is updated when the filter writes a result to the Data Register. If the filter is in *FAST*Step™ mode (see Filter Register section), and responding to a step input, the $\overline{\text{STDY}}$ bit remains high as the initial conversion results become available. The $\overline{\text{RDY}}$ output and bit are set low on these initial conversions to indicate that a result is available. However, if the $\overline{\text{STDY}}$ is high, it indicates that the result being provided is not from a fully settled second-stage FIR filter. When the FIR filter has fully settled, the $\overline{\text{STDY}}$ bit will go low coincident with $\overline{\text{RDY}}$. If the part is never placed into its *FAST*Step™ mode, the $\overline{\text{STDY}}$ bit will go low at the first Data Register read and it is not cleared by subsequent Data Register reads. A number of events set the $\overline{\text{STDY}}$ bit high as indicated in Table XVII. $\overline{\text{STDY}}$ is set high along with $\overline{\text{RDY}}$ by all events in the table except a Data Register read.
SR5	STBY	Standby Bit. This bit indicates whether the AD7731 is in its Standby Mode or normal mode of operation. The part can be placed in its standby mode using the $\overline{\text{STANDBY}}$ input pin or by writing 011 to the MD2 to MD0 bits of the Mode Register. The power-on/reset status of this bit is 0 assuming the $\overline{\text{STANDBY}}$ pin is high.
SR4	NOREF	No Reference Bit. If the voltage between the REF IN(+) and REF IN(–) pins is below 0.5 V or either of these inputs is open-circuit, the NOREF bit goes to 1. If NOREF is active on completion of a conversion, the Data Register is loaded with all 1s. If NOREF is active on completion of a calibration, updating of the calibration registers is inhibited.
SR3-SR0	MS3-MS0	These bits are for factory use. The power-on/reset status of these bits varies depending on the factory-assigned number.

Data Register (RS2-RS0 = 0, 0, 1); Power On/Reset Status: 000000 Hex

The Data Register on the part is a read-only register that contains the most up-to-date conversion result from the AD7731. Figure 5 shows a flowchart for reading from the registers on the AD7731. The register can be programmed to be either 16 or 24 bits wide, determined by the status of the WL bit of the Mode Register. The $\overline{RDY}$ output and $\overline{RDY}$ bit of the Status Register are set low when the Data Register is updated. The $\overline{RDY}$ pin and $\overline{RDY}$ bit will return high once the full contents of the register (either 16 or 24 bits) have been read. If the Data Register has not been read by the time the next output update occurs, the $\overline{RDY}$ pin and $\overline{RDY}$ bit will go high for at least $158.5 \times t_{CLK\ IN}$ indicating when a read from the Data Register should not be initiated to avoid a transfer from the Data Register as it is being updated. Once the updating of the Data Register has taken place, $\overline{RDY}$ returns low.

If the Communications Register data sets up the part for a write operation to this register, a write operation must actually take place in order to return the part to where it is expecting a write operation to the Communications Register (the default state of the interface). However, the 16 or 24 bits of data written to the part will be ignored by the AD7731.

Mode Register (RS2-RS0 = 0, 1, 0); Power-On/Reset Status: 0174 Hex

The Mode Register is a 16-bit register from which data can either be read or to which data can be written. This register configures the operating modes of the AD7731, the input range selection, the channel selection and the word length of the Data Register. Table X outlines the bit designations for the Mode Register. MR0 through MR15 indicate the bit location, MR denoting the bits are in the Mode Register. MR15 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit. Figure 5 shows a flowchart for reading from the registers on the AD7731 and Figure 6 shows a flowchart for writing to the registers on the part.

Table X. Mode Register

MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8
MD2 (0)	MD1 (0)	MD0 (0)	$\overline{B}$/U (0)	DEN (0)	D1 (0)	D0 (0)	WL (1)

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
HIREF (0)	RN2 (1)	RN1 (1)	RN0 (1)	BO (0)	CH2 (1)	CH1 (0)	CH0 (0)

Bit Location	Bit Mnemonic	Description
MR15–MR13	MD2–MD0	Mode Bits. These three bits determine the mode of operation of the AD7731 as outlined in Table XI. The modes are independent, such that writing new mode bits to the Mode Register will exit the part from the mode in which it is operating and place it in the new requested mode immediately after the Mode Register write. The function of the mode bits is described in more detail below.

Table XI. Operating Modes

MD2	MD1	MD0	Mode of Operation	
0	0	0	Sync (Idle) Mode	Power-On/Reset Default
0	0	1	Continuous Conversion Mode	
0	1	0	Single Conversion Mode	
0	1	1	Power-Down (Standby) Mode	
1	0	0	Internal Zero-Scale Calibration	
1	0	1	Internal Full-Scale Calibration	
1	1	0	System Zero-Scale Calibration	
1	1	1	System Full-Scale Calibration	

MD2	MD1	MD0	Operating Mode
0	0	0	Sync (Idle) Mode. In this mode, the modulator and filter are held in reset mode and the AD7731 is not processing any new samples or data. Placing the part in this mode is equivalent to exerting the $\overline{\text{SYNC}}$ input pin. However, exerting the $\overline{\text{SYNC}}$ does not actually force these mode bits to 0, 0, 0. The part returns to this mode after a calibration or after a conversion in Single Conversion Mode. This is the default condition of these bits after Power-On/Reset.
0	0	1	Continuous Conversion Mode. In this mode, the AD7731 is continuously processing data and providing conversion results to the Data Register at the programmed output update rate (as determined by the Filter Register). For most applications, this would be the normal operating mode of the AD7731.
0	1	0	Single Conversion Mode. In this mode, the AD7731 performs a single conversion, updates the Data Register, returns to the Sync Mode and resets the mode bits to 0, 0, 0. The result of the single conversion on the AD7731 in this mode will not be provided until the full settling-time of the filter has elapsed.
0	1	1	Power-Down (Standby) Mode. In this mode, the AD7731 goes into its power-down or standby state. Placing the part in this mode is equivalent to exerting the $\overline{\text{STANDBY}}$ input pin. However, exerting $\overline{\text{STANDBY}}$ does not actually force these mode bits to 0, 1, 1.
1	0	0	Zero-Scale Self-Calibration Mode. This activates zero-scale self-calibration on the channel selected by the CH2, CH1 and CH0 bits of the Mode Register. This zero-scale self-calibration is performed at the selected gain on internally shorted (zeroed) inputs. When this zero-scale self-calibration is complete, the part updates the contents of the Offset Calibration Register and returns to Sync Mode with MD2, MD1 and MD0 returning to 0, 0, 0. The $\overline{\text{RDY}}$ output and bit go high when calibration is initiated and return low when this zero-scale self-calibration is complete to indicate that the part is back in Sync Mode and ready for further operations.
1	0	1	Full-Scale Self-Calibration Mode. This activates full-scale self-calibration on the channel selected by the CH2, CH1 and CH0 bits of the Mode Register. This full-scale self-calibration is performed at the selected gain on an internally-generated full-scale signal. When this full-scale self-calibration is complete, the part updates the contents of the Gain Calibration Register and returns to Sync Mode with MD2, MD1 and MD0 returning to 0, 0, 0. The $\overline{\text{RDY}}$ output and bit go high when calibration is initiated and return low when this full-scale self-calibration is complete to indicate that the part is back in Sync Mode and ready for further operations.
1	1	0	Zero-Scale System Calibration Mode. This activates zero scale system calibration on the channel selected by the CH2, CH1 and CH0 bits of the Mode Register. Calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. When this zero-scale system calibration is complete, the part updates the contents of the Offset Calibration Register and returns to Sync Mode with MD2, MD1 and MD0 returning to 0, 0, 0. The $\overline{\text{RDY}}$ output and bit go high when calibration is initiated and return low when this zero-scale calibration is complete to indicate that the part is back in Sync Mode and ready for further operations.
1	1	1	Full-Scale System Calibration Mode. This activates full-scale system calibration on the selected input channel. Calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. When this full-scale system calibration is complete, the part updates the contents of the Gain Calibration Register and returns to Sync Mode with MD2, MD1 and MD0 returning to 0, 0, 0. The $\overline{\text{RDY}}$ output and bit go high when calibration is initiated and return low when this full-scale calibration is complete to indicate that the part is back in Sync Mode and ready for further operations.

Bit Location	Bit Mnemonic	Description
MR12	$\overline{B}$/U	Bipolar/Unipolar Bit. A 0 in this bit selects bipolar operation and the output coding is 00...000 for negative full-scale input, 10...000 for zero input and 11...111 for positive full-scale input. A 1 in this bit selects unipolar operation and the output coding is 00...000 for zero input and 11...111 for positive full-scale input.
MR11	DEN	Digital Output Enable Bit. With this bit at 1, the AIN3/D1 and AIN4/D0 pins assume their digital output functions and the output drivers connected to these pins are enabled. In this mode, the user effectively has two port bits which can be programmed over the serial interface.
MR10–MR9	D1–D0	Digital Output Bits. These bits determine the digital outputs on the AIN3/D1 and AIN4/D0 pins respectively when the DEN bit is a 1. For example, a 1 written to the D1 bit of the Mode Register (with the DEN bit also a 1) will put a logic 1 on the AIN3/D1 pin. This logic 1 will remain on this pin until a 0 is written to the D1 bit (in which case, the AIN3/D1 pin goes to a logic 0) or the digital output function is disabled by writing a 0 to the DEN bit.
MR8	WL	Data Word Length Bit. This bit determines the word length of the Data Register. A 0 in this bit selects 16-bit word length when reading from the data register (i.e., $\overline{RDY}$ returns high after 16 serial clock cycles in the read operation). A 1 in this bit selects 24-bit word length for the Data Register.
MR7	HIREF	High Reference Bit. This bit should be set in accordance with the reference voltage which is being used on the part. If the reference voltage is 2.5 V, the HIREF bit should be set to 0. If the reference voltage is 5 V, the HIREF bit should be set to a 1. With the HIREF bit set correctly for the appropriate applied reference voltage, the input ranges are 0 mV to +20 mV, +40 mV, +80 mV, +160 mV, +320 mV, +640 mV and +1.28 V for unipolar operation and ±20 mV, ±40 mV, ±80 mV, ±160 mV, ±320 mV, ±640 mV and ±1.28 V for bipolar operation. It is possible for a user with a 2.5 V reference to set the HIREF bit to a 1. In this case, the part is operating with a 2.5 V reference but assumes it has a 5 V reference. As a result, the input ranges on the part become 0 mV to +10 mV through 0 mV to +640 mV for unipolar operation and ±10 mV through ±640 mV for bipolar operation. However, the output noise from the part (in nV) will remain unchanged so the resolution of the part (in LSBs) will reduce by 1.
MR6–MR4	RN2–RN0	Input Range Bits. These bits determine the analog input range for the selected analog input. The different input ranges are outlined in Table XII. The table is valid for a reference voltage of 2.5 V with the HIREF bit at 0 or for a reference voltage of 5 V with the HIREF bit at a logic 1.

Table XII. Input Range Selection

RN2	RN1	RN0	Input Range $\overline{B}$/U Bit = 0	Input Range $\overline{B}$/U Bit = 1	
0	0	0	–20 mV to +20 mV	0 mV to +20 mV	
0	0	1	–20 mV to +20 mV	0 mV to +20 mV	
0	1	0	–40 mV to +40 mV	0 mV to +40 mV	
0	1	1	–80 mV to +80 mV	0 mV to +80 mV	
1	0	0	–160 mV to +160 mV	0 mV to +160 mV	
1	0	1	–320 mV to +320 mV	0 mV to +320 mV	
1	1	0	–640 mV to +640 mV	0 mV to +640 mV	
1	1	1	–1.28 V to +1.28 V	0 mV to +1.28 V	Power-On/Reset Default

Bit Location	Bit Mnemonic	Description
MR3	BO	Burnout Current Bit. A 1 in this bit activates the burnout currents. When active, the burnout currents connect to the selected analog input pair, one source current to the AIN(+) input and one sink current to the AIN(–) input. A 0 in this bit turns off the on-chip burnout currents.
MR2–MR0	CH2–CH0	Channel Select. These three bits select a channel either for conversion or for access to calibration coefficients as outlined in Table XIII. There are three pairs of calibration registers on the part. In fully differential mode, the part has three input channels so each channel has its own pair of calibration registers. In pseudo-differential mode, the AD7731 has five input channels with some of the input channel combinations sharing calibration registers. With CH2, CH1 and CH0 at a logic 1, the part looks at the AIN6 input internally shorted to itself. This can be used as a test method to evaluate the noise performance of the part with no external noise sources. In this mode, the AIN6 input should be connected to an external voltage within the allowable common-mode range for the part. The power-on/default status of these bits is 1, 0, 0.

Table XIII. Channel Selection

CH2	CH1	CH0	AIN(+)	AIN(–)	Type	Calibration Register Pair
0	0	0	AIN1	AIN6	Pseudo Differential	Register Pair 0
0	0	1	AIN2	AIN6	Pseudo Differential	Register Pair 1
0	1	0	AIN3	AIN6	Pseudo Differential	Register Pair 2
0	1	1	AIN4	AIN6	Pseudo Differential	Register Pair 2
1	0	0	AIN1	AIN2	Fully Differential	Register Pair 0
1	0	1	AIN3	AIN4	Fully Differential	Register Pair 1
1	1	0	AIN5	AIN6	Fully Differential	Register Pair 2
1	1	1	AIN6	AIN6	Test Mode	Register Pair 2

Filter Register (RS2-RS0 = 0, 1, 1); Power-On/Reset Status: 2002 Hex

The Filter Register is a 16-bit register from which data can either be read or to which data can be written. This register determines the amount of averaging performed by the filter and the mode of operation of the filter. It also sets the chopping mode. Table XIV outlines the bit designations for the Filter Register. FR0 through FR15 indicate the bit location, FR denoting the bits are in the Filter Register. FR15 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit. Figure 5 shows a flowchart for reading from the registers on the AD7731 and Figure 6 shows a flowchart for writing to the registers on the part.

Table XIV. Filter Register

FR15	FR14	FR13	FR12	FR11	FR10	FR9	FR8
SF11 (0)	SF10 (0)	SF9 (1)	SF8 (0)	SF7 (0)	SF6 (0)	SF5 (0)	SF4 (0)

FR7	FR6	FR5	FR4	FR3	FR2	FR1	FR0
SF3 (0)	SF2 (0)	SF1 (0)	SF0 (0)	ZERO (0)	CHP (0)	SKIP (1)	FAST (0)

Bit Location	Bit Mnemonic	Description
FR15–FR4	SF11–SF0	$Sinc^3$ Filter Selection Bits. The AD7731 contains two filters, a $Sinc^3$ filter and an FIR filter. The 12 bits programmed to SF11 through SF0 sets the amount of averaging which the $Sinc^3$ filter performs. As a result, the number programmed to these 12 bits affects the –3 dB frequency and output update rate from the part (see Filter Architecture section). The allowable range for SF words depends on whether the part is operated with CHP on or off and SKIP on or off. Table XV outlines the SF ranges for different setups.

Table XV. SF Ranges

CHOP	SKIP	SF Range	Output Update Rate Range (Assuming 4.9152 MHz Clock)
0	0	2048 to 150	150 Hz to 2.048 kHz
1	0	2048 to 75	50 Hz to 1.365 kHz
0	1	2048 to 40	150 Hz to 7.6 kHz
1	1	2048 to 20	50 Hz to 5.12 kHz

Bit Location	Bit Mnemonic	Description
FR3	ZERO	A zero **must** be written to this bit to ensure correct operation of the AD7731.
FR2	CHP	Chop Enable Bit. This bit determines if the chopping mode on the part is enabled. A 1 in this bit location enables chopping on the part. When the chop mode is enabled, the part is effectively chopped at its input and output to remove all offset and offset drift errors on the part. If offset performance with time and temperature are important parameters in the design, it is recommended that the user enable chopping on the part.
FR1	SKIP	FIR Filter Skip Bit. With a 0 in this bit, the AD7731 performs two stages of filtering before shipping a result out of the filter. The first is a $Sinc^3$ filter followed by a 22-tap FIR filter. With a 1 in this bit, the FIR filter on the part is bypassed and the output of the $Sinc^3$ is fed directly as the output result of the AD7731's filter (see Filter Architecture for more details on the filter implementation).
FR0	FAST	*FAST*Step™ Mode Enable Bit. A 1 in this bit enables the *FAST*Step™ mode on the AD7731. In this mode, if a step change on the input is detected, the FIR calculation portion of the filter is suspended and replaced by a simple moving average on the output of the $Sinc^3$ filter. Initially, two outputs from the $sinc^3$ filter are used to calculate an AD7731 output. The number of $sinc^3$ outputs used to calculate the moving average output is increased (from 2 to 4 to 8 to 16) until the $\overline{STDY}$ bit goes low. When the FIR filter has fully settled after a step, the $\overline{STDY}$ bit will become active and the FIR filter is switched back into the processing loop (see Filter Architecture section for more details on the *FAST*Step™ mode).

Offset Calibration Register (RS2–RS0 = 1, 0, 1)

The AD7731 contains three 24-bit Offset Calibration Registers, labeled Offset Calibration Register 0 to Offset Calibration Register 2, to which data can be written and from which data can be read. The three registers are totally independent of each other such that in fully-differential mode there is an offset register for each of the input channels. This register is used in conjunction with the associated Gain Calibration Register to form a register pair. The calibration register pair used to scale the output of the filter is as outlined in Table XIII. To access the appropriate Offset Calibration Register the user should write first to the Mode Register setting up the appropriate address in the CH2 to CH0 bits.

The Offset Calibration Register is updated after an offset calibration routine (1, 0, 0 or 1, 1, 0 loaded to the MD2, MD1, MD0 bits of the Mode Register). During subsequent conversions, the contents of this register are subtracted from the filter output prior to gain scaling being performed on the word. Figure 5 shows a flowchart for reading from the registers on the AD7731 and Figure 6 shows a flowchart for writing to the registers on the part.

Gain Calibration Register (RS2–RS0 = 1, 1, 0)

The AD7731 contains three 24-bit Gain Calibration Registers to which data can be written and from which data can be read. The three registers are totally independent of each other such that in fully-differential mode there is a gain register for each of the input channels. This register is used in conjunction with the associated Offset Calibration Register to form a register pair which scale the output of the filter before it is loaded to the Data Register. These register pairs are associated with input channel pairs as outlined in Table XIII. To access the appropriate Gain Calibration Register the user should write first to the Mode Register setting up the appropriate address in the CH2 to CH0 bits.

The Gain Calibration Register is updated after a gain calibration routine (1, 0, 1 or 1, 1, 1 loaded to the MD2, MD1, MD0 bits of the Mode Register). During subsequent conversions, the contents of this register are used to scale the number which has already been offset corrected with the Offset Calibration Register contents. Figure 5 shows a flowchart for reading from the registers on the AD7731 and Figure 6 shows a flowchart for writing to the registers on the part.

Test Register (RS2–RS0 = 1, 1, 1); Power On/Reset Status: 000000Hex

The AD7731 contains a 24-bit Test Register to which data can be written and from which data can be read. The contents of this register are used in testing the device. The user is advised not to change the status of any of the bits in this register from the default (Power-On or $\overline{RESET}$) status of all 0s as the part will be placed in one of its test modes and will not operate correctly. If the part enters one of its test modes, exercising $\overline{RESET}$ or writing 32 successive 1s to the part will exit the part from the mode and return all register contents to their power-on/reset status. Note, if the part is placed in one of its test modes, it may not be possible to read back the contents of the Test Register depending on the test mode which the part has been placed.

READING FROM AND WRITING TO THE ON-CHIP REGISTERS

The AD7731 contains a total of twelve on-chip registers. These registers are all accessed over a three-wire interface. As a result, addressing of registers is via a write operation to the topmost register on the part, the Communications Register. Figure 5 shows a flowchart for reading from the different registers on the part summarizing the sequence and the words to be written to access each of the registers. Figure 6 gives a flowchart for writing to the different registers on the part, again summarizing the sequence and words to be written to the AD7731.

Register	Byte W (Hex)	Byte Y (Hex)	Byte Z (Hex)
Status Register	10	20	30
Data Register	11	21	30
Mode Register	12	22	30
Filter Register	13	N/A*	N/A*
Offset Register	15	N/A*	N/A*
Gain Register	16	N/A*	N/A*

*N/A = Not Applicable. Continuous reads of these registers does not make sense as the register contents would remain the same since they are only changed by a write operation.

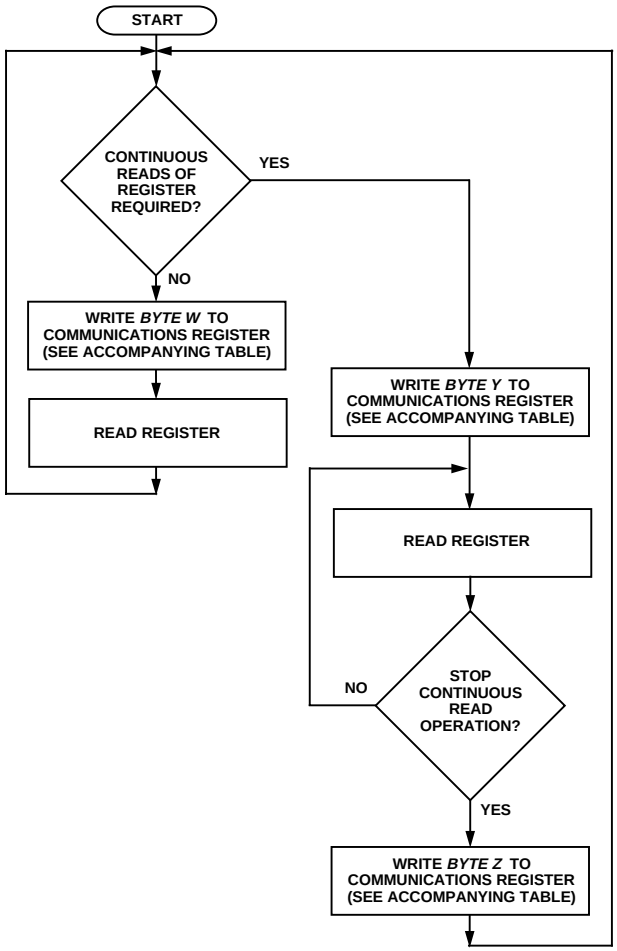


Figure 5. Flowchart for Reading from the AD7731 Registers

Register	Byte Y (Hex)
Communications Register	00
Data Register	Read Only Register.
Mode Register	02
Filter Register	03
Offset Register	05
Gain Register	06
Test Register	User is advised not to change contents of Test Register

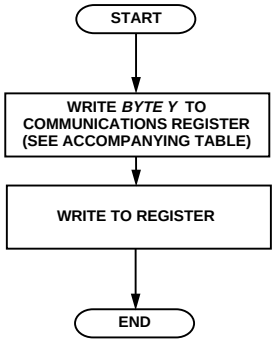


Figure 6. Flowchart for Writing to the AD7731 Registers

CALIBRATION OPERATION SUMMARY

The AD7731 contains a number of calibration options as outlined previously. Table XVI summarizes the calibration types, the operations involved and the duration of the operations. There are two methods of determining the end of calibration. The first is to monitor the hardware $\overline{RDY}$ pin using either interrupt-driven or polling routines. The second method is to do a software poll of the $\overline{RDY}$ bit in the Status Register. This can be achieved by setting up the part for continuous reads of the Status Register once a calibration has been initiated. The $\overline{RDY}$ pin and $\overline{RDY}$ bit go high on initiating a calibration and return low at the end of the calibration routine. At this time, the MD2, MD1, MD0 bits of the Mode Register have returned to 0, 0, 0. The FAST and SKIP bits are treated as 0 for the calibration sequence so the full filter is always used for the calibration routines. See Calibration section for full details.

Table XVI. Calibration Operations

Calibration Type	MD2, MD1, MD0	Duration to $\overline{RDY}$ Low (CHP = 1)	Duration to $\overline{RDY}$ Low (CHP = 0)	Calibration Sequence
Internal Zero-Scale	1, 0, 0	22 × 1/Output Rate	24 × 1/Output Rate	Calibration on internal shorted input with PGA set for selected input range. The Offset Calibration Register for the selected channel is updated at the end of this calibration sequence. For full self-calibration, this calibration should be preceded by an Internal Full-Scale calibration. For applications which require an Internal Zero-Scale and System Full Scale calibration, this Internal Zero-Scale calibration should be performed first.
Internal Full-Scale	1, 0, 1	44 × 1/Output Rate	48 × 1/Output Rate	Calibration on internally-generated input full-scale with PGA set for selected input range. The Gain Calibration Register for the selected channel is updated at the end of this calibration sequence. It is recommended that internal full-scale calibrations are performed on the operating input range except for the 20 mV and 40 mV input ranges where optimum results are achieved by calibrating on the 80 mV range. This calibration should be followed by either an Internal Zero-Scale or System Zero-Scale calibration. This calibration should be followed by either an Internal Zero-Scale or System Zero-Scale calibration. This zero-scale calibration should be performed at the operating input range.
System Zero-Scale	1, 1, 0	22 × 1/Output Rate	24 × 1/Output Rate	Calibration on externally-applied input voltage with PGA set for selected input range. The input applied is assumed to be the zero-scale of the system. For full system calibration, this System Zero-Scale calibration should be performed first. For applications which require a System Zero-Scale and Internal Full Scale calibration, this calibration should be preceded by the Internal Full-Scale calibration. The Offset Calibration Register for the selected channel is updated at the end of this calibration sequence.
System Full-Scale	1, 1, 1	22 × 1/Output Rate	24 × 1/Output Rate	Calibration on externally-applied input voltage with PGA set for selected input range. The input applied is assumed to be the full-scale of the system. This calibration should be preceded by a System Zero-Scale or Internal Zero-Scale calibration. The Gain Calibration Register for the selected channel is updated at the end of this calibration sequence.

CIRCUIT DESCRIPTION

The AD7731 is a sigma-delta A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low-frequency signals such as those in strain-gage, pressure transducer, temperature measurement, industrial control or process control applications. It contains a sigma-delta (or charge-balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bidirectional serial communications port. The part consumes 13.5 mA of power supply current with a standby mode which consumes only 20 μA. The part operates from a single +5 V supply. The clock source for the part can be provided via an external clock or by connecting a crystal oscillator or ceramic resonator across the MCLK IN or MCLK OUT pins.

The part contains three programmable-gain fully differential analog input channels which can be reconfigured as five pseudo-differential inputs. The part handles a total of seven different input ranges on all channels which are programmed via the on-chip registers. The differential unipolar ranges are: 0 mV to +20 mV through 0 V to +1.28 V and the differential bipolar ranges are: ±20 mV through ±1.28 V.

The AD7731 employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The sigma-delta modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A digital low-pass filter processes the output of the sigma-delta modulator and updates the data register at a rate that can be programmed over the serial interface. The output data from the part is accessed over this serial interface. The cutoff frequency and output rate of this filter can be programmed via on-chip registers. The output noise performance and peak-to-peak resolution of the part varies with gain and with the output rate as shown in Tables I to IV.

The analog inputs are buffered on-chip, allowing the part to handle significant source impedances on the analog input. This means that external R, C filtering (for noise rejection or RFI interference reduction) can be placed on the analog inputs if required. The common-mode voltage range for the analog inputs comes within 1.2 V of AGND and 0.95 V of AV_{DD}. The reference input is also differential and the common-mode range here is from AGND to AV_{DD}.

The AD7731 contains a number of hardware and software events that set or reset status flags and bits in registers. Table XVII summarizes which blocks and flags are affected by the different events.

Table XVII. Reset Events

Event	Set Registers to Default	Mode Bits	Filter Reset	Analog Power-Down	Reset Serial Interface	Set $\overline{\text{RDY}}$ Pin/Bit	Set $\overline{\text{STDY}}$ Bit
Power-On Reset	Yes	000	Yes	Yes	Yes	Yes	Yes
$\overline{\text{RESET}}$ Pin	Yes	000	Yes	No	Yes	Yes	Yes
$\overline{\text{STANDBY}}$ Pin	No	As Is	Yes	Yes	No	Yes	Yes
Mode 011 Write	No	011	Yes	Yes	No	Yes	Yes
$\overline{\text{SYNC}}$ Pin	No	As Is	Yes	No	No	Yes	Yes
Mode 000 Write	No	000	Yes	No	No	Yes	Yes
Conversion or Cal Mode Write	No	New Value	Initial Reset	No	No	Yes	Yes
Clock 32 1s	No	As Is	No	No	Yes	Yes	Yes
Data Register Read	No	As Is	No	No	No	Yes	No

ANALOG INPUT

Analog Input Channels

The AD7731 has six analog input pins (labelled AIN1 to AIN6) which can be configured as either three fully differential input channels or five pseudo-differential input channels. Bits CH0, CH1 and CH2 of the Mode Register configure the input channel arrangement and the channel selection is as outlined previously in Table XIII. The input pairs (either differential or pseudo-differential) provide programmable-gain, input channels which can handle either unipolar or bipolar input signals. It should be noted that the bipolar input signals are referenced to the respective AIN(–) input of the input pair. The AIN3 and AIN4 pins can also be reconfigured as two digital output port bits, also controlled by the Mode Register.

A differential multiplexer switches one of the two input channels to the on-chip buffer amplifier. When the analog input channel is switched, the $\overline{RDY}$ output goes high and the settling time of the part must elapse before a valid word from the new channel is available in the Data Register (indicated by $\overline{RDY}$ going low).

Buffered Inputs

The output of the multiplexer feeds into a high impedance input stage of the buffer amplifier. As a result, the analog inputs can handle significant source impedances. This buffer amplifier has an input bias current of 50 nA (CHP = 1) and 60 nA (CHP = 0). This current flows in each leg of the analog input pair. The offset current on the part is the difference between the input bias on the legs of the input pair. This offset current is less than 10 nA (CHP = 1) and 25 nA (CHP = 0). Large source resistances result in a dc offset voltage developed across the source resistance on each leg but matched impedances on the analog input legs will reduce the offset voltage to that generated by the input offset current.

Analog Input Ranges

The absolute input voltage range is restricted to between AGND + 1.2 V to AV_{DD} – 0.95 V which also places restrictions on the common-mode range. Care must be taken in setting up the common-mode voltage and input voltage range so that these limits are not exceeded, otherwise there will be a degradation in linearity performance.

In some applications, the analog input range may be biased either around system ground or slightly below system ground. In such cases, the AGND of the AD7731 must be biased negative with respect to system ground such that the analog input voltage does not go within 1.2 V of AGND. Care should taken to ensure that the differential between either AV_{DD} or DV_{DD} and this biased AGND does not exceed 5.5 V. This is discussed in more detail in the Applications section.

Programmable Gain Amplifier

The output from the buffer amplifier is applied to the input of the on-chip programmable gain amplifier (PGA). The PGA can handle seven different unipolar input ranges and seven bipolar ranges. With the HIREF bit of the Mode Register at 0 and a +2.5 V reference (or the HIREF bit at 1 and a +5 V reference), the unipolar ranges are 0 mV to +20 mV, 0 mV to +40 mV, 0 mV to +80 mV, 0 mV to +160 mV, 0 mV to +320 mV, 0 mV to +640 mV and 0 V to +1.28 V while the bipolar ranges are ±20 mV, ±40 mV, ±80 mV, ±160 mV, ±320 mV, ±640 mV, ±1.28 V. These are the nominal ranges which should appear at the input to the on-chip PGA.

Bipolar/Unipolar Inputs

The analog inputs on the AD7731 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the part can handle negative voltages with respect to system ground on its analog inputs unless the AGND of the part is also biased below system ground. Unipolar and bipolar signals on the AIN(+) input are referenced to the voltage on the respective AIN(–) input. For example, if AIN(–) is +2.5 V and the AD7731 is configured for an analog input range of 0 mV to +20 mV, the input voltage range on the AIN(+) input is +2.5 V to +2.52 V. If AIN(–) is +2.5 V and the AD7731 is configured for an analog input range of ±1.28 V, the analog input range on the AIN(+) input is +1.22 V to +3.78 V (i.e., 2.5 V ± 1.28 V).

Bipolar or unipolar options are chosen by programming the $\overline{B}$/U bit of the Mode Register. This programs the selected channel for either unipolar or bipolar operation. Programming the channel for either unipolar or bipolar operation does not change any of the input signal conditioning; it simply changes the data output coding and the points on the transfer function where calibrations occur. When the AD7731 is configured for unipolar operation, the output coding is natural (straight) binary with a zero differential voltage resulting in a code of 000...000, a midscale voltage resulting in a code of 100...000 and a full-scale input voltage resulting in a code of 111...111. When the AD7731 is configured for bipolar operation, the coding is offset binary with a negative full-scale voltage resulting in a code of 000...000, a zero differential voltage resulting in a code of 100...000 and a positive full-scale voltage resulting in a code of 111...111.

Burnout Currents

The AD7731 contains two 100 nA constant current generators, one source current from AV_{DD} to AIN(+) and one sink from AIN1(–) to AGND. The currents are switched to the selected analog input pair. Both currents are either on or off depending on the BO bit of the Mode Register. These currents can be used in checking that a transducer is still operational before attempting to take measurements on that channel. If the currents are turned on, allowed flow in the transducer, a measurement of the input voltage on the analog input taken and the voltage measured is full scale then it indicates that the transducer has gone open-circuit. If the voltage measured is 0 V, it indicates that the transducer has gone open-circuit. For normal operation, these burnout currents are turned off by writing a 0 to the BO bit. The current sources work over the normal absolute input voltage range specifications.

REFERENCE INPUT

The AD7731's reference inputs, REF IN(+) and REF IN(–), provide a differential reference input capability. The common-mode range for these differential inputs is from AGND to AV_{DD}. The nominal reference voltage, V_{REF} (REF IN(+) – REF IN(–)), for specified operation is +2.5 V with the HIREF bit at 0 and +5 V with the HIREF bit at 1. The part is also functional with V_{REF} of +2.5 V with the HIREF bit at 1. This results in a halving of all input ranges. The resolution in nV will be unaltered, but will be reduced by 1 bit in terms of peak-to-peak resolution.

Both reference inputs provide a high impedance, dynamic load. The typical average dc input leakage current is over temperature is 4.5 μA with HIREF = 0 and 8 μA with HIREF = 1. Because the input impedance on each reference input is dynamic, external resistance/capacitance combinations may result in gain errors on the part.

The output noise performance outlined in Tables I through IV is for an analog input of 0 V and is unaffected by noise on the reference. To obtain the same noise performance as shown in the noise tables over the full input range requires a low noise reference source for the AD7731. If the reference noise in the bandwidth of interest is excessive, it will degrade the performance of the AD7731. In applications where the excitation voltage for the transducer on the analog input also drives the reference voltage for the part, the effect of the low-frequency noise in the excitation voltage will be removed as the application is ratiometric. In this case, the reference voltage for the AD7731 and the excitation voltage for the transducer are the same. The HIREF bit of the Mode Register should be set to 1.

If the AD7731 is not used in a ratiometric application, a low noise reference should be used. Recommended reference voltage sources for the AD7731 include the AD780, REF43 and REF192. If any of these references are used as the reference source for the AD7731, the HIREF bit should be set to 0. It is generally recommended to decouple the output of these references to further reduce the noise level.

Reference Detect

The AD7731 includes on-chip circuitry to detect if the part has a valid reference for conversions or calibrations. If the voltage between the REF IN(+) and REF IN(–) pins goes below 0.3 V or either the REF IN(+) or REF IN(–) inputs is open circuit, the AD7731 detects that it no longer has a valid reference. In this case, the NOREF bit of the Status Register is set to a 1.

If the AD7731 is performing normal conversions and the NOREF bit becomes active, the part places all 1s in the Data Register. Therefore, it is not necessary to continuously monitor the status of the NOREF bit when performing conversions. It is only necessary to verify its status if the conversion result read from the Data Register is all 1s.

If the AD7731 is performing either an offset or gain calibration and the NOREF bit becomes active, the updating of the respective calibration register is inhibited to avoid loading incorrect coefficients to this register. If the user is concerned about verifying that a valid reference is in place every time a calibration is performed, then the status of the NOREF bit should be checked at the end of the calibration cycle.

SIGMA-DELTA MODULATOR

A sigma-delta ADC generally consists of two main blocks, an analog modulator and a digital filter. In the case of the AD7731, the analog modulator consists of a difference amplifier, an integrator block, a comparator and a feedback DAC as illustrated in Figure 7. In operation, the analog signal sample is fed to the difference amplifier along with the output of the feedback DAC. The difference between these two signals is integrated and fed to the comparator. The output of the comparator provides the input to the feedback DAC so the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. This duty cycle data can be recovered as a data word using the digital filter. The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (which results from the analog to digital conversion) so that the noise is pushed towards one half of the modulator frequency. The digital filter then bandlimits the response to a frequency significantly lower than one half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a bandlimited, low noise output from the AD7731.

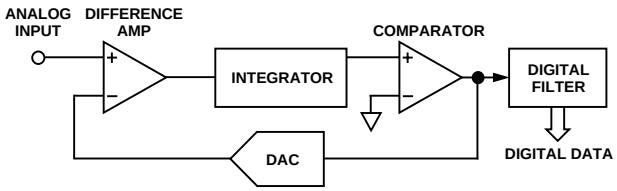


Figure 7. Sigma-Delta Modulator Block Diagram

DIGITAL FILTERING

Filter Architecture

The output of the modulator feeds directly into the digital filter. This digital filter consists of two portions, a first stage filter and a second stage filter. The cutoff frequency and output rate of the filter are programmable. The first stage filter is a low-pass, $sinc^3$ or $(sinx/x)^3$ filter whose primary function is to remove the quantization noise introduced at the modulator. The second stage filter has three distinct modes of operation. The first option is where it is bypassed completely such that the only filtering provided on the AD7731 is performed by the first stage $sinc^3$ filter. The second is where it provides a low-pass 22-tap FIR filter which processes the output of the first stage filter. The third option is to enable *FAST*Step™ mode. In this mode, when a step change is detected on the analog input or the analog input channel switched, the second stage filter enters a mode where it performs a variable number of averages for some time after the step change and then the second stage filter switches back to the FIR filter.

The AD7731 has two primary modes of operation, chop mode (CHP = 1) and nonchop mode (CHP = 0). The AD7731 alternatively reverses its inputs with CHP = 1, and alternate outputs from the first stage filter have a positive offset and negative offset term included. With CHP = 0, the input is never reversed and the output of the first stage filter includes an offset which is always of the same polarity.

The operation mode can be changed to achieve optimum performance in various applications. The CHP bit should generally be set to 0 when using the AD7731 in applications where higher throughput rates are a concern or in applications where the reduced rejection at the chopping frequency in chop mode is an issue. The part should be operated with CHP = 1 when drift, noise rejection and optimum EMI rejection are important criteria in the application.

The output update rate of the AD7731 is programmed using the SF bits of the Filter Register. With CHP = 0, the output update is determined by the relationship:

$$Output\ Rate = f_{MOD} \times \frac{1}{SF} \quad (CHP = 0)$$

where *SF* is the decimal equivalent of the data loaded to the SF bits of the Filter Register and f_{MOD} is the modulator frequency and is 1/16th of the master clock frequency.

With CHP = 1, the output update is determined by the relationship:

$$Output\ Rate = f_{MOD} \times \frac{1}{3 \times SF} \quad (CHP = 1)$$

where *SF* is the decimal equivalent of the data loaded to the SF bits of the Filter Register and f_{MOD} is the modulator frequency and is 1/16th of the master clock frequency.

Thus for a given SF word the output rate from the AD7731 is three times faster with CHP = 0 than CHP = 1.

The various filter stages and options are discussed in the following sections.

First Stage Filter/SKIP Mode Enabled (SKIP = 1)
With SKIP mode enabled, the only filtering on the part is the first stage filter. The frequency response for this first stage filter is shown in Figure 8. The response of this first stage filter is similar to that of an averaging filter but with a sharper roll-off. With CHP = 0, the output rate for the filter corresponds with the positioning of the first notch of the filter's frequency response. Thus, for the plot of Figure 8 where the output rate is 600 Hz ($f_{CLK\ IN}$ = 4.9152 MHz and SF = 512), the first notch of the filter is at 600 Hz. With CHP = 1, the magnitude response is the same as in Figure 8 but in this case, the output rate is 1/3rd the output rate so for the example shown in Figure 8 the output data rate is 200 Hz. The notches of this $sinc^3$ filter frequency response are repeated at multiples of the first notch. The filter provides attenuation of better than 100 dB around these notches. Programming a different cutoff frequency via SF0 – SF11 does not alter the profile of the filter response; it simply changes the location of the notches. The –3 dB frequency for both Chop and Nonchop modes is defined as:

$$f_{3\,dB} = 0.262 \times f_{MOD} \times \frac{1}{SF}$$

Nonchop Mode (SKIP = 1, CHP = 0)
With CHP = 0, the input chopping on the AD7731 is disabled and any offset content in the samples to the first stage filter are all of the same polarity. When using the part in SKIP mode, the user can take the output from the AD7731 directly. Time to the first output for the part is 3 × 1/Output Rate in this mode. Table XVIII summarizes the settling time and subsequent throughput rate for the various different modes.

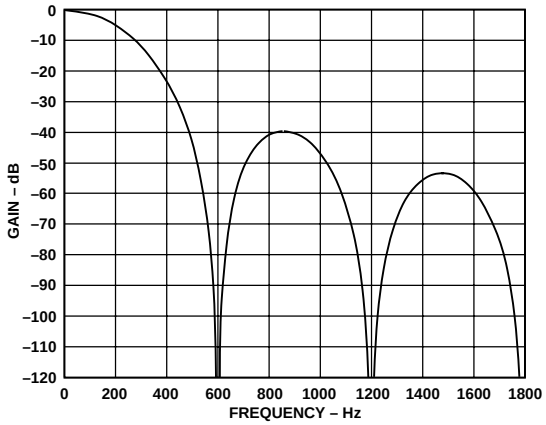


Figure 8. SKIP Mode Frequency Response (SKIP = 1, SF = 512)

Chop Mode (SKIP = 1, CHP = 1)
With CHP = 1, the AD7731 alternatively reverses the ADC inputs, producing an output which contains the channel offset when not reversed and the negative of the offset when reversed. As a result, when operating in SKIP mode, the user has to take two subsequent outputs from the AD7731 and average them to produce a valid output from the first stage filter. While operating in this mode gives the benefits of chopping without the longer settling time associated with the 22-tap FIR filter, care should be taken with input signals near positive full-scale or negative full-scale (zero-scale in unipolar mode). Since the calibration coefficients are generated for the averaged offset, and not for the individual offsets represented in each sample, one of the two samples in the pair may record an all 1s or all 0s reading. If this happens it will result in an error in the averaged reading. Time to first output for the part is 1/Output Rate in this mode. However, since the user really needs two outputs to derive a correct chopped result, the time to get two outputs for averaging is 2 × 1/Output Rate. Table XVIII summarizes the settling time and subsequent throughput rate for the various different modes. If the user wants the benefits of chopping without the longer settling time associated with the 22-tap FIR filter, it is recommended that the part be used in *FAST*Step™ mode.

Second Stage Filter
With SKIP mode disabled, the second stage filter is included in the signal processing. This second stage filter produces a different response depending on the CHP and FAST bits.

Normal FIR Operation (SKIP = 0)
The normal mode of operation of the second stage filter is as a 22-tap low-pass FIR filter. This second stage filter processes the output of the first stage filter and the net frequency response of the filter is simply a product of the filter response of both filters. The overall filter response of the AD7731 is guaranteed to have no overshoot.

Chop Mode (SKIP = 0, CHP = 1)
With CHOP mode enabled and SKIP mode disabled, the second stage filter is presented with alternating first stage filter outputs and processes data accordingly. It has two primary functions. One is to set the overall frequency response and the second is to eliminate the modulated offset effect which appears on the output of the first stage filter. Time to first output is 22 × 1/Output Rate in this mode. Table XVIII summarizes the settling time and subsequent throughput rate for the various different modes.

Figure 9 shows the full frequency response of the AD7731 when the second stage filter is set for normal FIR operation. This response is for chop mode enabled with the decimal equivalent of the word in the SF bits set to 512 and a master clock frequency of 4.9152 MHz. The response will scale proportionately with master clock frequency. The response is shown from dc to 100 Hz. The rejection at 50 Hz ± 1 Hz and 60 Hz ± 1 Hz is better than 88 dB.

The –3 dB frequency for the frequency response of the AD7731 with the second stage filter set for normal FIR operation and chop mode enabled is determined by the following relationship:

$$f_{3dB} = 0.0395 \times f_{MOD} \times \frac{1}{3 \times SF} \left(CHP = 1\right)$$

In this case, f_{3dB} = 7.9 Hz and the stop-band, where the attenuation is greater than 64.5 dB, is determined by:

$$f_{STOP} = 0.14 \times f_{MOD} \times \frac{1}{3 \times SF} \quad \left(CHP = 1\right)$$

In this case, f_{STOP} = 28 Hz.

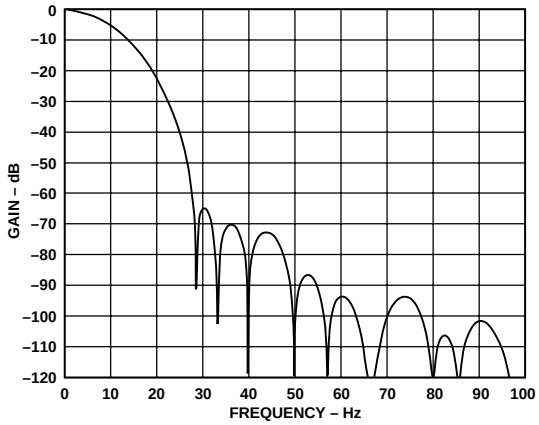


Figure 9. Detailed Full Frequency Response of AD7731 (SKIP = 0, CHP = 1, SF = 512)

Figure 10 shows the frequency response for the same set of conditions as for Figure 9 but in this case the response in shown out to 600 Hz. This response shows that the attenuation of input frequencies close to 200 Hz and 400 Hz is significantly less than at other input frequencies. These "peaks" in the frequency response are a by-product of the chopping of the input. The plot of Figure 10 is the amplitude for different input frequencies. Note that because the output rate is 200 Hz for the conditions under which Figure 10 is plotted, if something existed in the input frequency domain at 200 Hz, it would be aliased and appear in the output frequency domain at dc.

Because of this effect, care should be taken in choosing an output rate which is close to the line frequency in the application. For example, if the line frequency is 50 Hz, an output update rate of 50 Hz should not be chosen as it will significantly reduce the AD7731's line frequency rejection (the 50 Hz will appear as a dc component with only 6 dB attenuation). However, choosing 60 Hz as the output rate (SF = 1707) will give better than 90 dB attenuation of the aliased line frequency. In a similar fashion, if the line frequency is 60 Hz, it is recommended that the user choose an output update rate of 50 Hz (SF = 2048).

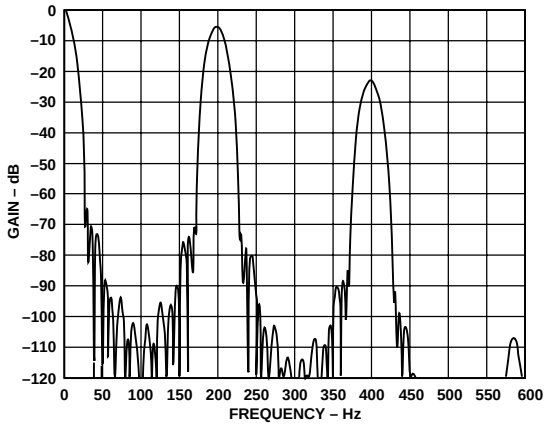


Figure 10. Expanded Full Frequency Response of AD7731 (SKIP = 0, CHP = 1, SF = 512)

Similarly, multiples of the line frequency should be avoided as the output rate because harmonics of the line frequency will not be fully attenuated. The programmability of the AD7731's output rate should allow the user to readily choose an output rate which overcomes this issue. An alternative is to use the part in nonchop mode.

Nonchop Mode (SKIP = 0, CHP = 0)

With CHOP mode disabled and SKIP mode disabled, the only function of the second stage filter is to give the overall frequency response. Figure 11 shows the frequency response for the AD7731 with the second stage filter is set for normal FIR operation, chop mode disabled, the decimal equivalent of the word in the SF bits set to 1536 and a master clock frequency of 4.9152 MHz. The response is analogous to that of Figure 9 with the three-times larger SF word producing the same 200 Hz output rate. Once again, the response will scale proportionally with master clock frequency. The response is shown from dc to 100 Hz. The rejection at 50 Hz ± 1 Hz and 60 Hz ± 1 Hz is better than 88 dB.

The –3 dB frequency for the frequency response of the AD7731 with the second stage filter set for normal FIR operation and chop mode enabled is determined by the following relationship:

$$f_{3\,dB} = 0.039 \times f_{MOD} \times \frac{1}{SF} \quad (CHP = 0)$$

In this case, $f_{3\,dB}$ = 7.8 Hz and the stop-band, where the attenuation is greater than 64.5 dB, is determined by:

$$f_{STOP} = 0.14 \times f_{MOD} \times \frac{1}{SF} \quad (CHP = 0)$$

In this case, f_{STOP} = 28 Hz.

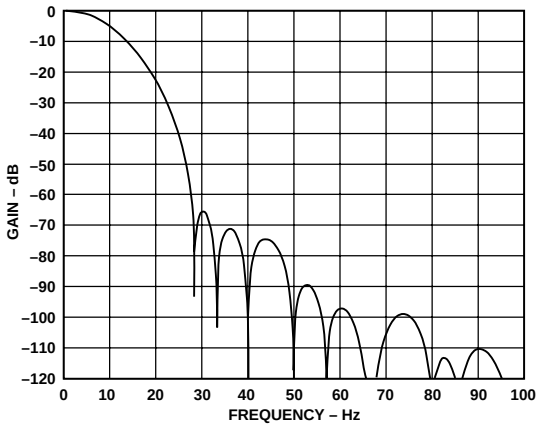


Figure 11. Detailed Full Frequency Response of AD7731 (SKIP = 0, CHP = 0, SF = 1536)

Figure 12 shows the frequency response for the same set of conditions as for Figure 11 but in this case the response in shown out to 600 Hz. This plot is comparable to that of Figure 10. The most notable difference is absence of the peaks in the response at 200 Hz and 400 Hz. As a result, interference at these frequencies will be effectively eliminated before being aliased back to dc.

Table XVIII summarizes the settling time and subsequent throughput rate for the various different modes.

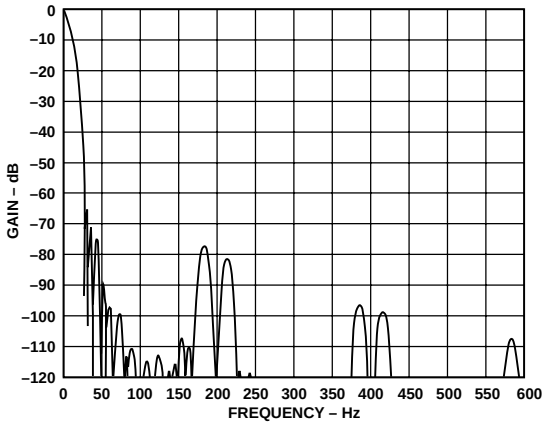


Figure 12. Expanded Full Frequency Response of AD7731 (SKIP = 0, CHP = 0, SF = 1536)

***FAST*Step™ Mode (SKIP = 0, FAST = 1)**

The second mode of operation of the second stage filter is in *FAST*Step™ mode which enables it to respond rapidly to step inputs even when the second stage filter is in the loop. The *FAST*Step™ mode is not relevant with SKIP mode enabled. The *FAST*Step™ mode is enabled by placing a 1 in the FAST bit of the Filter Register. If the FAST bit is 0, the part continues to process step inputs with the normal FIR filter as the second stage filter. With *FAST*Step™ mode enabled, the second stage filter will continue to process steady state inputs with the filter in its normal FIR mode of operation. However, the part is continuously monitoring the output of the first stage filter and comparing it with the second-previous output. If the difference between these two outputs is greater than a predetermined threshold (1% of full scale), the second stage filter switches to a simple moving average computation. This also happens when a change in channels takes place regardless of how close the voltages on the two channels are. When the change is detected, the $\overline{\text{STDY}}$ bit of the Status Register goes to 1.

The initial number of averages in the moving average computation is either 2 (chop enabled) or 1 (chop disabled). The number of averages will be held at this value as long as the threshold is exceeded. Once the threshold is no longer exceeded (the step on the analog input has settled), the number of outputs used to compute the moving average output is increased. The first and second outputs from the first stage filter where the threshold is no longer exceeded is computed as an average by 2, then 4 outputs with an average of 4, 8 outputs with an average of 8 and 6 outputs with an average of 16. At this time, the second stage filter reverts back to its normal FIR mode of operation. When the second stage filter reverts back to the normal FIR, the $\overline{\text{STDY}}$ bit of the Status Register goes to 0.

Figure 13 gives an indication of the different responses to a step input with *FAST*Step™ mode enabled and disabled. The vertical axis indicates the settling of the output to the input step change while the horizontal axis shows how many outputs it takes for that settling to occur. The positive input step change occurs at a time coincident with the fifth output.

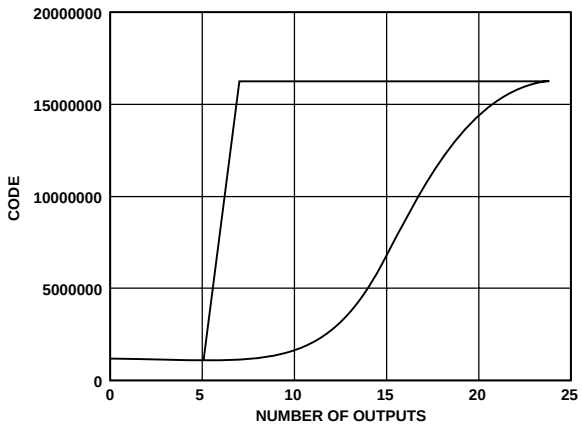


Figure 13. Step Response for FASTStep™ and Normal Operation

In *FAST*Step™ mode, the part has settled to the new value much faster. For example, with CHP = 1, the *FAST*Step™ mode settles to its value in two outputs while the normal mode settling takes 23 outputs. Between the second and 23rd output, the *FAST*Step™ mode produces a settled result but with additional noise compared to the specified noise level for its operating conditions. This noise level starts at approximately 3 times the final noise converging to FIR mode performance. The complete settling time to where the part is back within the specified noise number, is the same for *FAST*Step™ mode and for normal mode. When switching channels, the profile of Figure 13 will not be seen. Since the part is synchronized when a channel change takes place, it will not produce an output until the filter (either *FAST*Step™ or FIR) is settled. Table XVIII gives an indication of the faster settling time benefits of *FAST*Step™ mode.

As can be seen from Table XVIII, the *FAST*Step™ mode gives a much earlier indication of where the output channel is going and what its new value is. This feature is very useful in scanning multiple channels where the user does not have to wait for the FIR settling time to see if a channel has changed value. In this case, the part can be set up with CHP = 1, SKIP = 0 and FAST = 1. This takes advantage of the low drift, better noise immunity benefits of the CHOP mode. When a change in channels takes place, the part enters *FAST*Step™ mode and provides an output result in 2 × 1/Output Rate.

Note, if the FAST bit is set and the part operated in single conversion mode, the AD7731 will continue to output results until the $\overline{\text{STDY}}$ bit goes to 0.

Table XVIII. Time to First and Subsequent Outputs Following Channel Change

SKIP	CHP	FAST	Time to First O/P[1]	Time to Subsequent O/Ps
0	0	0	$24 \times SF/f_{MOD}$	SF/f_{MOD}
0	1	0	$66 \times SF/f_{MOD}$	$3 \times SF/f_{MOD}$
1	0	X[2]	$3 \times SF/f_{MOD}$	SF/f_{MOD}
1	1	X	$3 \times SF/f_{MOD}$	$3 \times SF/f_{MOD}$
0	0	1	$3 \times SF/f_{MOD}$	SF/f_{MOD}
0	1	1	$6 \times SF/f_{MOD}$	$3 \times SF/f_{MOD}$

[1]This O/P is fully settled.
[2]X = Don't Care.

CALIBRATION

The AD7731 provides a number of calibration options that can be programmed via the MD2, MD1 and MD0 bits of the Mode Register. The different calibration options are outlined in the Mode Register and Calibration Operations sections. A calibration cycle may be initiated at any time by writing to these bits of the Mode Register. Calibration on the AD7731 removes offset and gain errors from the device.

The AD7731 gives the user access to the on-chip calibration registers allowing the microprocessor to read the device's calibration coefficients and also to write its own calibration coefficients to the part from prestored values in E^2PROM. This gives the microprocessor much greater control over the AD7731's calibration procedure. It also means that by comparing the coefficients after calibration with prestored values in E^2PROM, the user can verify that the device has correctly performed its calibration. The values in these calibration registers are 24 bits wide. In addition, the span and offset for the part can be adjusted by the user.

Internally in the AD7731, the coefficients are normalized before being used to scale the words coming out of the digital filter. The offset calibration register contains a value which, when normalized, is subtracted from all conversion results. The gain calibration register contains a value which, when normalized, is multiplied by all conversion results. The offset calibration coefficient is subtracted from the result prior to the multiplication by the gain coefficient.

The AD7731 offers self-calibration or system calibration facilities. For full calibration to occur on the selected channel, the on-chip microcontroller must record the modulator output for two different input conditions. These are "zero-scale" and "full-scale" points. These points are derived by performing a conversion on the different input voltages provided to the input of the modulator during calibration. The result of the "zero-scale" calibration conversion is stored in the Offset Calibration Register for the appropriate channel. The result of the "full-scale" calibration conversion is stored in the Gain Calibration Register for the appropriate channel. With these readings, the microcontroller can calculate the offset and the gain slope for the input-to-output transfer function of the converter. Internally, the part works with 33 bits of resolution to determine its conversion result of either 16 bits or 24 bits.

The sequence in which the zero-scale and full-scale calibration occurs depends upon the type of full-scale calibration being performed. The internal full-scale calibration is a two-step calibration that alters the value of the Offset Calibration Register. Thus, the user *must* perform a zero-scale calibration (either internal or system) after an internal full-scale calibration to correct the Offset Calibration Register contents. When using system full-scale calibration, it is recommended that the zero-scale calibration (either internal or system) is performed first.

Calibration time is the same regardless of whether the SKIP mode is enabled or not. This is because the SKIP bit is ignored and the second stage filter is included in the calibration cycle. This is done to derive more accurate calibration coefficients. If the subsequent operating mode is with CHP = 0, the calibration should be performed with CHP = 0 so the offset calibration coefficient and the subsequent conversion offsets are consistent. Since the calibration coefficients are derived by performing a conversion on the input voltage provided, the accuracy of the calibration can only be as good as the noise level which the part provides in normal mode. To optimize the calibration accuracy, it is recommended to calibrate the part at its lowest output rate where the noise level is lowest. The coefficients generated at any output update rate will be valid for all selected output update rates. This scheme of calibrating at the lowest output update rate does mean that the duration of calibration is longer.

Internal Zero-Scale Calibration

An internal zero-scale calibration is initiated on the AD7731 by writing the appropriate values (1, 0, 0) to the MD2, MD1 and MD0 bits of the Mode Register. In this calibration mode with a unipolar input range, the zero-scale point used in determining the calibration coefficients is with the inputs of the differential pair internally shorted on the part (i.e., AIN[+] = AIN[–] = Externally-Applied AIN[–] voltage). The PGA is set for the selected gain (as per the RN2, RN1, RN0 bits in the Mode Register) for this internal zero-scale calibration conversion.

The duration time of the calibration depends upon the CHP bit of the Filter Register. With CHP = 1, the duration is $22 \times 1/$ Output Rate; with CHP = 0, the duration is $24 \times 1/$Output Rate. At this time the MD2, MD1 and MD0 bits in the Mode Register return to 0, 0, 0 (Sync or Idle Mode for the AD7731). The $\overline{RDY}$ line goes high when calibration is initiated and returns low when calibration is complete. Note, the part has not performed a conversion at this time; it has simply performed a zero-scale calibration and updated the Offset Calibration Register for the selected channel. The user must write either 0, 0, 1 or 0, 1 ,0 to the MD2, MD1, MD0 bits of the Mode Register to initiate a conversion. If $\overline{RDY}$ is low before (or goes low during) the calibration command write to the Mode Register, it may take up to one modulator cycle (MCLK IN/16) before $\overline{RDY}$ goes high to indicate that calibration is in progress. Therefore, $\overline{RDY}$ should be ignored for up to one modulator cycle after the last bit of the calibration command is written to the Mode Register.

For bipolar input ranges in the internal zero-scale calibrating mode, the sequence is very similar to that just outlined. In this case, the zero-scale point is exactly the same as above but since the part is configured for bipolar operation, the output code for zero differential input is 800000 Hex in 24-bit mode.

The internal zero-scale calibration needs to be performed as one part of a two-step full calibration. However, once a full calibration has been performed, additional internal zero-scale calibrations can be performed by themselves to adjust the part's zero-scale point only. When performing a two-step full calibration, care should be taken as to the sequence in which the two steps are performed. If the internal zero-scale calibration is one part of a full self-calibration, then it should take place after an internal full-scale calibration. If it takes place in association with a system full-scale calibration, then this internal zero-scale calibration should be performed first.

Internal Full-Scale Calibration

An internal full-scale calibration is initiated on the AD7731 by writing the appropriate values (1, 0, 1) to the MD2, MD1 and MD0 bits of the Mode Register. In this calibration mode, the full-scale point used in determining the calibration coefficients is with an internally-generated full-scale voltage. This full-scale voltage is derived from the reference voltage for the AD7731 and the PGA is set for the selected gain (as per the RN2, RN1, RN0 bits in the Mode Register) for this internal full-scale calibration conversion.

Normally, the internal full-scale calibration is performed at the required operating output range. When operating with a 20 mV or 40 mV input range, it is recommended that internal full-scale calibrations are performed on the 80 mV input range.

The internal full-scale calibration is a two-step sequence which runs when an internal full-scale calibration command is written to the AD7731. One part of the calibration is a zero-scale calibration and as a result, the contents of the Offset Calibration Register are altered during this Internal Full-Scale Calibration. The user must, therefore, perform a zero-scale calibration (either internal or system) AFTER the internal full-scale calibration. This means that internal full-scale calibrations cannot be performed in isolation.

The duration time of the calibration depends upon the CHP bit of the Filter Register. With CHP = 1, the duration is 44 × 1/Output Rate; with CHP = 0, the duration is 48 × 1/Output Rate. At this time the MD2, MD1 and MD0 bits in the Mode Register return to 0, 0, 0 (Sync or Idle Mode for the AD7731). The $\overline{RDY}$ line goes high when calibration is initiated and returns low when calibration is complete. Note, the part has not performed a conversion at this time. The user must write either 0, 0, 1 or 0, 1, 0 to the MD2, MD1, MD0 bits of the Mode Register to initiate a conversion. If $\overline{RDY}$ is low before (or goes low during) the calibration command write to the Mode Register, it may take up to one modulator cycle (MCLK IN/16) before $\overline{RDY}$ goes high to indicate that calibration is in progress. Therefore, $\overline{RDY}$ should be ignored for up to one modulator cycle after the last bit of the calibration command is written to the Mode Register.

System Zero-Scale Calibration

System calibration allows the AD7731 to compensate for system gain and offset errors as well as its own internal errors. System calibration performs the same slope factor calculations as self-calibration but uses voltage values presented by the system to the AIN inputs for the zero- and full-scale points.

A system zero-scale calibration is initiated on the AD7731 by writing the appropriate values (1, 1, 0) to the MD2, MD1 and MD0 bits of the Mode Register. In this calibration mode with a unipolar input range, the zero-scale point used in determining the calibration coefficients is the bottom end of the transfer function. The system's zero-scale point is applied to the AD7731's AIN input before the calibration step and this voltage must remain stable for the duration of the system zero-scale calibration. The PGA is set for the selected gain (as per the RN2, RN1, RN0 bits in the Mode Register) for this system zero-scale calibration conversion. The allowable range for the system zero-scale voltage is discussed in the Span and Offsets Section.

The duration time of the calibration depends upon the CHP bit of the Filter Register. With CHP = 1, the duration is 22 × 1/Output Rate; with CHP = 0, the duration is 24 × 1/Output Rate. At this time the MD2, MD1 and MD0 bits in the Mode Register return to 0, 0, 0 (Sync or Idle Mode for the AD7731). The $\overline{RDY}$ line goes high when calibration is initiated and returns low when calibration is complete. Note, the part has not performed a conversion at this time; it has simply performed a zero-scale calibration and updated the Offset Calibration Register for the selected channel. The user must write either 0, 0, 1 or 0, 1, 0 to the MD2, MD1, MD0 bits of the Mode Register to initiate a conversion. If $\overline{RDY}$ is low before (or goes low during) the calibration command write to the Mode Register, it may take up to one modulator cycle (MCLK IN/16) before $\overline{RDY}$ goes high to indicate that calibration is in progress. Therefore, $\overline{RDY}$ should be ignored for up to one modulator cycle after the last bit of the calibration command is written to the Mode Register.

For bipolar input ranges in the system zero-scale calibrating mode, the sequence is very similar to that just outlined. In this case, the zero-scale point is the mid-point of the AD7731's transfer function.

The system zero-scale calibration needs to be performed as one part of a two part full calibration. However, once a full calibration has been performed, additional system zero-scale calibrations can be performed by themselves to adjust the part's zero-scale point only. When performing a two-step full calibration, care should be taken as to the sequence in which the two steps are performed. If the system zero-scale calibration is one part of a full system calibration, it should take place before a system full-scale calibration. If it takes place in association with an internal full-scale calibration, this system zero-scale calibration should be performed after the full-scale calibration.

System Full-Scale Calibration

A system full-scale calibration is initiated on the AD7731 by writing the appropriate values (1, 1, 1) to the MD2, MD1 and MD0 bits of the Mode Register. System full-scale calibration is performed using the system's positive full-scale voltage. This full-scale voltage must be set up before the calibration is initiated, and it must remain stable throughout the calibration step. The system full-scale calibration is performed at the selected gain (as per the RN2, RN1, RN0 bits in the Mode Register).

The duration time of the calibration depends upon the CHP bit of the Filter Register. With CHP = 1, the duration is 22 × 1/Output Rate; with CHP = 0, the duration is 24 × 1/Output Rate. At this time the MD2, MD1 and MD0 bits in the Mode Register return to 0, 0, 0 (Sync or Idle Mode for the AD7731). The $\overline{RDY}$ line goes high when calibration is initiated and returns low when calibration is complete. Note, the part has not performed a conversion at this time; it has simply performed a full-scale calibration and updated the Gain Calibration Register for the selected channel. The user must write either 0, 0, 1 or 0, 1, 0 to the MD2, MD1, MD0 bits of the Mode Register to initiate a conversion. If $\overline{RDY}$ is low before (or goes low during) the calibration command write to the Mode Register, it may take up to one modulator cycle (MCLK IN/16) before $\overline{RDY}$ goes high to indicate that calibration is in progress. Therefore, $\overline{RDY}$ should be ignored for up to one modulator cycle after the last bit of the calibration command is written to the Mode Register.

The system full-scale calibration needs to be performed as one part of a two part full calibration. However, once a full calibration has been performed, additional system full-scale calibrations can be performed by themselves to adjust the part's gain calibration point only. When performing a two-step full calibration, care should be taken as to the sequence in which the two steps are performed. A system full-scale calibration should not be carried out unless the part contains valid zero-scale coefficients. Therefore, an internal zero-scale calibration or a system zero-scale calibration must be performed before the system full-scale calibration when a full two-step calibration operation is being performed.

Span and Offset Limits

Whenever a system calibration mode is used, there are limits on the amount of offset and span that can be accommodated. The overriding requirement in determining the amount of offset and gain that can be accommodated by the part is the requirement that the positive full-scale calibration limit is ≤ 1.05 × FS, where FS is 20 mV through 1.28 V depending on the RN2, RN1, RN0 bits in the Mode Register. This allows the input range to go 5% above the nominal range. The built-in headroom in the AD7731's analog modulator ensures that the part will still operate correctly with a positive full-scale voltage that is 5% beyond the nominal.

The range of input span in both the unipolar and bipolar modes has a minimum value of 0.8 × FS and a maximum value of 2.1 × FS. However, the span (which is the difference between the bottom of the AD7731's input range and the top of its input range) has to take into account the limitation on the positive full-scale voltage. The amount of offset which can be accommodated depends on whether the unipolar or bipolar mode is being used. Once again, the offset has to take into account the limitation on the positive full-scale voltage. In unipolar mode, there is considerable flexibility in handling negative (with respect to AIN[–]) offsets. In both unipolar and bipolar modes, the range of positive offsets that can be handled by the part depends on the selected span. Therefore, in determining the limits for system zero-scale and full-scale calibrations, the user has to ensure that the offset range plus the span range does not exceed 1.05 × FS. This is best illustrated by looking at a few examples.

If the part is used in unipolar mode with a required span of 0.8 × FS, the offset range the system calibration can handle is from –1.05 × FS to +0.25 × FS. If the part is used in unipolar mode with a required span of FS, the offset range the system calibration can handle is from –1.05 × FS to +0.05 × FS. Similarly, if the part is used in unipolar mode and required to remove an offset of 0.2 × FS, the span range the system calibration can handle is 0.85 × FS.

If the part is used in bipolar mode with a required span of ±0.4 × FS, the offset range the system calibration can handle is from –0.65 × FS to +0.65 × FS. If the part is used in bipolar mode with a required span of ±FS, the offset range the system calibration can handle is from –0.05 × FS to +0.05 × FS. Similarly, if the part is used in bipolar mode and required to remove an offset of ±0.2 × FS, the span range the system calibration can handle is ±0.85 × FS. Figure 14 summarizes the span and offset ranges.

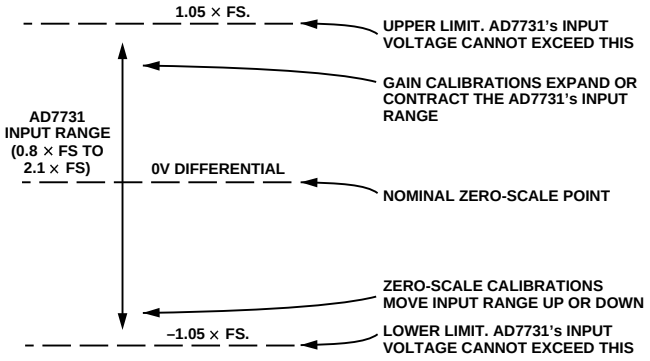


Figure 14. Span and Offset Limits

Power-Up and Calibration

On power-up, the AD7731 performs an internal reset that sets the contents of the internal registers to a known state. There are default values loaded to all registers after a power-on or reset. The default values contain nominal calibration coefficients for the calibration registers. However, to ensure correct calibration for the device, a calibration routine should be performed after power-up.

The power dissipation and temperature drift of the AD7731 are low and no warm-up time is required before the initial calibration is performed. However, if an external reference is being used, this reference must have stabilized before calibration is initiated. Similarly, if the clock source for the part is generated from a crystal or resonator across the MCLK pins, the start-up time for the oscillator circuit should elapse before a calibration is initiated on the part (see below).

Drift Considerations

The AD7731 uses chopper stabilization techniques to minimize input offset drift. Charge injection in the analog multiplexer and dc leakage currents at the analog input are the primary sources of offset voltage drift in the part. The dc input leakage current is essentially independent of the selected gain. Gain drift within the converter depends primarily upon the temperature tracking of the internal capacitors. It is not affected by leakage currents.

When operating the part in CHOP mode (CHP = 1), the signal chain including the first-stage filter is chopped. This chopping reduces the overall offset drift to 5 nV/°C. When operating in CHOP mode, it is recommended to calibrate the AD7731 only after power-up or reset to achieve the optimum drift performance from the part. Integral and differential linearity errors are not significantly affected by temperature changes.

Care must also be taken with external drift effects in order to achieve optimum drift performance. The user has to be especially careful to avoid, as much as possible, thermocouple effects from junctions of different materials. Devices should not be placed in sockets when evaluating temperature drift, there should be no links in series with the analog inputs and care must be taken as to how the input voltage is applied to the input pins. The true offset drift of the AD7731 itself can be evaluated by performing temperature drift testing of the part with the AIN(–)/AIN(–) input channel arrangement (i.e., internal shorted input, test mode).

USING THE AD7731

Clocking and Oscillator Circuit

The AD7731 requires a master clock input, which may be an external CMOS compatible clock signal applied to the MCLK IN pin with the MCLK OUT pin left unconnected. Alternatively, a crystal or ceramic resonator of the correct frequency can be connected between MCLK IN and MCLK OUT in which case the clock circuit will function as an oscillator, providing the clock source for the part. The input sampling frequency, the modulator sampling frequency, the –3 dB frequency, output update rate and calibration time are all directly related to the master clock frequency, $f_{CLK\ IN}$. Reducing the master clock frequency by a factor of 2 will halve the above frequencies and update rate and double the calibration time.

The crystal or ceramic resonator is connected across the MCLK IN and MCLK OUT pins, as per Figure 15*. When using a master clock frequency of 4.9152 MHz, C1 and C2 should both have a value equal to 33 pF.

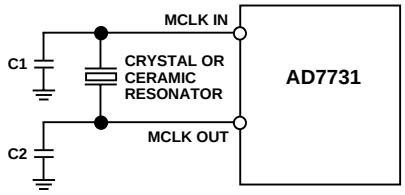


Figure 15. Crystal/Resonator Connections

The on-chip oscillator circuit also has a start-up time associated with it before it has attained its correct frequency and correct voltage levels. The typical start-up time for the circuit is 6 ms with a DV_{DD} of +5 V and 8 ms with a DV_{DD} of +3 V.

The AD7731's master clock appears on the MCLK OUT pin of the device. The maximum recommended load on this pin is one CMOS load. When using a crystal or ceramic resonator to generate the AD7731's clock, it may be desirable to then use this clock as the clock source for the system. In this case, it is recommended that the MCLK OUT signal is buffered with a CMOS buffer before being applied to the rest of the circuit.

System Synchronization

The $\overline{\text{SYNC}}$ input allows the user to reset the modulator and digital filter without affecting any of the setup conditions on the part. This allows the user to start gathering samples of the analog input from a known point in time, i.e., the rising edge of $\overline{\text{SYNC}}$.

If multiple AD7731s are operated from a common master clock, they can be synchronized to update their output registers simultaneously. A falling edge on the $\overline{\text{SYNC}}$ input resets the digital filter and analog modulator and places the AD7731 into a consistent, known state. While the $\overline{\text{SYNC}}$ input is low, the AD7731 will be maintained in this state. On the rising edge of $\overline{\text{SYNC}}$, the modulator and filter are taken out of this reset state and on the next clock edge the part again starts to gather input samples. In a system using multiple AD7731s, a common signal to their $\overline{\text{SYNC}}$ inputs will synchronize their operation. This would normally be done after each AD7731 has performed its own calibration or has had calibration coefficients loaded to it. The output updates will then be synchronized with the maximum possible difference between the output updates of the individual AD7731s being one MCLK IN cycle.

Single-Shot Conversions

The $\overline{\text{SYNC}}$ input can also be used as a start convert command allowing the AD7731 to be operated in a conventional converter fashion. In this mode, the rising edge of $\overline{\text{SYNC}}$ starts conversion and the falling edge of $\overline{\text{RDY}}$ indicates when conversion is complete. The disadvantage of this scheme is that the settling time of the filter has to be taken into account for every data register update.

Writing 0, 1, 0 to the MD2, MD1, MD0 bits of the Mode register has the same effect. This initiates a single conversion on the AD7731 with the part returning to idle mode at the end of conversion. Once again, the full settling time of the filter has to elapse before the Data Register is updated.

Note, if the FAST bit is set and the part operated in single conversion mode, the AD7731 will continue to output results until the $\overline{\text{STDY}}$ bit goes to 0.

Reset Input

The $\overline{\text{RESET}}$ input on the AD7731 resets all the logic, the digital filter and the analog modulator while all on-chip registers are reset to their default state. $\overline{\text{RDY}}$ is driven high and the AD7731 ignores all communications to any of its registers while the $\overline{\text{RESET}}$ input is low. When the $\overline{\text{RESET}}$ input returns high, the AD7731 starts to process data and $\overline{\text{RDY}}$ will return low after the filter has settled indicating a valid new word in the data register. However, the AD7731 operates with its default setup conditions after a $\overline{\text{RESET}}$ and it is generally necessary to set up all registers and carry out a calibration after a $\overline{\text{RESET}}$ command.

The AD7731's on-chip oscillator circuit continues to function even when the $\overline{\text{RESET}}$ input is low. The master clock signal continues to be available on the MCLK OUT pin. Therefore, in applications where the system clock is provided by the AD7731's clock, the AD7731 produces an uninterrupted master clock during $\overline{\text{RESET}}$ commands.

Standby Mode

The $\overline{\text{STANDBY}}$ input on the AD7731 allows the user to place the part in a power-down mode when it is not required to provide conversion results. The part can also be placed in its standby mode by writing 0, 1, 1 to the MD2, MD1, MD0 bits of the Mode Register. The AD7731 retains the contents of all its on-chip registers (including the Data Register) while in standby mode. Data can still be read from the part in Standby Mode. The STBY bit of the Status Register indicates whether the part is in standby or normal operating mode. When the $\overline{\text{STANDBY}}$ pin is taken high, the part returns to operating as it had been prior to the $\overline{\text{STANDBY}}$ pin going low.

The $\overline{\text{STANDBY}}$ input (or 0, 1, 1 in the MD2, MD1, MD0 bits) does not affect the digital interface. It does, however, set the $\overline{\text{RDY}}$ bit and pin high and also sets the $\overline{\text{STDY}}$ bit high. When $\overline{\text{STANDBY}}$ goes high again, $\overline{\text{RDY}}$ and $\overline{\text{STDY}}$ remain high until set low by a conversion or calibration.

*The AD7731 has a capacitance of 5 pF on MCLK IN and 13 pF on MCLK OUT.

Placing the part in standby mode reduces the total current to 10 μA typical when the part is operated from an external master clock, provided this master clock is stopped. If the external clock continues to run in standby mode, the standby current increases to 400 μA typical. If a crystal or ceramic resonator is used as the clock source, then the total current in standby mode is 400 μA typical. This is because the on-chip oscillator circuit continues to run when the part is in its standby mode. This is important in applications where the system clock is provided by the AD7731's clock, so that the AD7731 produces an uninterrupted master clock even when it is in its standby mode.

Digital Outputs

The AD7731 has two digital output pins, D0 and D1. When the DEN bit of the Mode Register is set to 1, these digital outputs assume the logic status of bits D0 and D1 of the Mode Register. It gives the user access to two digital port pins which can be programmed over the normal serial interface of the AD7731. The two outputs obtain their supply voltage from AV_{DD}, thus the outputs operate to 5 V levels even in cases where DV_{DD} = +3 V.

POWER SUPPLIES

There is no specific power sequence required for the AD7731, either the AV_{DD} or the DV_{DD} supply can come up first. While the latch-up performance of the AD7731 is very good, it is important that power is applied to the AD7731 before signals at REF IN, AIN or the logic input pins in order to avoid latch-up caused by excessive current. If this is not possible, then the current which flows in any of these pins should be limited to less than 30 mA per pin and less than 100 mA cumulative. If separate supplies are used for the AD7731 and the system digital circuitry, then the AD7731 should be powered up first. If it is not possible to guarantee this, then current limiting resistors should be placed in series with the logic inputs to again limit the current to less than 30 mA per pin and less than 100 mA total.

Grounding and Layout

Since the analog inputs and reference input are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent Common-Mode Rejection of the part will remove common-mode noise on these inputs. The analog and digital supplies to the AD7731 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs provided those noise sources do not saturate the analog modulator. As a result, the AD7731 is more immune to noise interference that a conventional high resolution converter. However, because the resolution of the AD7731 is so high and the noise levels from the AD7731 so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7731 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes which can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD7731 is the only device requiring an AGND to DGND connection, the ground planes should be connected at the AGND and DGND pins of the AD7731. If the AD7731 is in a system where multiple devices require AGND to DGND connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD7731.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7731 to avoid noise coupling. The power supply lines to the AD7731 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. All analog supplies should be decoupled with 10 μF tantalum in parallel with 0.1 μF capacitors to AGND. To achieve the best from these decoupling components, they have to be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 μF disc ceramic capacitors to DGND. In systems where a common supply voltage is used to drive both the AV_{DD} and DV_{DD} of the AD7731, it is recommended that the system's AV_{DD} supply is used. This supply should have the recommended analog supply decoupling capacitors between the AV_{DD} pin of the AD7731 and AGND and the recommended digital supply decoupling capacitor between the DV_{DD} pin of the AD7731 and DGND.

Evaluating the AD7731 Performance

A recommended layout for the AD7731 is outlined in the evaluation board for the AD7731. The evaluation board package includes a fully assembled and tested evaluation board, documentation, software for controlling the board over the printer port of a PC and software for analyzing the AD7731's performance on the PC. The evaluation board order number is EVAL-AD7731EB.

Noise levels in the signals applied to the AD7731 may also affect performance of the part. The AD7731 allows a technique for evaluating the true performance of the part, independent of the analog input signal. This scheme should be used after a calibration has been performed on the part.

The first method is to select the AIN6/AIN6 input channel arrangement. In this case, the differential inputs to the AD7731 are internally shorted together to provide a zero differential voltage for the analog modulator. External to the device, the AIN6 input should be connected to a voltage which is within the allowable common-mode range of the part.

The software in the evaluation board package allows the user to look at the noise performance in terms of bits and nV. Once the user has established that the noise performance of the part is satisfactory in this mode, then an external input voltage can be applied to the device incorporating more of the signal chain.

SERIAL INTERFACE

The AD7731's programmable functions are controlled via a set of on-chip registers. Access to these registers is via the part's serial interface. After power-on or RESET, the device expects a write to its Communications Register. The data written to this register determines whether the next operation to the part is a read or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to one of the control registers on the part starts with a write operation to the Communications Register followed by a write to the selected register. Reading from the part's on-chip registers can either take the form of a single read or continuous read. A single read from a register consists of a write to the Communications Register (with RW1 = 0 and RW0 = 1) followed by the read from the specified register. To perform continuous reads from a register, write to the Communications Register (with RW1 = 1 and RW0 = 0) to place the part in continuous read mode. The specified register can then be read from continuously until a write operation to the Communications Register (with RW1 = 1 and RW0 = 1) which takes the part out of continuous read mode. When operating in continuous read mode, the part is continuously monitoring its DIN line. Therefore, the DIN line should be permanently low to allow the part to stay in continuous read mode. Figure 5 and Figure 6, shown previously, indicate the correct flow diagrams when reading and writing from the AD7731's registers.

The AD7731's serial interface consists of five signals, $\overline{CS}$, SCLK, DIN, DOUT and $\overline{RDY}$. The DIN line is used for transferring data into the on-chip registers while the DOUT line is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on DIN or DOUT) take place with respect to this SCLK signal.

Write Operation

The transfer of data into the part is to an input shift register. On completion of a write operation, data is transferred to the specified register. This internal transfer will not take place until the correct number of bits for the specified register have been loaded to the input shift register. For example, the transfer of data from the input shift register takes place after eight serial clock cycles for a DAC Register write while the transfer of data from the input shift register takes place after 24 serial clock cycles when writing to the Filter Register. Figure 16 shows a timing diagram for a write operation to the input shift register of the AD7731. With the POL input at a logic high, the data is latched into the input shift register on the rising edge of SCLK. With the POL input at a logic low, the data is latched into the input shift register on the falling edge of SCLK.

Figure 16 also shows the $\overline{CS}$ input being used to decode the write operation to the AD7731. However, this $\overline{CS}$ input can be used in a number of different ways. It is possible to operate the part in three-wire mode where the $\overline{CS}$ input is permanently tied low. In this case, the SCLK line should idle high between data transfer when the POL input is high and should idle low between data transfers when the POL input is low. For POL = 1, the first falling edge of SCLK clocks data from the microcontroller onto the DIN line of the AD7731. It is then clocked into the input shift register on the next rising edge of SCLK. For POL = 0, the first clock edge which clocks data from the microcontroller onto the DIN line of the AD7731 is a rising edge. It is then clocked into the input shift register on the next falling edge of SCLK.

In other microcontroller applications, which require a decoding of the AD7731, $\overline{CS}$ can be generated from a port line. In this case, $\overline{CS}$ would go low well in advance of the first falling edge of SCLK (POL = 1) or the first rising edge of SCLK (POL = 0). Clocking of each bit of data is as just described.

In DSP applications, the SCLK is generally a continuous clock. In these applications, the $\overline{CS}$ input for the AD7731 is generated from a frame synchronization signal from the DSP. For processors with the rising edge of SCLK as the active edge, the POL input should be tied high. For processors with the falling edge of SCLK as the active edge, the POL input should be tied low. In these applications, the first edge after $\overline{CS}$ goes low is the active edge. The MSB of the data to be shifted into the AD7731 must be set up prior to this first active edge.

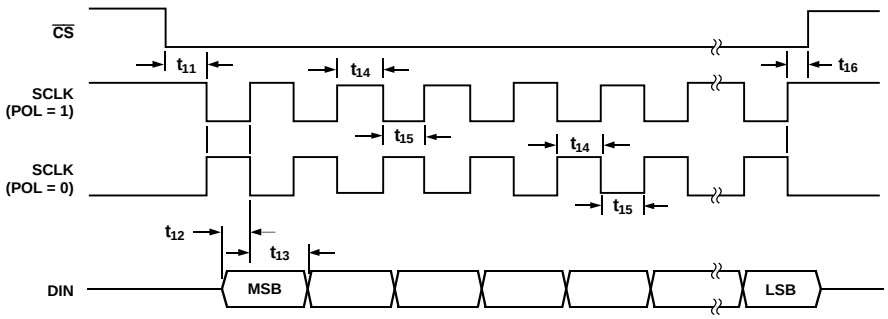


Figure 16. Write Cycle Timing Diagram

Read Operation

The reading of data from the part is from an output shift register. On initiation of a read operation, data is transferred from the specified register to the output shift register. This is a parallel shift and is transparent to the user. Figure 16 shows a timing diagram for a read operation from the output shift register of the AD7731. With the POL input at a logic high, the data is clocked out of the output shift register on the falling edge of SCLK. With the POL input at a logic low, the data is clocked out of the output shift register on the rising edge of SCLK.

Figure 16 also shows the $\overline{CS}$ input being used to decode the read operation to the AD7731. However, this $\overline{CS}$ input can be used in a number of different ways. It is possible to operate the part in three-wire mode where the $\overline{CS}$ input is tied low permanently. In this case, the SCLK line should idle high between data transfer when the POL input is high and should idle low between data transfers when the POL input is low. For POL = 1, the first falling edge of SCLK clocks data from the output shift register onto the DOUT line of the AD7731. It is then clocked into the microcontroller on the next rising edge of SCLK. For POL = 0, the first clock edge which clocks data from the AD7731 onto the DOUT line is a rising edge. It is then clocked into the microcontroller on the next falling edge of SCLK.

In other microcontroller applications, which require a decoding of the AD7731, $\overline{CS}$ can be generated from a port line. In this case, $\overline{CS}$ would go low well in advance of the first falling edge of SCLK (POL = 1) or the first rising edge of SCLK (POL = 0). Clocking of each bit of data is as just described.

In DSP applications, the SCLK is generally a continuous clock. In these applications, the $\overline{CS}$ input for the AD7731 is generated from a frame synchronization signal from the DSP. In these applications, the first edge after $\overline{CS}$ goes low is the active edge. The MSB of the data to be shifted into the microcontroller must be set up prior to this first active edge. Unlike microcontroller applications, the DSP does not provide a clock edge to clock the MSB from the AD7731. In this case, the $\overline{CS}$ of the AD7731 places the MSB on the DOUT line. For processors with the rising edge of SCLK as the active edge, the POL input should be tied high. In this case, the microcontroller takes data on the rising edge. If $\overline{CS}$ goes low while SCLK is low, the MSB is clocked out on the DOUT line from the $\overline{CS}$. Subsequent data bits are clocked from the falling edge of SCLK. For processors with the falling edge of SCLK as the active edge, the POL input should be tied low. In this case, the microcontroller takes data on the falling edge. If $\overline{CS}$ goes low while SCLK is high, then the MSB is clocked out on the DOUT line from the $\overline{CS}$. Subsequent data bits are clocked from the rising edge of SCLK.

The $\overline{RDY}$ line is used as a status signal to indicate when data is ready to be read from the AD7731's data register. $\overline{RDY}$ goes low when a new data word is available in the data register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the data register to indicate when a read from the data register should not be initiated. This is to ensure that the transfer of data from the data register to the output shift register does not occur while the data register is being updated. It is possible to read the same data twice from the output register even though the $\overline{RDY}$ line returns high after the first read operation. Care must be taken, however, to ensure that the read operations are not initiated as the next output update is about to take place.

For systems with a single data line, the DIN and DOUT lines on the AD7731 can be connected together but care must be taken in this case not to place the part in continuous read mode as the part monitors DIN while supplying data on DOUT and as a result, it may not be possible to take the part out of its continuous read mode.

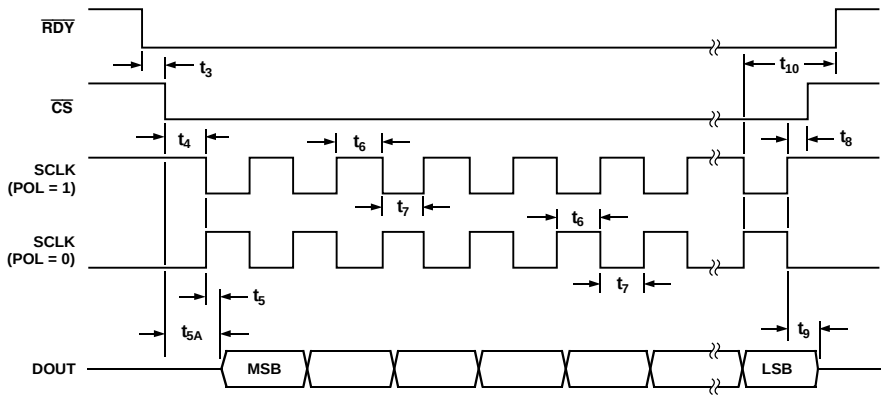


Figure 17. Read Cycle Timing Diagram

CONFIGURING THE AD7731

The AD7731 contains twelve on-chip registers which can be accessed via the serial interface. Figure 5 and Figure 6 have outlined a flowchart for the reading and writing of these registers. Table XIX and Table XX outline sample pseudo-code for some commonly used routines. The required operating conditions will dictate the values loaded to the Mode and Filter Registers. The values given here are for example purposes only.

Table XIX. Pseudo-Code for Initiating a Self-Calibration after Power-On/Reset

Write 03 Hex to Serial Port[1]	/* Writes to Communications Register Setting Next Operation as Write to Filter Register*/
Write 1332 Hex to Serial Port[1]	/* Writes to Filter Register Setting a 1 kHz Output Rate in nonCHOP Mode*/
Write 02 Hex to Serial Port	/* Writes to Communications Register Setting Next Operation as Write to Mode Register*/
Write B174 Hex to Serial Port	/* Writes to Mode Register Initiating Internal Full-Scale Calibration for 0 V to +1.28 V Input Range on Channel Pair AIN1/AIN2*/
Wait for $\overline{\text{RDY}}$ Low	/* Wait for $\overline{\text{RDY}}$ pin to go low to indicate end of calibration cycle*/
Write 02 Hex to Serial Port	/* Writes to Communications Register Setting Next Operation as Write to Mode Register*/
Write 9174 Hex to Serial Port	/* Writes to Mode Register Initiating Internal Zero-Scale Calibration for 0 V to +1.28 V Input Range*/
Wait for $\overline{\text{RDY}}$ Low	/* Wait for $\overline{\text{RDY}}$ pin to go low to indicate end of calibration cycle*/
	/* The part has now completed self-calibration and is in idle mode*/

[1]This operation is not necessary if the default values of the Filter Register are the values used in the application.

Table XX. Pseudo-Code for Looping AD7731 Through Three Fully-Differential Channels

CHANNEL = 4 Hex	/* Sets a Variable Called CHANNEL*/
CH_LOOP: MODE = 2177 Hex	/* Sets a Variable Called MODE */
MODE = MODE AND CHANNEL	/* Logical AND of Both Variables */
Write 02 Hex to Serial Port	/* Writes to Communications Register Setting Next Operation as Write to Mode Register*/
Write MODE to Serial Port	/* Writes to Mode Register Setting Continuous Conversion Mode for 0 V to +1.28 V Input Range on Channel Determined by CHANNEL Variable*/
Wait for $\overline{\text{RDY}}$ Low	/* Wait for $\overline{\text{RDY}}$ pin to go low to Indicate Output Update*/
Write 11 Hex to Serial Port	/* Writes to Communications Register Setting Next Operation as Read From Data Register*/
Read 24-Bit Data From Serial Port	/* Read Conversion Result from AD7731's Data Register*/
Increment CHANNEL	/* Increments Channel Address*/
If CHANNEL = 7Hex Then Set CHANNEL = 4 Hex	/* Resets Channel Address*/
Loop to CH_LOOP	

MICROCOMPUTER/MICROPROCESSOR INTERFACING

The AD7731's flexible serial interface allows for easy interface to most microcomputers and microprocessors. The pseudo-code of Table XVIII and Table XIX outline typical sequences for interfacing a microcontroller or microprocessor to the AD7731. Figures 18, 19 and 20 show some typical interface circuits.

The serial interface on the AD7731 has the capability of operating from just three wires and is compatible with SPI interface protocols. The three-wire operation makes the part ideal for isolated systems where minimizing the number of interface lines minimizes the number of opto-isolators required in the system.

Register lengths on the AD7731 vary from 8 to 16 to 24 bits. The 8-bit serial serial ports of most microcontrollers can handle communication with these registers as either one, two or three 8-bit transfers. DSP processors and microprocessors generally transfer 16 bits of data in a serial data operation. Some of these processors, such as the ADSP-2105, have the facility to program the amount of cycles in a serial transfer. This allows the user to tailor the number of bits in any transfer to match the register length of the required register in the AD7731. In any case, writing 32 bits of data to a 24-bit register is not an issue provided the final 8 bits of the word are all 1s. This is because the part returns to the Communications Register following a write operation.

AD7731 to 68HC11 Interface

Figure 18 shows an interface between the AD7731 and the 68HC11 microcontroller. The diagram shows the minimum (three-wire) interface with $\overline{CS}$ on the AD7731 hard-wired low. In this scheme, the $\overline{RDY}$ bit of the Status Register is monitored to determine when the Data Register is updated. An alternative scheme, which increases the number of interface lines to four, is to monitor the $\overline{RDY}$ output line from the AD7731. The monitoring of the $\overline{RDY}$ line can be done in two ways. First, $\overline{RDY}$ can be connected to one of the 68HC11's port bits (such as PC0) which is configured as an input. This port bit is then polled to determine the status of $\overline{RDY}$. The second scheme is to use an interrupt driven system in which case, the $\overline{RDY}$ output is connected to the IRQ input of the 68HC11. For interfaces which require control of the $\overline{CS}$ input on the AD7731, one of the port bits of the 68HC11 (such as PC1), which is configured as an output, can be used to drive the $\overline{CS}$ input.

The 68HC11 is configured in the master mode with its CPOL bit set to a logic zero and its CPHA bit set to a logic one. When the 68HC11 is configured like this, its SCLK line idles low between data transfers. Therefore, the POL input of the AD7731 should be hard-wired low. For systems where it is preferable that the SCLK idle high, the CPOL bit of the 68HC11 should be set to a logic 1 and the POL input of the AD7731 should be hard-wired to a logic high.

The AD7731 is not capable of full duplex operation. If the AD7731 is configured for a write operation, no data appears on the DATA OUT lines even when the SCLK input is active. However, when the AD7731 is configured for continuous read operation, data presented to the part on the DATA IN line is monitored to determine when to exit the continuous read mode.

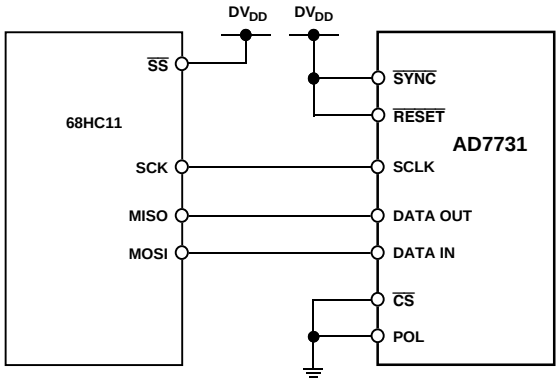


Figure 18. AD7731 to 68HC11 Interface

AD7731 to 8051 Interface

An interface circuit between the AD7731 and the 8XC51 microcontroller is shown in Figure 19. The diagram shows the minimum number of interface connections with $\overline{CS}$ on the AD7731 hard-wired low. In the case of the 8XC51 interface the minimum number of interconnects is just two. In this scheme, the $\overline{RDY}$ bit of the Status Register is monitored to determine when the Data Register is updated. The alternative scheme, which increases the number of interface lines to three, is to monitor the $\overline{RDY}$ output line from the AD7731. The monitoring of the $\overline{RDY}$ line can be done in two ways. First, $\overline{RDY}$ can be connected to one of the 8XC51's port bits (such as P1.0) which is configured as an input. This port bit is then polled to determine the status of $\overline{RDY}$. The second scheme is to use an interrupt driven system in which case, the $\overline{RDY}$ output is connected to the INT1 input of the 8XC51. For interfaces which require control of the $\overline{CS}$ input on the AD7731, one of the port bits of the 8XC51 (such as P1.1), which is configured as an output, can be used to drive the $\overline{CS}$ input.

The 8XC51 is configured in its Mode 0 serial interface mode. Its serial interface contains a single data line. As a result, the DATA OUT and DATA IN pins of the AD7731 should be connected together. This means that the AD7731 must not be configured for continuous read operation when interfacing to the 8XC51. The serial clock on the 8XC51 idles high between data transfers and, therefore, the POL input of the AD7731 should be hard-wired to a logic high. The 8XC51 outputs the LSB first in a write operation while the AD7731 expects the MSB first so the data to be transmitted has to be rearranged before being written to the output serial register. Similarly, the AD7731 outputs the MSB first during a read operation while the 8XC51 expects the LSB first. Therefore, the data read into the serial buffer needs to be rearranged before the correct data word from the AD7731 is available in the accumulator.

AD7731 to ADSP-2103/ADSP-2105 Interface

Figure 20 shows an interface between the AD7731 and the ADSP-2105 DSP processor. In the interface shown, the $\overline{RDY}$ bit of the Status Register is again monitored to determine when the Data Register is updated. The alternative scheme is to use an interrupt driven system, in which case the $\overline{RDY}$ output is connected to the $\overline{IRQ2}$ input of the ADSP-2105. The $\overline{RFS}$ and $\overline{TFS}$ pins of the ADSP-2105 are configured as active low outputs and the ADSP-2105 serial clock line, SCLK, is also configured as an output. The POL pin of the AD7731 is hard-wired low. Because the SCLK from the ADSP-2105 is a continuous clock, the $\overline{CS}$ of the AD7731 must be used to gate off the clock once the transfer is complete. The $\overline{CS}$ for the AD7731 is active when either the $\overline{RFS}$ or $\overline{TFS}$ outputs from the ADSP-2105 are active. The serial clock rate on the ADSP-2105 should be limited to 3 MHz to ensure correct operation with the AD7731.

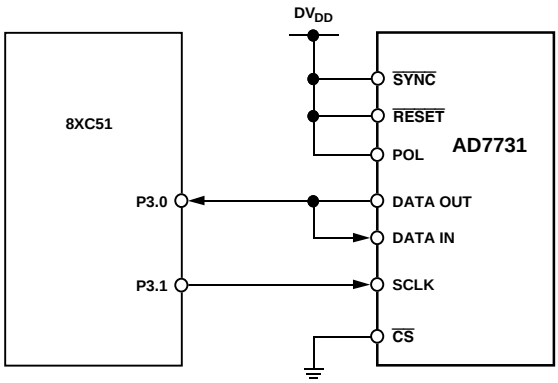


Figure 19. AD7731 to 8XC51 Interface

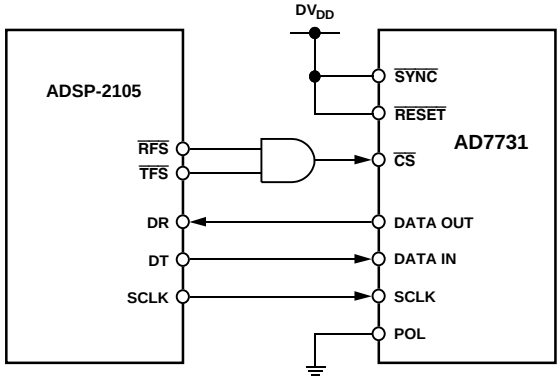


Figure 20. AD7731 to ADSP-2105 Interface

APPLICATIONS

The on-chip PGA allows the AD7731 to handle analog input voltage ranges from 20 mV to 1.28 V. This makes the AD7731 suitable for a range of application areas from handling signals directly from a transducer to processing fully-conditioned full-scale inputs. Some of these applications are discussed in the following sections.

The AD7731 offers both unipolar and bipolar input ranges. In many cases, the application is single supply with the bipolar input voltages referenced to a biased-up differential voltage. Some applications will, however, require the flexibility of handling true bipolar inputs. Figure 25 shows how to configure the AD7731 to handle this type of signal.

It should be noted in multiplexed applications that an input overvoltage (either >AVDD + 0.3 V or <AGND – 0.3 V) on an unselected channel can affect the conversion result on the selected channel. The system design should ensure that the input voltage on channels where input leads may be unconnected or broken be kept within the above limits.

The AD7731 has a variety of different modes aimed at optimizing the AD7731's performance across differing application requirements. The issue of filtering and settling time and throughput rates in multichannel applications has previously been discussed in the Filter Architecture section.

Data Acquisition

The AD7731 with its three differential channels (or five pseudo-differential channels) is suited to low bandwidth, high resolution data acquisition systems. In addition, the three-wire digital interface allows this data acquisition front end to be isolated with just three optoisolators. The entire system can be operated from a single +5 V supply provided that the input signals to the AD7731's analog inputs are all of positive polarity. Figure 21 shows the AD7731 in an isolated three-channel data acquisition system.

Programmable Logic Controllers

The AD7731 is also suited to programmable logic controller applications. In such applications, the ADC is required to handle signals from a variety of different transducers. The AD7731's programmable gain front end allows the part to either handle low level signals directly from a transducer or full-scale signals which have already been conditioned. The fast throughput rate and settling-time of the part is also an important feature in these applications where loop response time is often critical. The configuration of the AD7731 in PLC applications is similar to that outlined in Figure 21 for the data acquisition system.

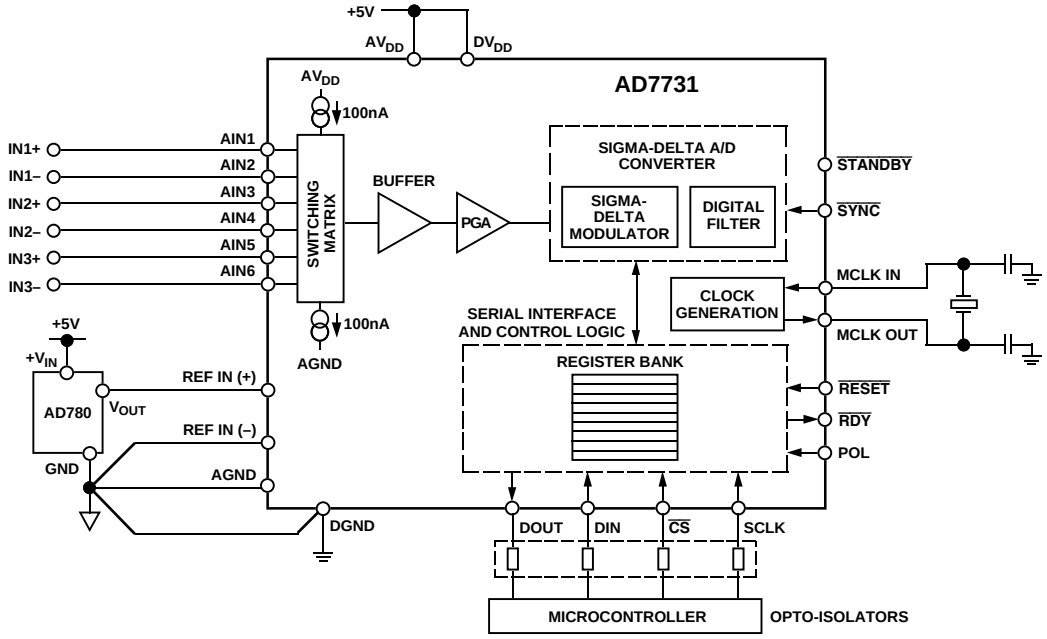


Figure 21. Data Acquisition Using the AD7731

Pressure Measurement

One typical application of the AD7731 where it is connected directly to a transducer is in pressure measurement. Figure 22 shows the AD7731 with a pressure transducer in a bridge arrangement. The differential output from the transducer is connected directly to the AIN1/AIN2 input channel. The entire circuit is powered from a single +5 V supply that generates the excitation voltage for the transducer and the power supply, and reference voltage for the AD7731. The application is ratiometric and variations in the excitation voltage do not introduce errors in the measurement.

Temperature Measurement

Another application area where the transducer can be connected directly to the AD7731 is in temperature measurement. Figure 23 outlines a connection between a thermocouple and the AD7731. In order to place the differential voltage from the AD7731 on a suitable common-mode voltage, the AIN2 input of the AD7731 is biased up at the reference voltage, +2.5 V.

Figure 24 shows another temperature measurement application for the AD7731. In this case, the temperature transducer is an RTD (Resistive Temperature Device), a PT100. The arrangement is a four-lead RTD configuration. There are voltage drops across lead resistances RL1 and RL4 and across resistor R2 but these simply shift the common-mode voltage. Resistor R2 is required to set the common-mode voltage within the allowable range for the AD7731. The voltage differential caused by RL2 and RL3 and the AD7731's offset current is negligible.

In the application shown, the external 400 μA current source provides the excitation current for the PT100 and it also generates the reference voltage for the AD7731 via resistor R1. Variations in the excitation current do not affect the circuit as the input voltage and the reference voltage vary ratiometrically with the excitation current. Resistor R1, however, must have a low temperature coefficient to avoid errors in the reference voltage over temperature.

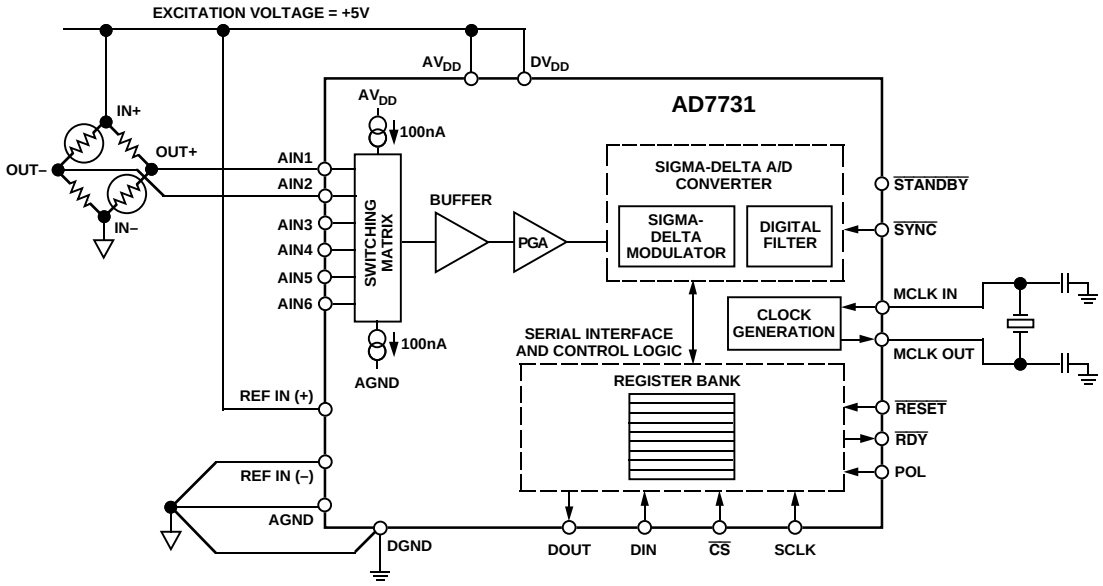


Figure 22. Pressure Measurement Using the AD7731

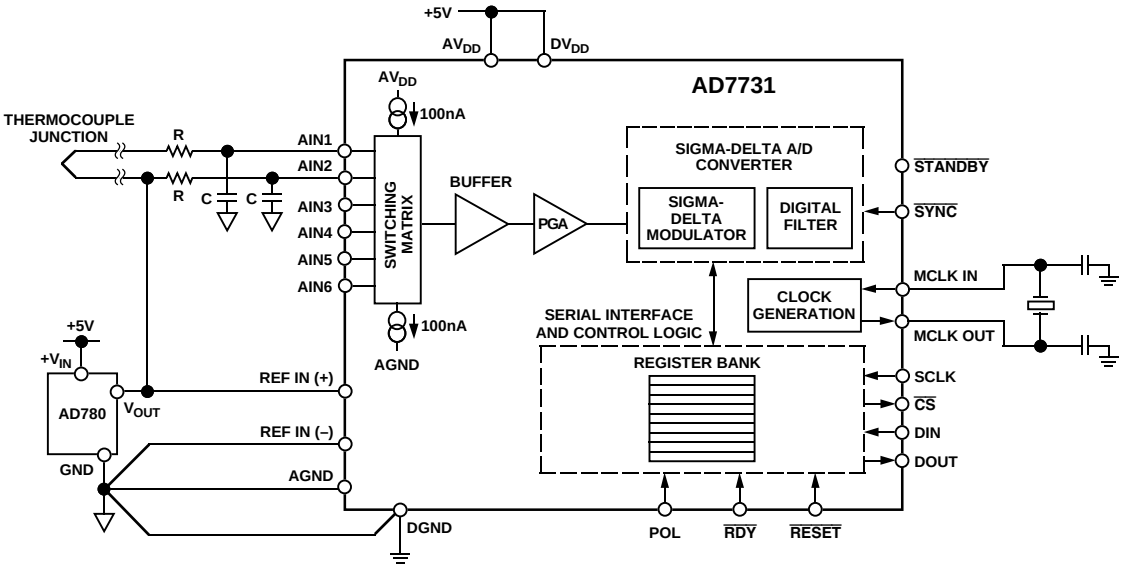


Figure 23. Temperature Measurement Using the AD7731

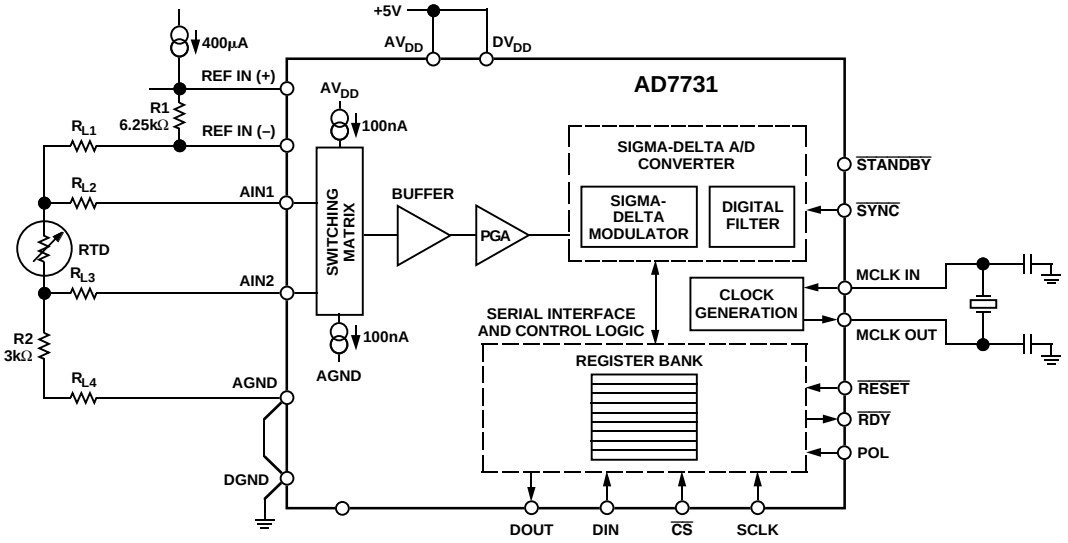


Figure 24. RTD Measurement Using the AD7731

Bipolar Input Signals

As mentioned previously, some applications will require that the AD7731 handle input signals that are negative with respect to system ground. The number of applications requiring this are limited but with the addition of some external components the AD7731 is capable of handling such signals. Figure 25 outlines one approach to the problem.

The example shown is a system that is driven from ±5 V supplies. In such a circuit, two issues must be addressed. The first is how to get the AD7731 to handle input voltages below ground and the second is how to generate a suitable reference voltage for the AD7731. The circuit of Figure 25 attempts to address these two issues simultaneously.

The AD7731's analog and digital supplies can be split such that AV_{DD} and DV_{DD} can be at separate potentials and AGND and DGND can also be at separate potentials. The only stipulation is that AV_{DD} or DV_{DD} must not exceed the AGND by 5.5 V. In Figure 25, the DV_{DD} is operated at +3 V which allows the AGND to go down to –2.5 V with respect to system ground. This means that all logic signals to the part must not exceed 3 V with respect to system ground. The AV_{DD} is operated at +2.5 V with respect to system ground.

The resistor string R1, R2 and R3 takes the ±5 V supply voltage and generates a differential voltage of nominally 5 V. Amplifiers A1 and A2 buffer the resistor string voltages and provide the AV_{DD} and AGND voltages as well as the REF IN(+) and REF IN(–) voltages for the AD7731. The differential reference voltage for the part is +5 V. If the input voltage is from a transducer excited by the ±5 V, the AD7731 retains its ratiometric operation with this reference voltage varying in sympathy with the analog input voltage.

The values of the resistors in the resistor string are chosen assuming the maximum input voltage range of ±1.28 V is applied to the AD7731. The minimum input voltage must be 1.2 V above the AD7731's AGND, while the maximum input voltage must be 0.95 V below the AD7731's AV_{DD}. For smaller input voltage ranges, the resistor ratios in the resistor string can be changed to allow a larger DV_{DD} voltage. For example, if R1 = 3 kΩ, R2 = 10 kΩ and R3 = 6.8 kΩ, the AV_{DD} and AGND voltages become +3.49 V and –1.56 V respectively. This allows the AD7731 to be used with a +3.6 V DV_{DD} voltage while allowing analog input ranges of ±320 mV and below.

An alternate scheme is to generate the AV_{DD} and AGND voltages from regulators or Zener diodes driven from the +5 V and –5 V supplies respectively. The reference voltage for the part can be generated from an AD780 whose GND pin is connected to the AD7731's AGND pin.

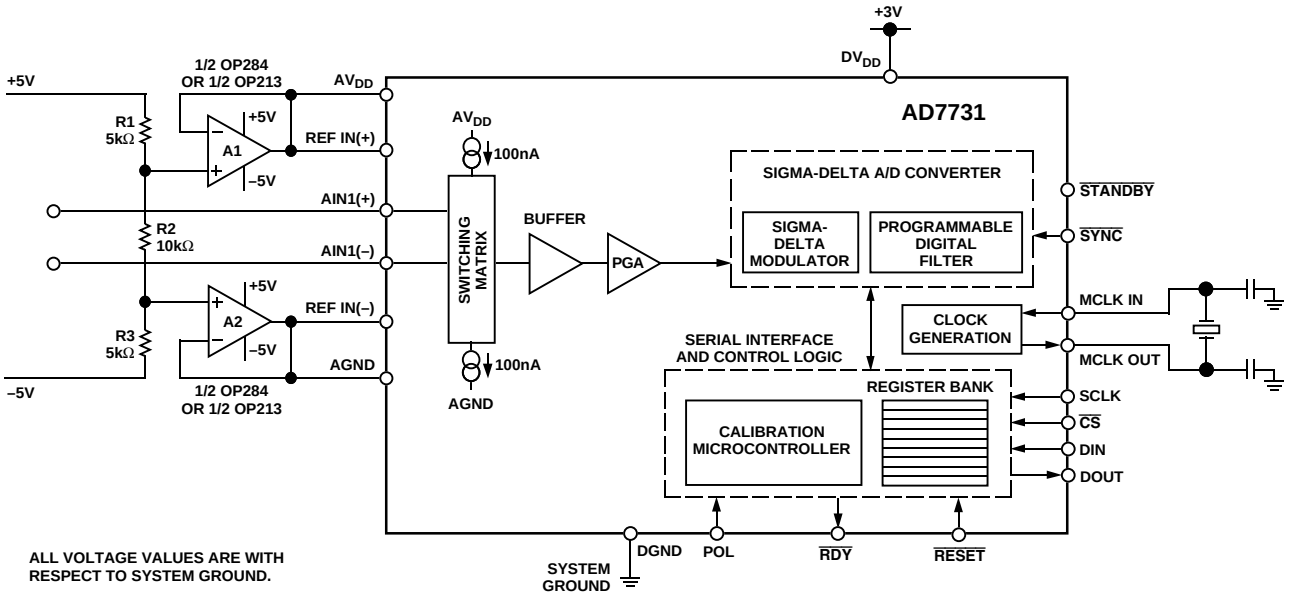


Figure 25. Bipolar Input Signals on the AD7731

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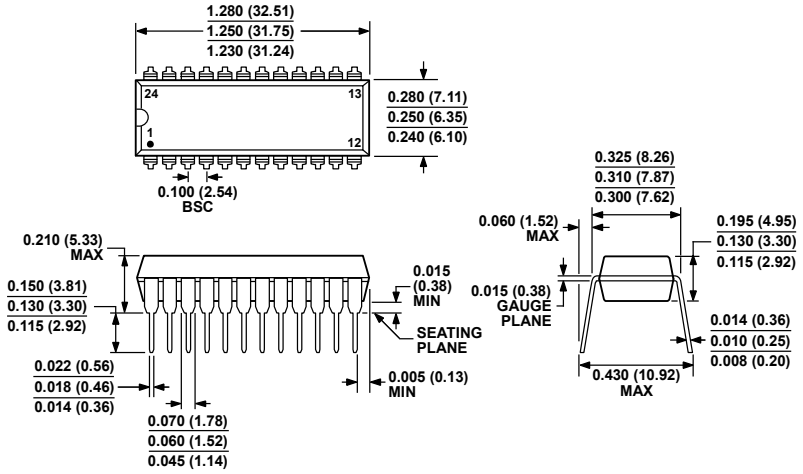
OUTLINE DIMENSIONS

24-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body (N-24-1)

Dimensions shown in inches and (millimeters)



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071006-A

24-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-24)

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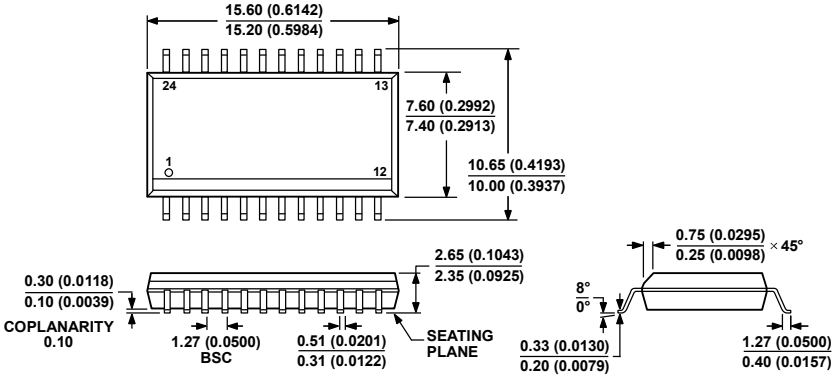

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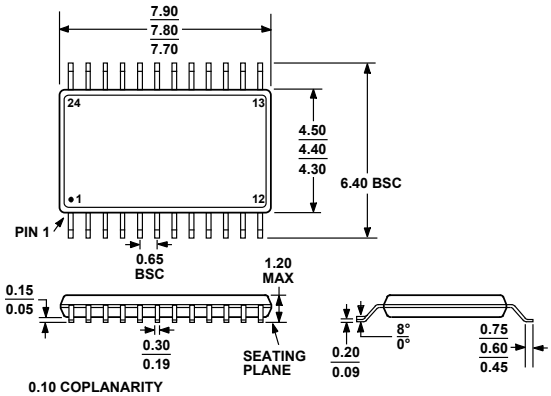
060706-A

24-Lead Thin Shrink Small Outline Package [TSSOP]
[RU-24]

Dimensions shown in millimeters



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