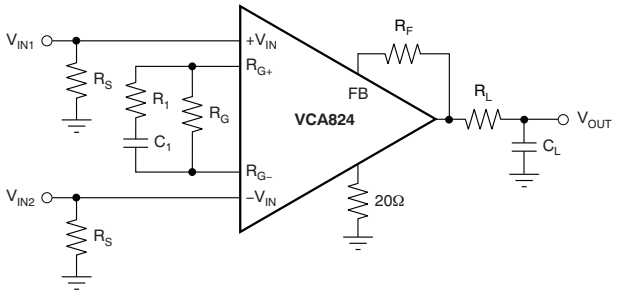
Ultra-Wideband, > 40dB Gain Adjust Range, Linear in V/V VARIABLE GAIN AMPLIFIER

FEATURES

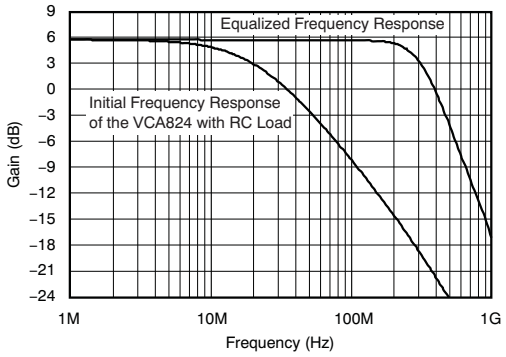
- **710MHz SMALL-SIGNAL BANDWIDTH (G = +2V/V)**
- **320MHz, 4V_{PP} BANDWIDTH (G = +10V/V)**
- **0.1dB GAIN FLATNESS to 135MHz**
- **2500V/µs SLEW RATE**
- **> 40dB GAIN ADJUST RANGE**
- **HIGH GAIN ACCURACY: 20dB ±0.3dB**
- **HIGH OUTPUT CURRENT: ±90mA**

APPLICATIONS

- **DIFFERENTIAL LINE RECEIVERS**
- **DIFFERENTIAL EQUALIZERS**
- **PULSE AMPLITUDE COMPENSATION**
- **VARIABLE ATTENUATORS**
- **VOLTAGE-TUNABLE ACTIVE FILTERS**



Differential Equalizer



Differential Equalization of an RC Load

DESCRIPTION

The VCA824 is a dc-coupled, wideband, linear in V/V, continuously variable, voltage-controlled gain amplifier. It provides a differential input to single-ended conversion with a high-impedance gain control input used to vary the gain down 40dB from the nominal maximum gain set by the gain resistor (R_G) and feedback resistor (R_F).

The VCA824 internal architecture consists of two input buffers and an output current feedback amplifier stage integrated with a multiplier core to provide a complete variable gain amplifier (VGA) system that does not require external buffering. The maximum gain is set externally with two resistors, providing flexibility in designs. The maximum gain is intended to be set between +2V/V and +40V/V. Operating from ±5V supplies, the gain control voltage for the VCA824 adjusts the gain linearly in V/V as the control voltage varies from +1V to –1V. For example, set for a maximum gain of +10V/V, the VCA824 provides 10V/V, at +1V input, to 0.1V/V at –1V input of gain control range. The VCA824 offers excellent gain linearity. For a 20dB maximum gain, and a gain-control input voltage varying between 0V and 1V, the gain does not deviate by more than ±0.3dB (maximum at +25°C).

VCA824 RELATED PRODUCTS

SINGLES	DUALS	GAIN ADJUST RANGE (dB)	INPUT NOISE (nV/√Hz)	SIGNAL BANDWIDTH (MHz)
VCA810	—	80	2.4	35
—	VCA2612	45	1.25	80
—	VCA2613	45	1	80
—	VCA2615	52	0.8	50
—	VCA2617	48	4.1	50
VCA820	—	40	8.2	150
VCA821	—	40	6.0	420
VCA822	—	40	8.2	150
VCA824	—	40	6.0	420

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VCA824	SO-14	D	–40°C to +85°C	VCA824ID	VCA824ID	Rail, 50
					VCA824IDR	Tape and Reel, 2500
VCA824	MSOP-10	DGS	–40°C to +85°C	BOT	VCA824IDGST	Tape and Reel, 250
					VCA824IDGSR	Tape and Reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

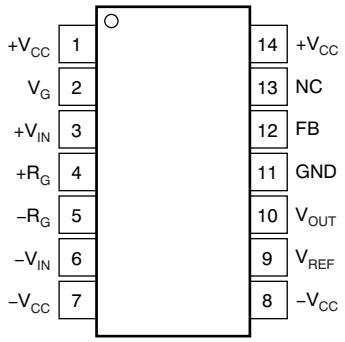
ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		VCA824	UNIT
Power Supply		±6.5	V
Internal Power Dissipation		See Thermal Characteristics	
Input Voltage Range		$\pm V_S$	V
Storage Temperature Range		–65 to +125	°C
Lead Temperature (soldering, 10s)		+260	°C
Junction Temperature (T_J)		+150	°C
Junction Temperature (T_J), Maximum Continuous Operation		+140	°C
ESD Rating	Human Body Model (HBM)	2000	V
	Charge Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

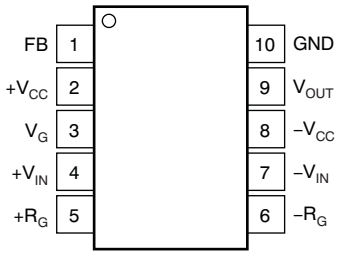
PIN CONFIGURATION

D PACKAGE SO-14 (TOP VIEW)



NC = No Connection

DGS PACKAGE MSOP-10 (TOP VIEW)



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ELECTRICAL CHARACTERISTICS: V_S = ±5V

At A_{VMAX} = +10V/V, V_G = +1V, R_F = 402Ω, R_G = 80Ω, and R_L = 100Ω, unless otherwise noted.

PARAMETER	CONDITIONS	VCA824 TYP +25°C	VCA824 MIN/MAX OVER TEMPERATURE +25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)	UNITS	MIN/ MAX	TEST LEVEL(1)
AC PERFORMANCE								
Small-Signal Bandwidth	A_{VMAX} = +2V/V, V_G = +1V , V_O = 500mV$_{PP}$	710				MHz	typ	C
	A_{VMAX} = +10V/V, V_G = +1V, V_O = 500mV$_{PP}$	420				MHz	typ	C
	A_{VMAX} = +40V/V, V_G = +1V, V_O = 500mV$_{PP}$	170				MHz	typ	C
Large-Signal Bandwidth	A_{VMAX} = +10V/V, V_G = +1V, V_O = 4V$_{PP}$	320				MHz	typ	C
Gain Control Bandwidth	V_O = 200mV$_{PP}$	330	240	235	235	MHz	min	B
Bandwidth for 0.1dB Flatness	A_{VMAX} = +10V/V, V_G = +1V, V_O = 2V$_{PP}$	135				MHz	typ	C
Slew Rate	A_{VMAX} = +10V/V, V_G = +1V, V_O = 4V Step	2500	1800	1700	1700	V/µs	min	B
Rise-and-Fall Time	A_{VMAX} = +10V/V, V_G = +1V, V_O = 4V Step	1.5	1.8	1.9	1.9	ns	max	B
Settling Time to 0.01%	A_{VMAX} = +10V/V, V_G = +1V, V_O = 4V Step	11				ns	typ	C
Harmonic Distortion								
2nd-Harmonic	V_O = 2V$_{PP}$, f = 20MHz	-66	–64	–64	–64	dBc	min	B
3rd-Harmonic	V_O = 2V$_{PP}$, f = 20MHz	-63	–61	–61	–61	dBc	min	B
Input Voltage Noise	f > 100kHz	6				nV/√Hz	typ	C
Input Current Noise	f > 100kHz	2.6				pA/√Hz	typ	C
GAIN CONTROL								
Gain Error	A_{VMAX} = +10V/V, V_G = 1V	±0.1	**±0.4**	±0.5	±0.6	dB	max	A
Gain Deviation	A_{VMAX} = +10V/V, 0 < V_G < 1	±0.05	**±0.3**	±0.34	±0.37	dB	max	A
Gain Deviation	A_{VMAX} = +10V/V, -0.8 < V_G < 1	±1.06	**±1.9**	±2.1	±2.2	dB	max	A
Gain at V_G = –0.9V	Relative to max gain	–26	**–24**	–24	–23	dB	max	A
Gain Control Bias Current		22	**30**	35	37	µA	max	A
Average Gain Control Bias Current Drift				±100	±100	nA/°C	max	B
Gain Control Input Impedance		1.5 || 0.6				MΩ || pF	typ	C
DC PERFORMANCE								
Input Offset Voltage	A_{VMAX} = +10V/V, V_{CM} = 0V, V_G = 1V	±4	**±17**	±17.8	±19	mV	max	A
Average Input Offset Voltage Drift	A_{VMAX} = +10V/V, V_{CM} = 0V, V_G = 1V			±30	±30	µV/°C	max	B
Input Bias Current	A_{VMAX} = +10V/V, V_{CM} = 0V, V_G = 1V	19	**25**	29	31	µA	max	A
Average Input Bias Current Drift	A_{VMAX} = +10V/V, V_{CM} = 0V, V_G = 1V			±90	±90	nA/°C	max	B
Input Offset Current	A_{VMAX} = +10V/V, V_{CM} = 0V, V_G = 1V	±0.5	**±2.5**	±3.2	±3.5	µA	max	A
Average Input Offset Current Drift	A_{VMAX} = +10V/V, V_{CM} = 0V, V_G = 1V			±16	±16	nA/°C	max	B
Max Current Through Gain Resistance		±2.6	±2.55	±2.55	±2.5	mA	max	B
INPUT								
Most Positive Common-Mode Input Voltage	R_L = 100Ω	+1.6	**+1.6**	+1.6	+1.6	V	min	A
Most Negative Common-Mode Input Voltage	R_L = 100Ω	–2.1	**–2.1**	–2.1	–2.1	V	max	A
Common-Mode Rejection Ratio	V_{CM} = ±0.5V	80	**65**	60	60	dB	min	A
Input Impedance								
Differential		1 || 1				MΩ || pF	typ	C
Common-Mode		1 || 2				MΩ || pF	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.

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ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

At A_{VMAX} = +10V/V, V_G = +1V, R_F = 402Ω, R_G = 80Ω, and R_L = 100Ω, unless otherwise noted.

		VCA824						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)	UNITS	MIN/ MAX	TEST LEVEL(1)
OUTPUT								
Output Voltage Swing	R_L = 1kΩ	±3.9	**±3.6**	±3.4	±3.3	V	min	A
	R_L = 100Ω	±3.6	**±3.5**	±3.3	±3.2	V	min	A
Output Current	V_O = 0V, R_L = 10Ω	±90	**±60**	= 50	= 45	mA	min	A
Output Impedance	A_{VMAX} = +10V/V, f > 100kHz	0.01				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Minimum Operating Voltage			±4	±4	±4	V	min	B
Maximum Operating Voltage			**±6**	±6	±6	V	max	A
Maximum Quiescent Current	V_G = 0V	36.5	**37.5**	38	38.5	mA	max	A
Minimum Quiescent Current	V_G = 0V	36.5	**35**	34.5	34	mA	max	A
Power-Supply Rejection Ratio (-PSRR)	V_G = +1V	-68	**-61**	-59	-58	dB	min	A
THERMAL CHARACTERISTICS								
Specified Operating Range D Package		–40 to +85				°C	typ	C
Thermal Resistance θ_{JA}	Junction-to-Ambient							
DGS, MSOP-10		130				°C/W	typ	C
D, SO-14		80				°C/W	typ	C

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TYPICAL CHARACTERISTICS: V_S = ±5V, DC Parameters

At T_A = +25°C, R_L = 100Ω, V_G = +1V, and V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, unless otherwise noted.

MAXIMUM DIFFERENTIAL INPUT VOLTAGE vs R_G

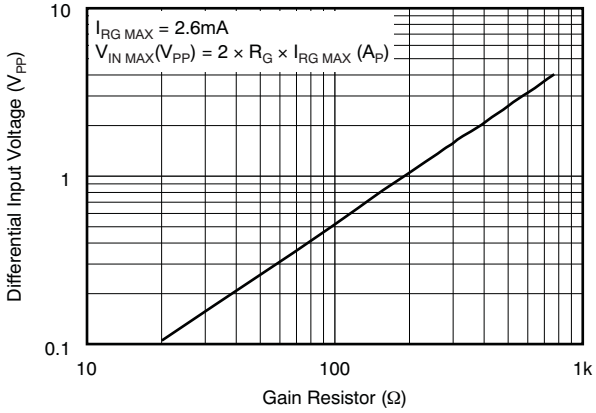

Figure 1.

MAXIMUM GAIN ADJUST RANGE vs R_F

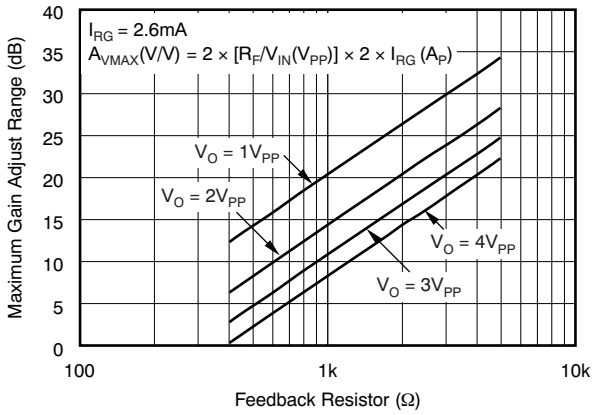

Figure 2.

MAXIMUM GAIN ADJUST RANGE vs PEAK-TO-PEAK OUTPUT VOLTAGE

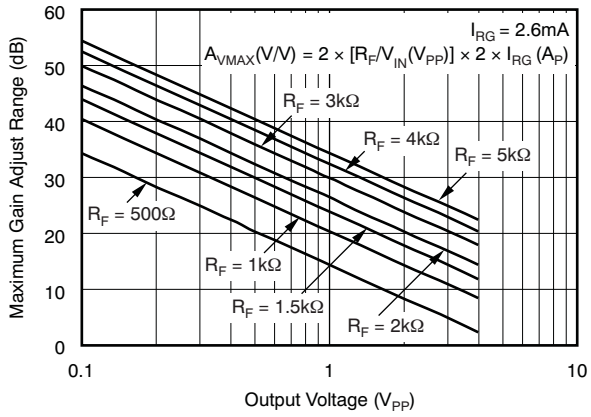

Figure 3.

GAIN ERROR BAND vs GAIN CONTROL VOLTAGE

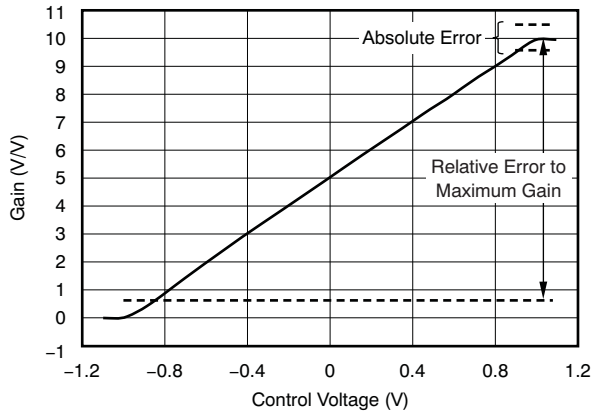

Figure 4.

GAIN ERROR BAND vs GAIN CONTROL VOLTAGE

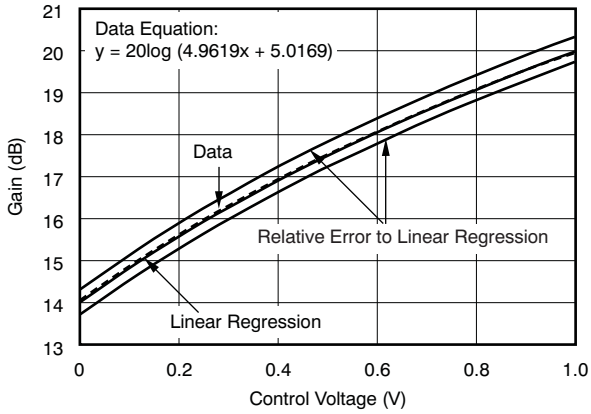

Figure 5.

GAIN ERROR BAND vs GAIN CONTROL VOLTAGE

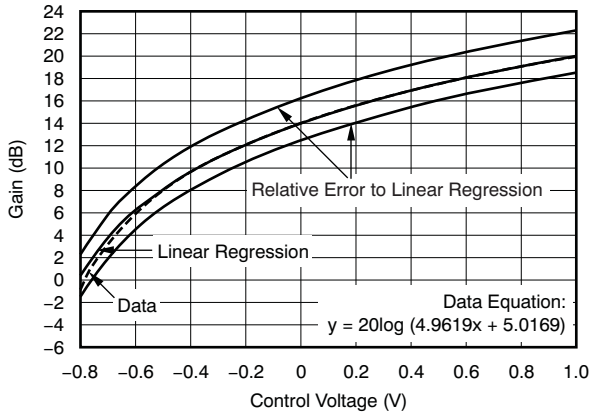

Figure 6.

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TYPICAL CHARACTERISTICS: V_S = ±5V, DC and Power-Supply Parameters

At T_A = +25°C, R_L = 100Ω, V_G = +1V, and V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, unless otherwise noted.

RECOMMENDED R_F vs A_{VMAX}

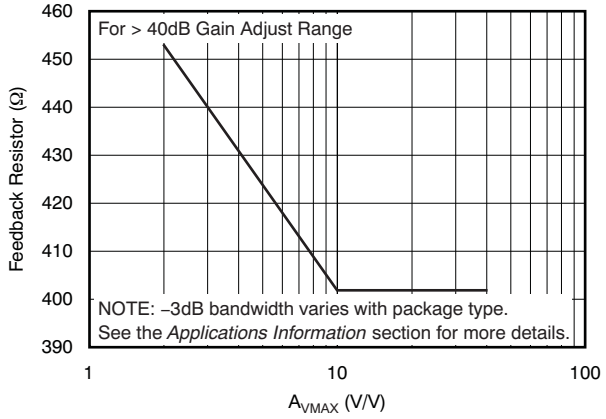

Figure 7.

SUPPLY CURRENT vs CONTROL VOLTAGE (A_{VMAX} = +2V/V)

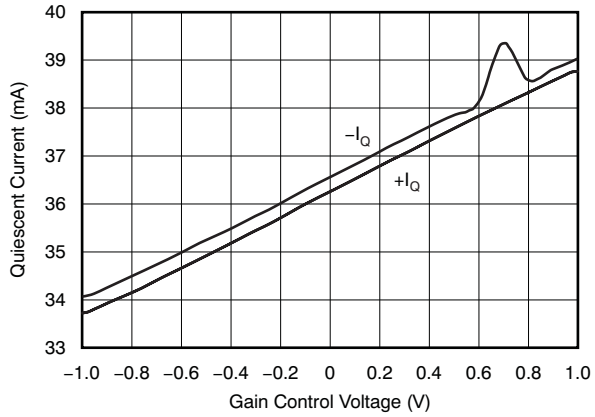

Figure 8.

SUPPLY CURRENT vs CONTROL VOLTAGE (A_{VMAX} = +10V/V)

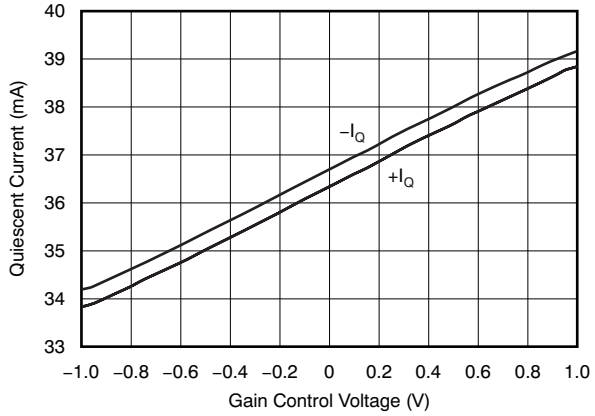

Figure 9.

SUPPLY CURRENT vs CONTROL VOLTAGE (A_{VMAX} = +40V/V)

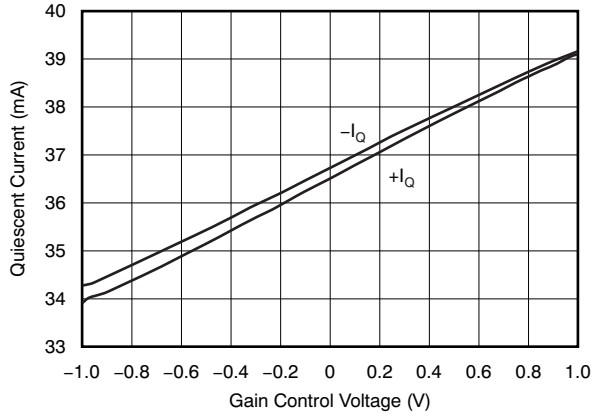

Figure 10.

TYPICAL DC DRIFT vs TEMPERATURE

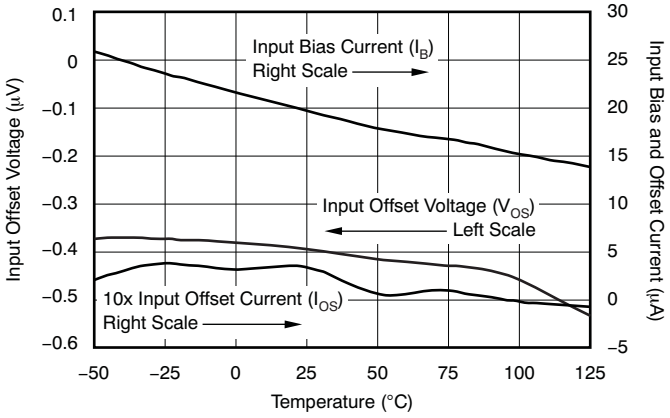

Figure 11.

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TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = +2V/V

At T_A = +25°C, R_L = 100Ω, R_F = 453Ω, R_G = 453Ω, V_G = +1V, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

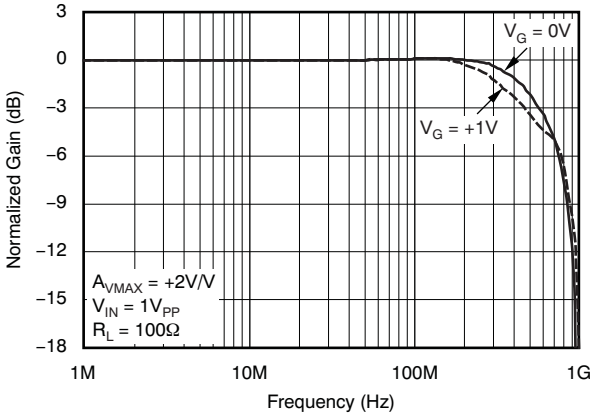

Figure 12.

LARGE-SIGNAL FREQUENCY RESPONSE

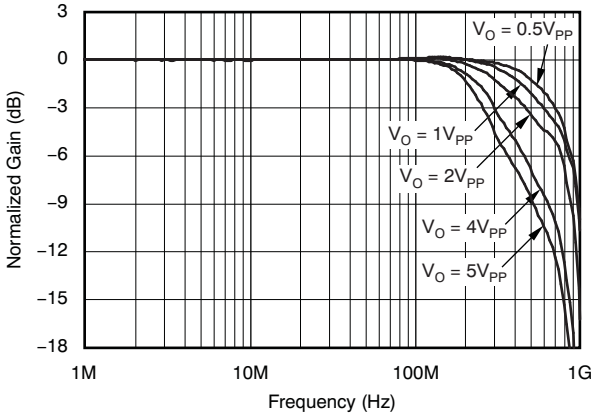

Figure 13.

SMALL-SIGNAL PULSE RESPONSE

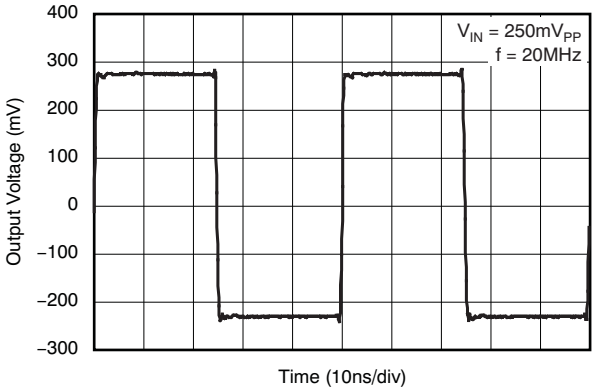

Figure 14.

LARGE-SIGNAL PULSE RESPONSE

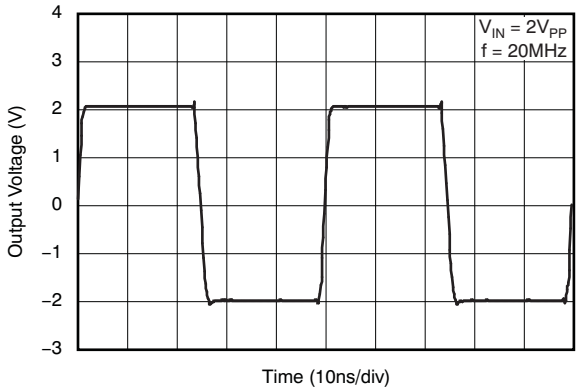

Figure 15.

COMPOSITE VIDEO dG/dP

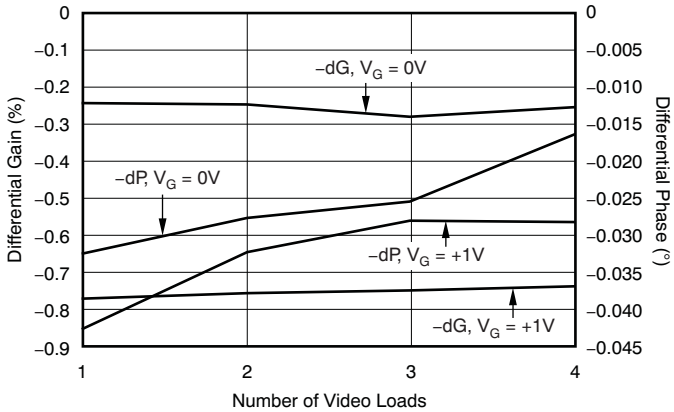

Figure 16.

GAIN FLATNESS, DEVIATION FROM LINEAR PHASE

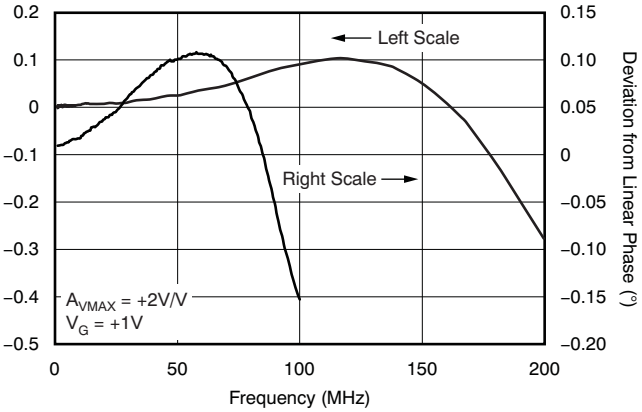

Figure 17.

TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = +2V/V (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 453Ω, R_G = 453Ω, V_G = +1V, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

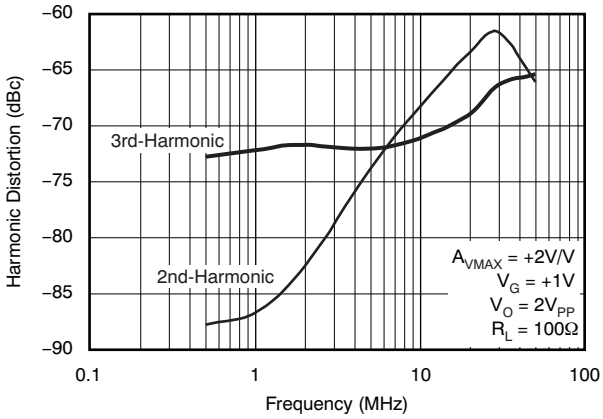

Figure 18.

HARMONIC DISTORTION vs LOAD RESISTANCE

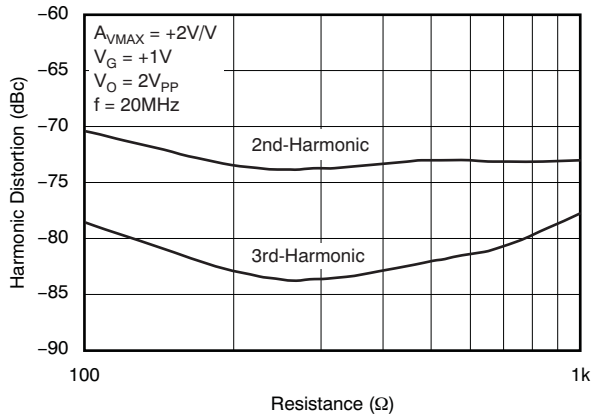

Figure 19.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

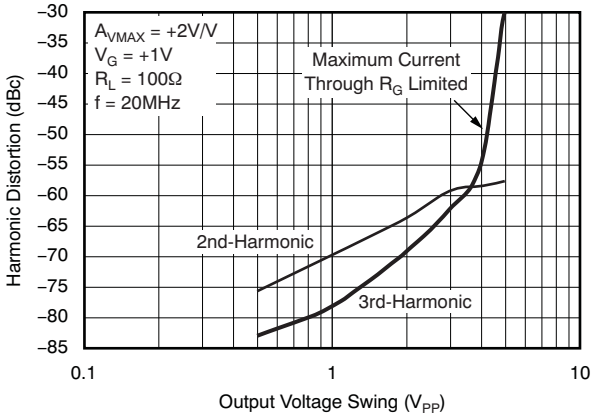

Figure 20.

HARMONIC DISTORTION vs GAIN CONTROL VOLTAGE

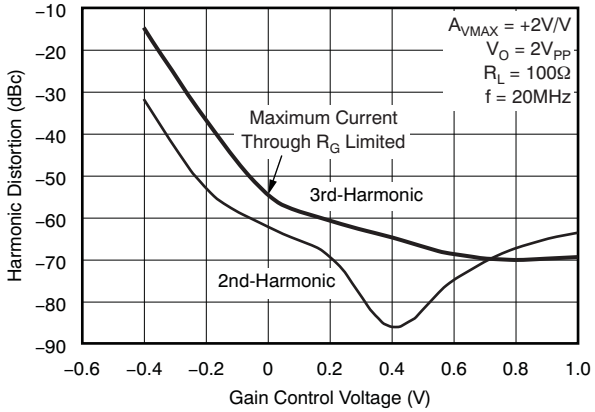

Figure 21.

TWO-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

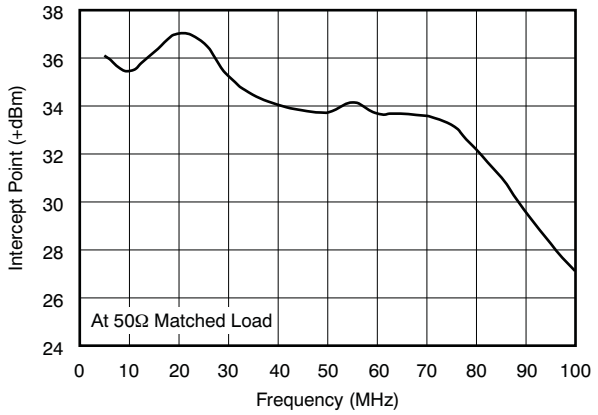

Figure 22.

TWO-TONE, 3RD-ORDER INTERMODULATION INTERCEPT vs GAIN CONTROL VOLTAGE

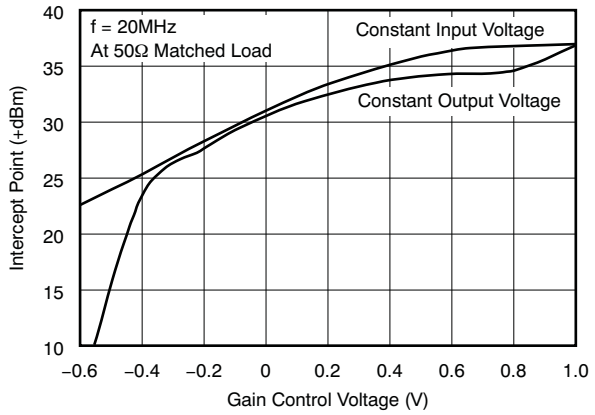

Figure 23.

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TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = +2V/V (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 453Ω, R_G = 453Ω, V_G = +1V, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

GAIN vs GAIN CONTROL VOLTAGE

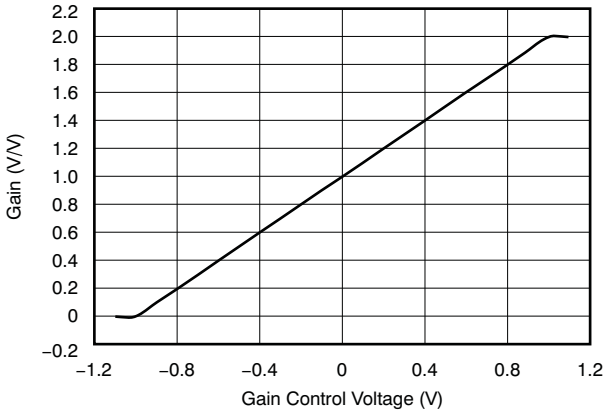

Figure 24.

GAIN CONTROL FREQUENCY RESPONSE

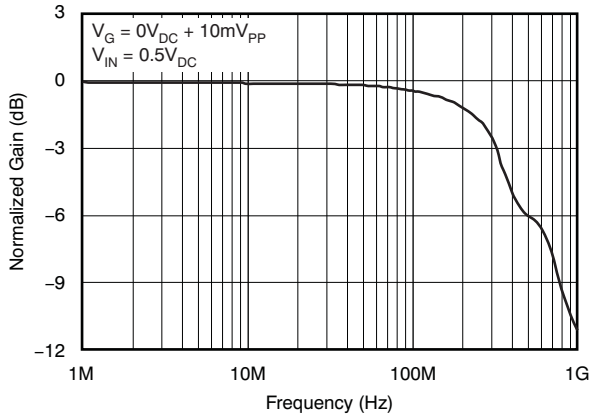

Figure 25.

GAIN CONTROL PULSE RESPONSE

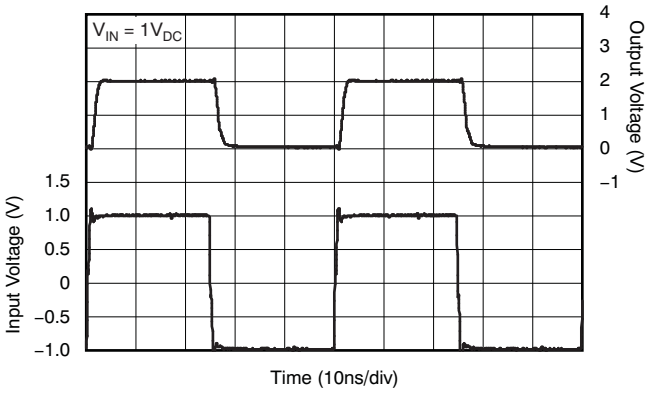

Figure 26.

FULLY-ATTENUATED RESPONSE

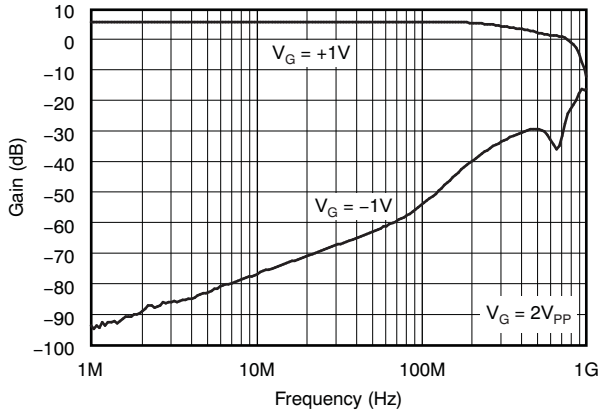

Figure 27.

GROUP DELAY vs GAIN CONTROL VOLTAGE

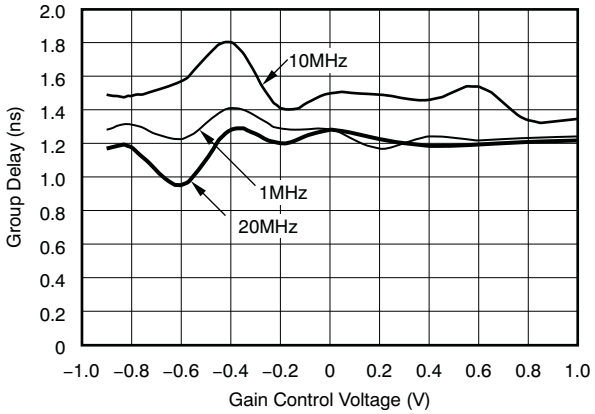

Figure 28.

GROUP DELAY vs FREQUENCY

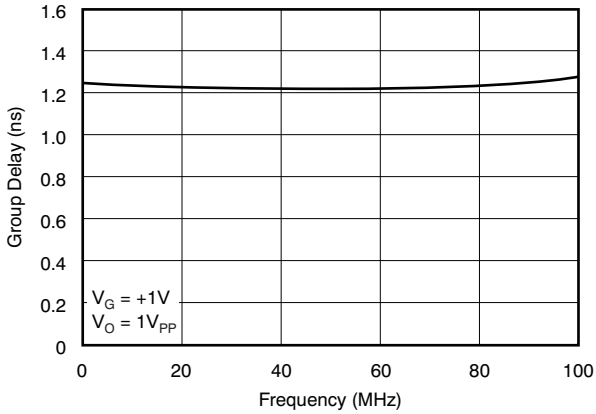

Figure 29.

TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = +2V/V (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 453Ω, R_G = 453Ω, V_G = +1V, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

RECOMMENDED R_S vs CAPACITIVE LOAD

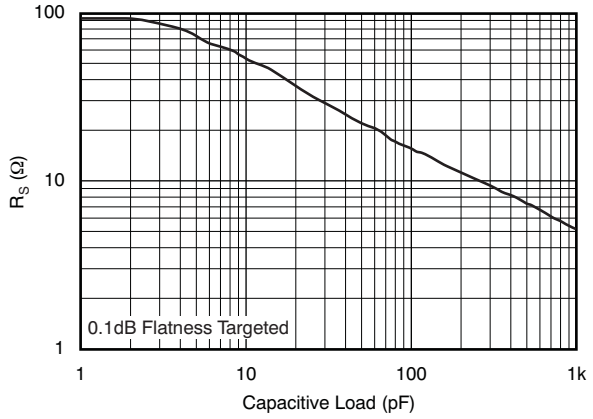

Figure 30.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

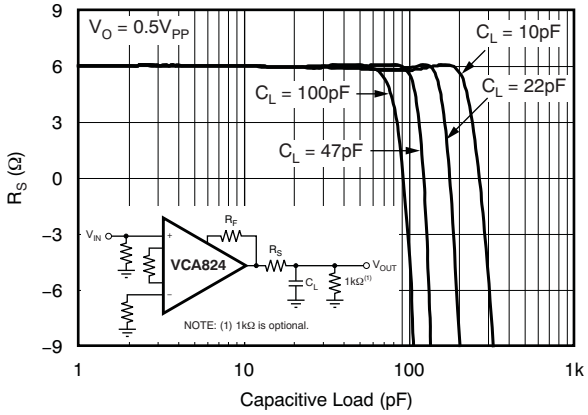

Figure 31.

OUTPUT VOLTAGE NOISE DENSITY

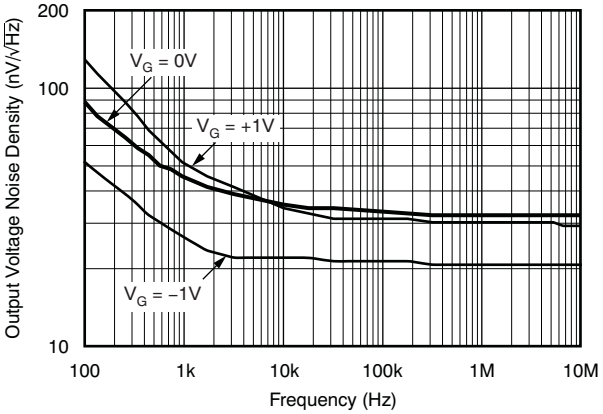

Figure 32.

INPUT CURRENT NOISE DENSITY

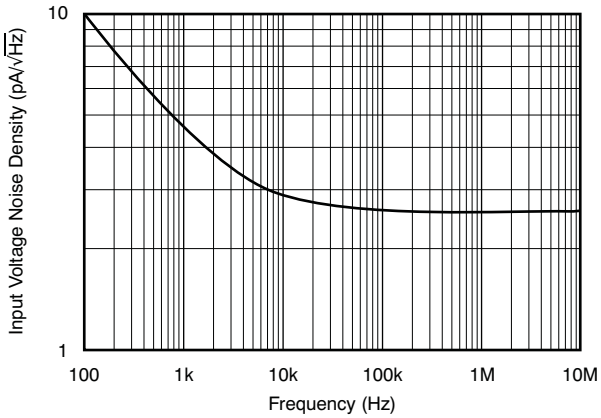

Figure 33.

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TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = +10V/V

At T_A = +25°C, R_L = 100Ω, R_F = 402Ω, R_G = 80Ω, V_G = +1V, and V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

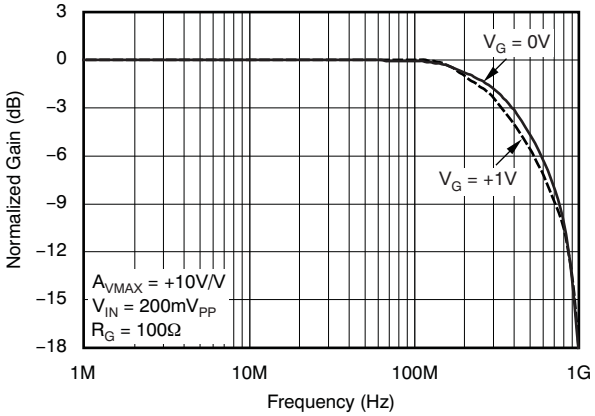

Figure 34.

LARGE-SIGNAL FREQUENCY RESPONSE

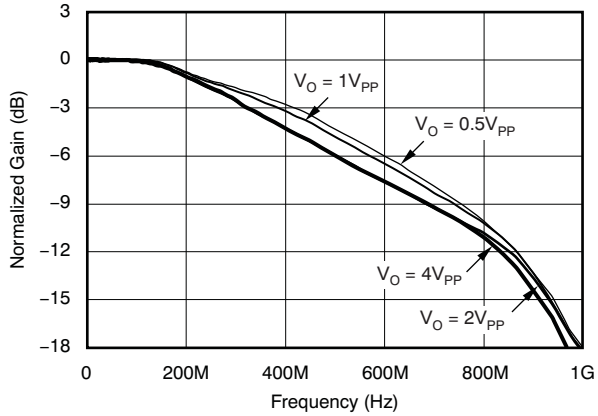

Figure 35.

SMALL-SIGNAL PULSE RESPONSE

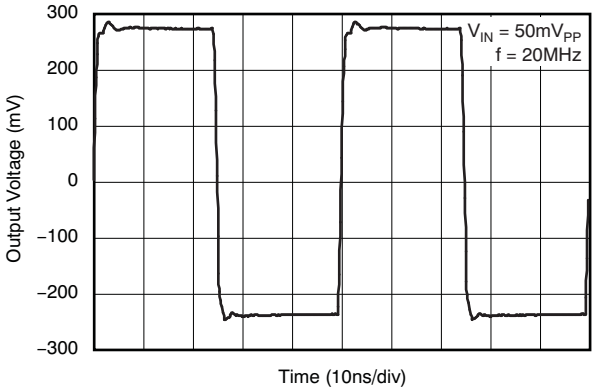

Figure 36.

LARGE-SIGNAL PULSE RESPONSE

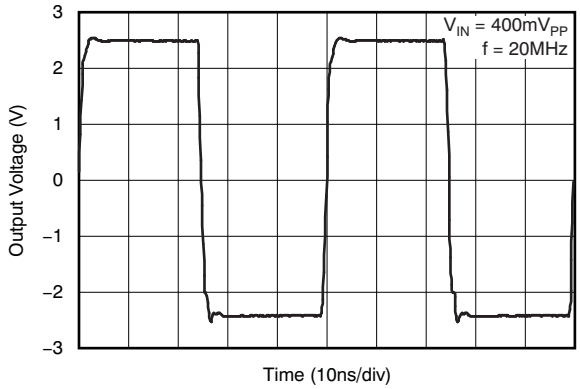

Figure 37.

GAIN FLATNESS, DEVIATION FROM LINEAR PHASE

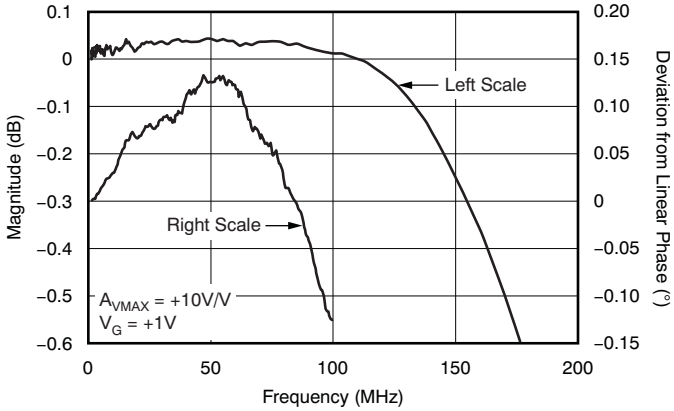

Figure 38.

OUTPUT VOLTAGE NOISE DENSITY

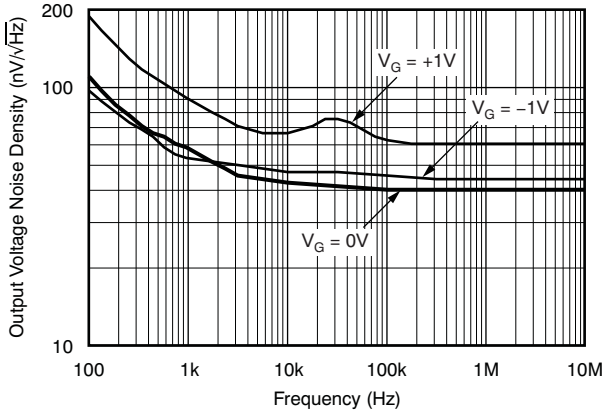

Figure 39.

TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = +10V/V (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 402Ω, R_G = 80Ω, V_G = +1V, and V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

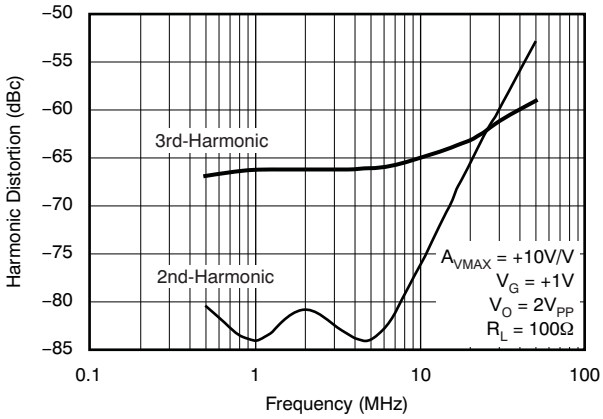

Figure 40.

HARMONIC DISTORTION vs LOAD RESISTANCE

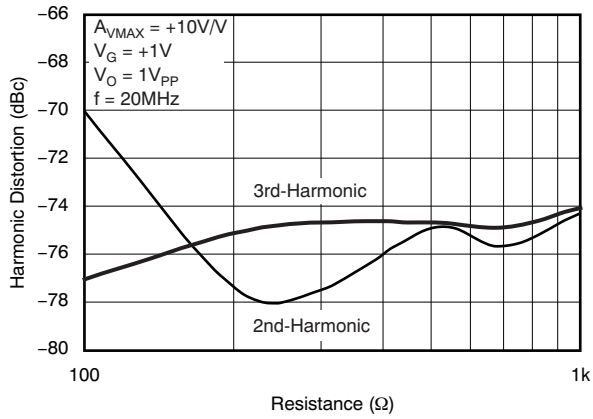

Figure 41.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

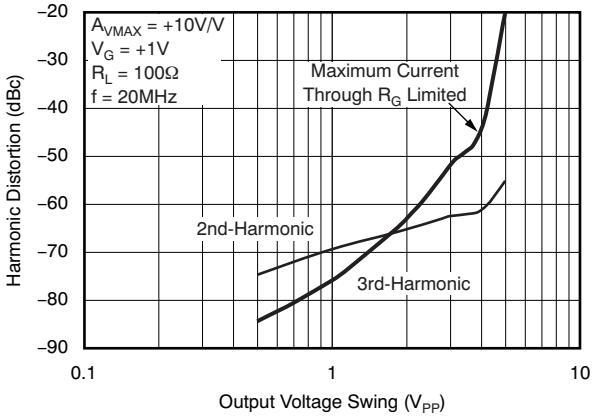

Figure 42.

HARMONIC DISTORTION vs GAIN CONTROL VOLTAGE

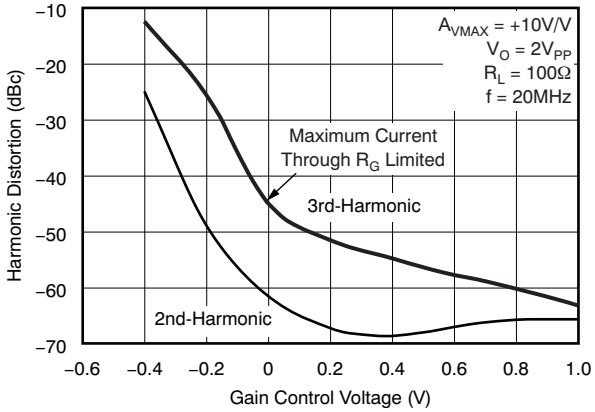

Figure 43.

TWO-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

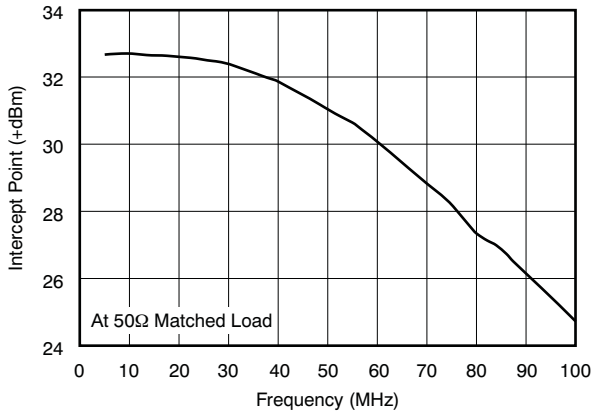

Figure 44.

TWO-TONE, 3RD-ORDER INTERMODULATION INTERCEPT vs GAIN CONTROL VOLTAGE

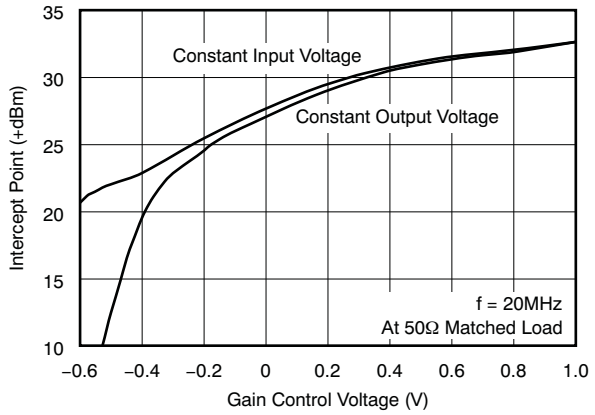

Figure 45.

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TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = +10V/V (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 402Ω, R_G = 80Ω, V_G = +1V, and V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, unless otherwise noted.

GAIN vs GAIN CONTROL VOLTAGE

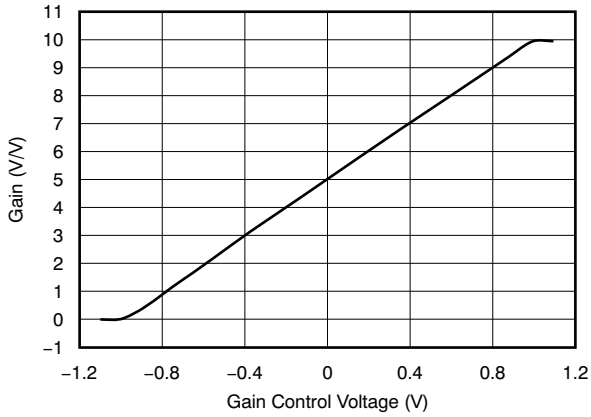

Figure 46.

GAIN CONTROL FREQUENCY RESPONSE

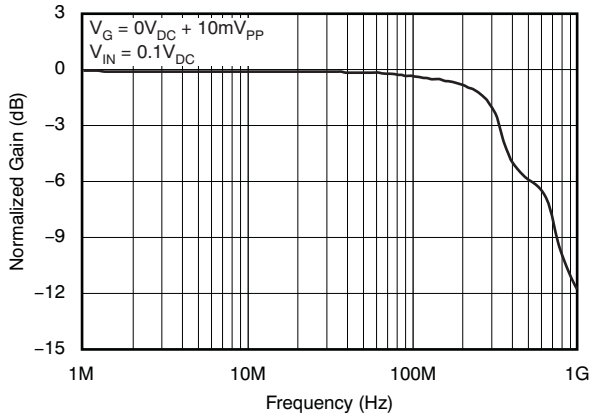

Figure 47.

GAIN CONTROL PULSE RESPONSE

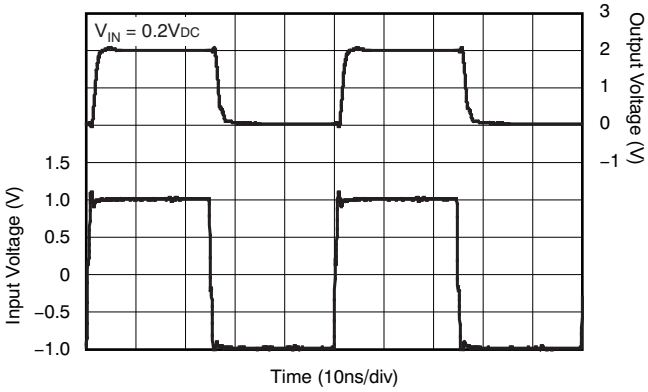

Figure 48.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

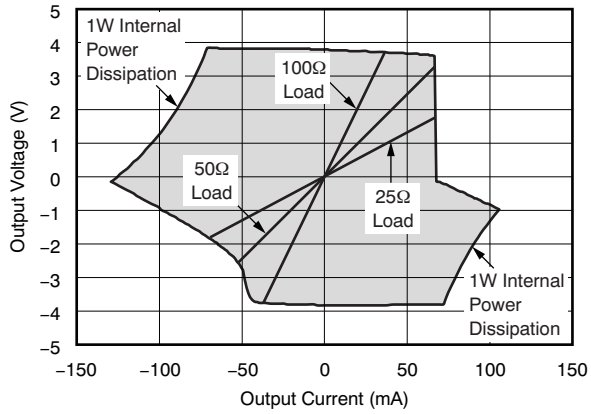

Figure 49.

FULLY-ATTENUATED RESPONSE

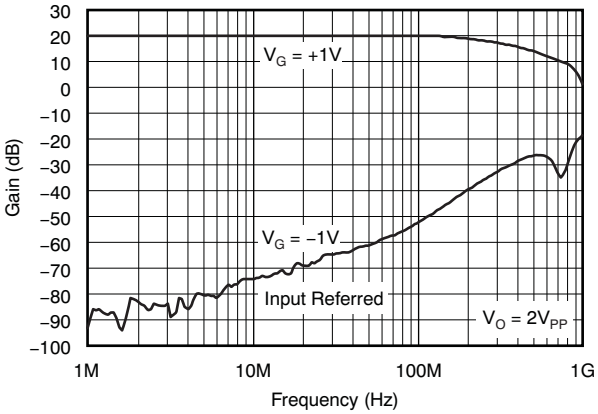

Figure 50.

I_{RG} LIMITED OVERDRIVE RECOVERY

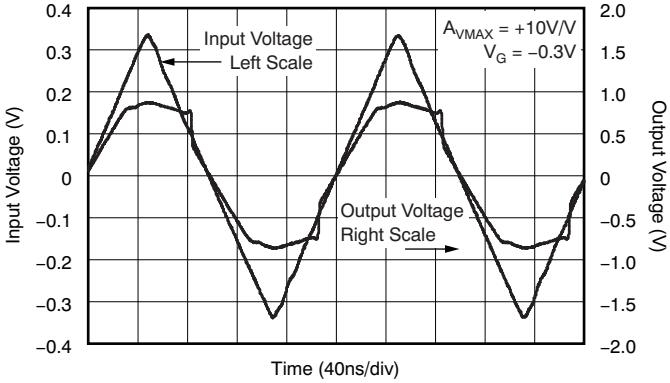

Figure 51.

TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = +10V/V (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 402Ω, R_G = 80Ω, V_G = +1V, and V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, unless otherwise noted.

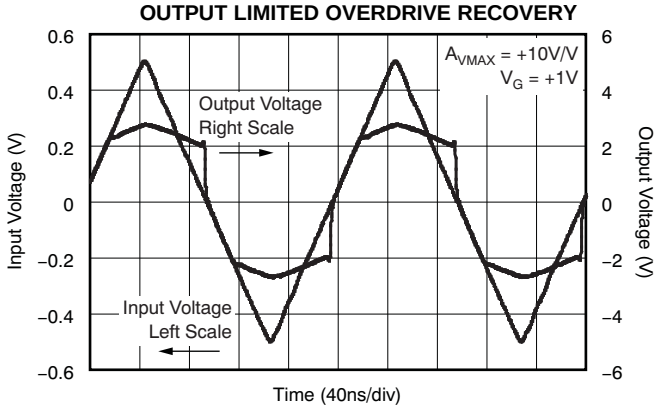

Figure 52.

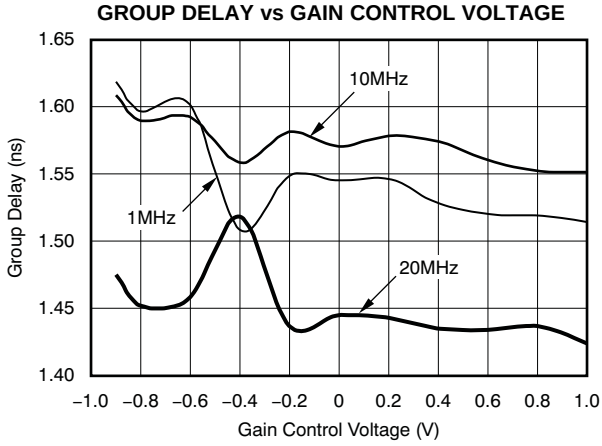

Figure 53.

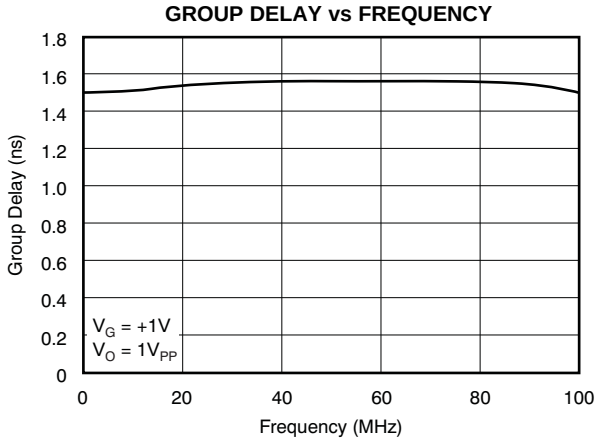

Figure 54.

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TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = +40V/V

At T_A = +25°C, R_L = 100Ω, R_F = 402Ω, R_G = 18Ω, V_G = +1V, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

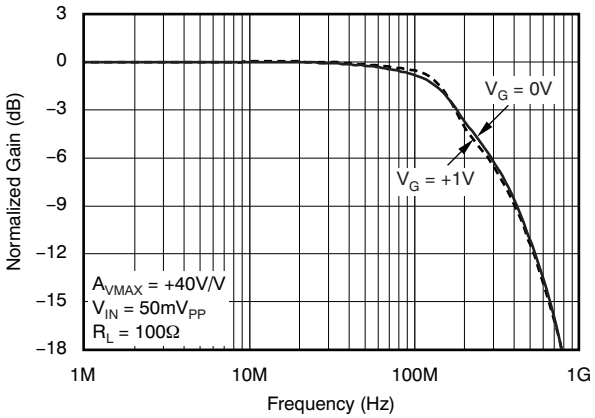

Figure 55.

LARGE-SIGNAL FREQUENCY RESPONSE

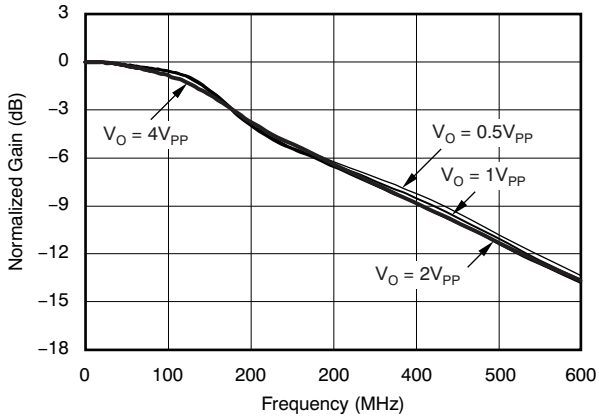

Figure 56.

SMALL-SIGNAL PULSE RESPONSE

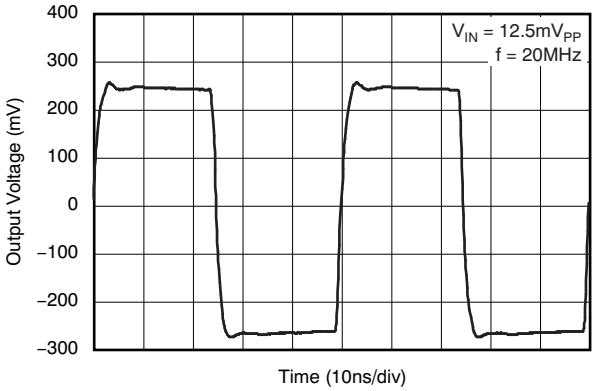

Figure 57.

LARGE-SIGNAL PULSE RESPONSE

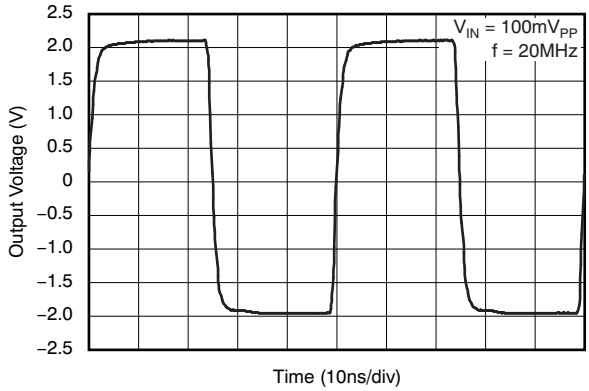

Figure 58.

GAIN FLATNESS, DEVIATION FROM LINEAR PHASE

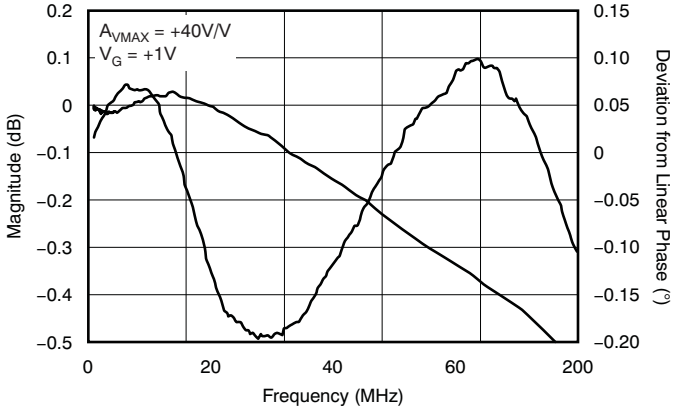

Figure 59.

OUTPUT VOLTAGE NOISE DENSITY

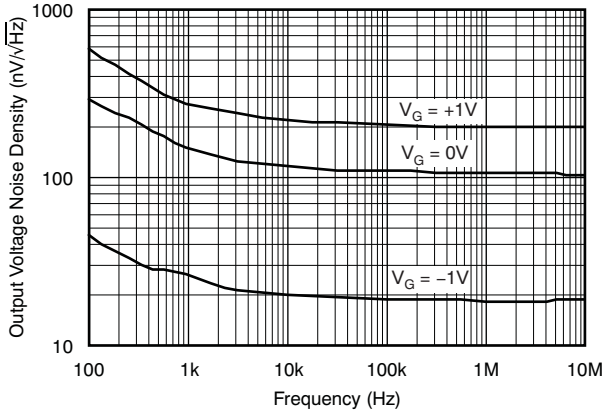

Figure 60.

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TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = +40V/V (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 402Ω, R_G = 18Ω, V_G = +1V, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

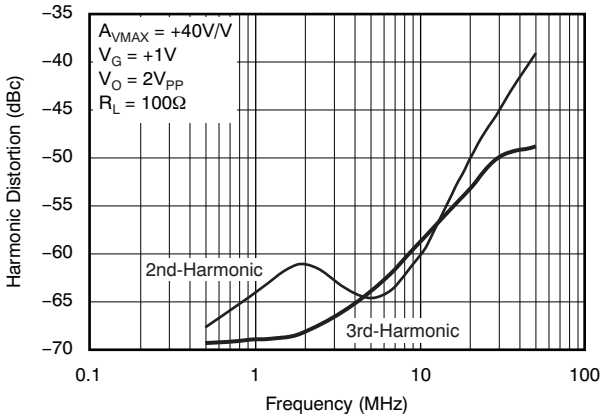

Figure 61.

HARMONIC DISTORTION vs LOAD RESISTANCE

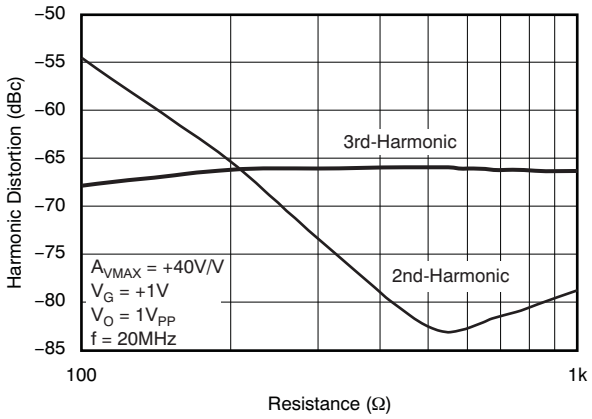

Figure 62.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

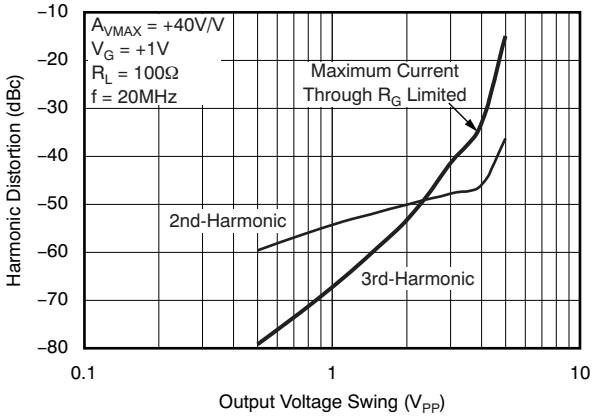

Figure 63.

HARMONIC DISTORTION vs GAIN CONTROL VOLTAGE

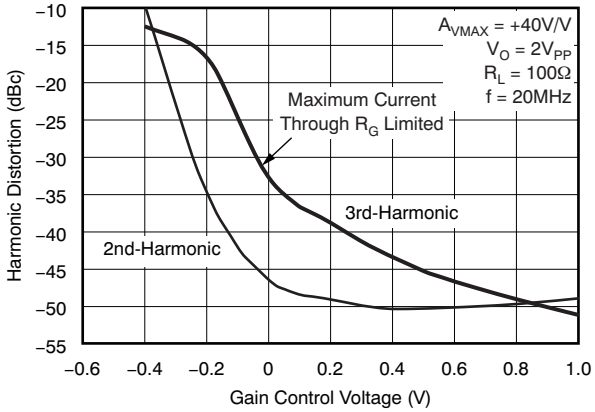

Figure 64.

TWO-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

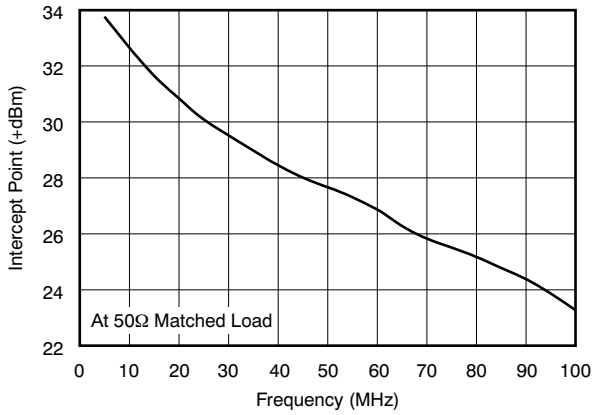

Figure 65.

TWO-TONE, 3RD-ORDER INTERMODULATION INTERCEPT vs GAIN CONTROL VOLTAGE

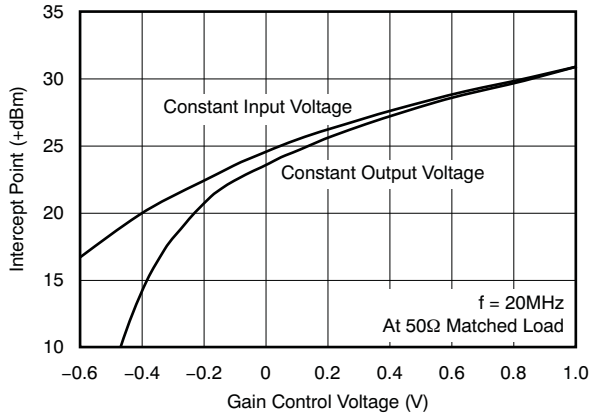

Figure 66.

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TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = +40V/V (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 402Ω, R_G = 18Ω, V_G = +1V, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

GAIN vs GAIN CONTROL VOLTAGE

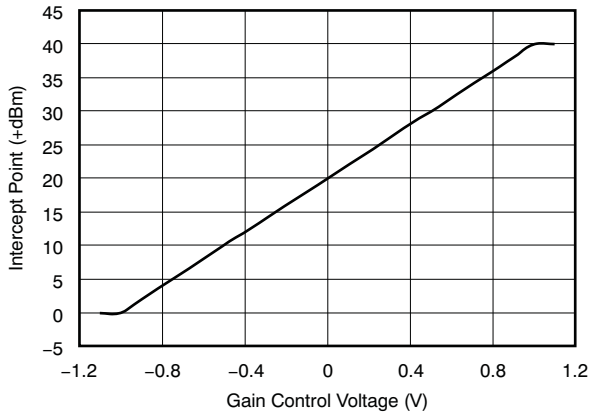

Figure 67.

GAIN CONTROL FREQUENCY RESPONSE

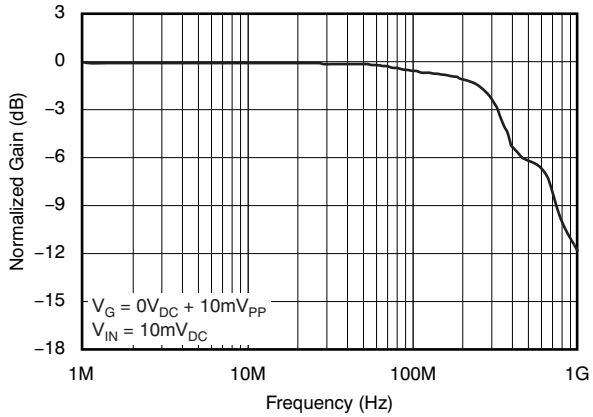

Figure 68.

GAIN CONTROL PULSE RESPONSE

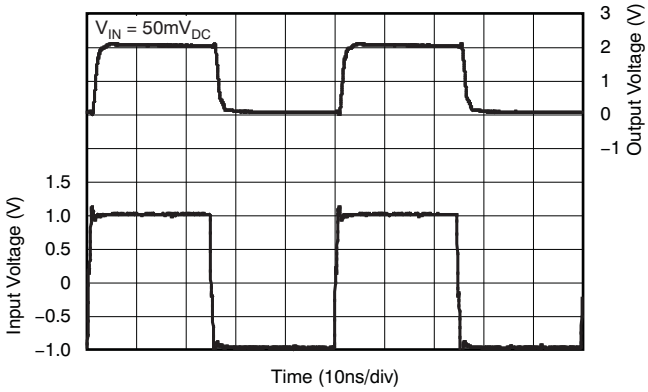

Figure 69.

FULLY ATTENUATED RESPONSE

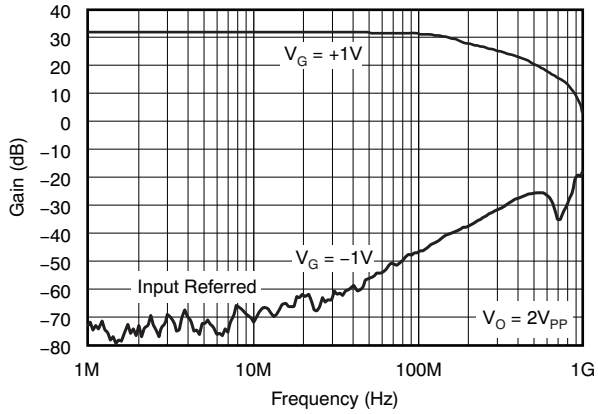

Figure 70.

I_{RG} LIMITED OVERDRIVE RECOVERY

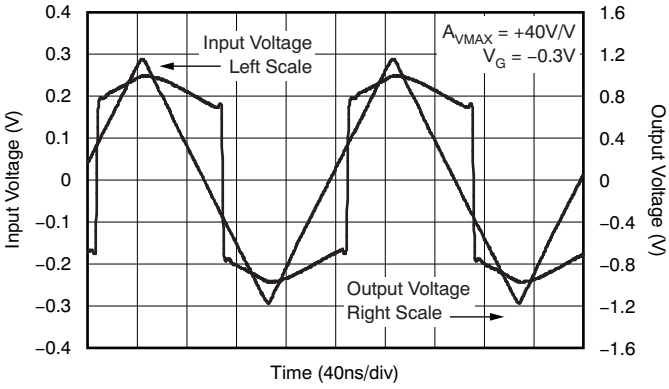

Figure 71.

OUTPUT LIMITED OVERDRIVE RECOVERY

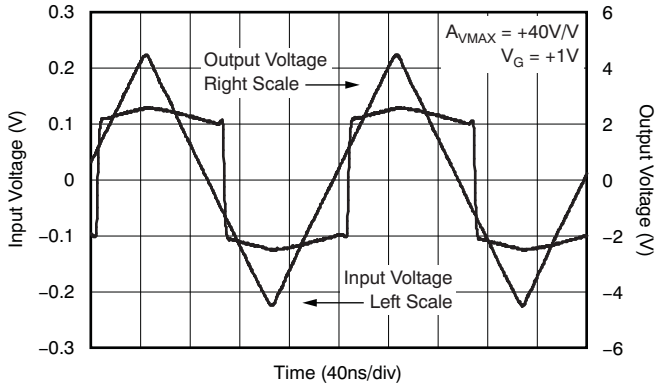

Figure 72.

TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = +40V/V (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 402Ω, R_G = 18Ω, V_G = +1V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

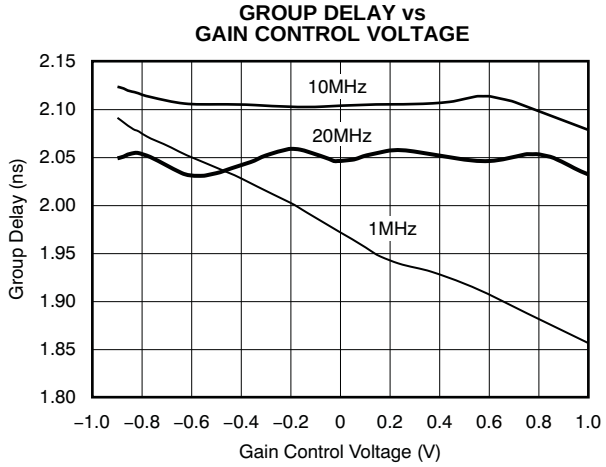

Figure 73.

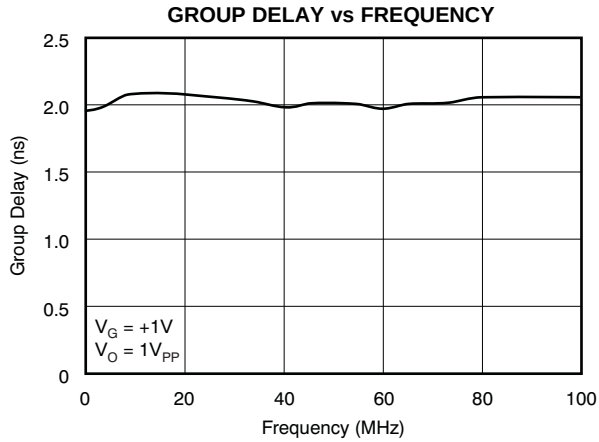

Figure 74.

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APPLICATION INFORMATION

WIDEBAND VARIABLE GAIN AMPLIFIER OPERATION

The VCA824 provides an exceptional combination of high output power capability with a wideband, greater than 40dB gain adjust range, linear in V/V variable gain amplifier. The VCA824 input stage places the transconductance element between two input buffers, using the output currents as the forward signal. As the differential input voltage rises, a signal current is generated through the gain element. This current is then mirrored and gained by a factor of two before reaching the multiplier. The other input of the multiplier is the voltage gain control pin, V_G. Depending on the voltage present on V_G, up to two times the gain current is provided to the transimpedance output stage. The transimpedance output stage is a current-feedback amplifier providing high output current capability and high slew rate, 2500V/µs. This exceptional full-power performance comes at the price of relatively high quiescent current (36.5mA), but low input voltage noise for this type of architecture (6nV/√Hz).

Figure 75 shows the dc-coupled, gain of +10V/V, dual power-supply circuit used as the basis of the ±5V Electrical Characteristics and Typical Characteristics.

For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the Electrical Characteristics table are taken directly at the input and output pins, while output power (dBm) is at the matched 50Ω load. For the circuit in Figure 75, the total effective load is 100Ω ‖ 1kΩ. Note that for the SO-14 package, there is a voltage reference pin, V_{REF} (pin 9). For the SO-14 package, this pin must be connected to ground through a 20Ω resistor in order to avoid possible oscillations of the output stage. In the MSOP-10 package, this pin is internally connected and does not require such precaution. An X2Y® capacitor has been used for power-supply bypassing. The combination of low inductance, high resonance frequency, and integration of three capacitors in one package (two capacitors to ground and one across the supplies) enables the VCA824 to achieve the low second-harmonic distortion reported in the Electrical Characteristics table. More information on how the VCA824 operates can be found in the *Operating Suggestions* section.

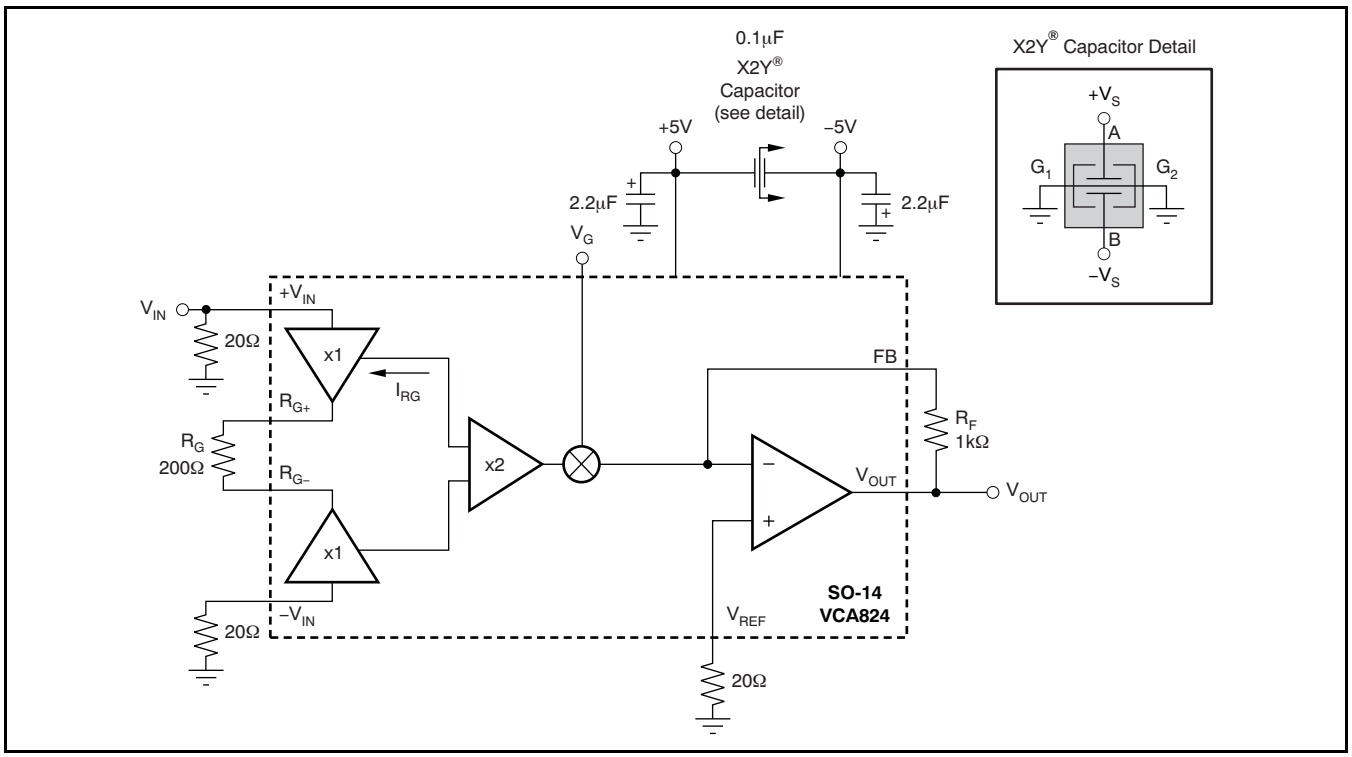

Figure 75. DC-Coupled, A_{VMAX} = +10V/V, Bipolar Supply Specification and Test Circuit

FOUR-QUADRANT MULTIPLIER

A four-quadrant multiplier can easily be implemented using the VCA824. By placing a resistor between FB and V_{IN}, the transfer function depends upon both V_{IN} and V_G, as shown in Equation 1.

$$V_{OUT} = \frac{R_F}{R_G} \times V_G \times V_{IN} + \left(\frac{R_F}{R_G} - \frac{R_F}{R_1}\right) \times V_{IN} \quad (1)$$

Setting R_1 to equal R_G, the term that depends only on V_{IN} drops out of the equation, leaving only the term that depends on both V_G and V_{IN}. V_{OUT} then follows Equation 2.

$$V_{OUT} = \frac{R_F}{R_G} \times V_{IN} \times V_G \quad (2)$$

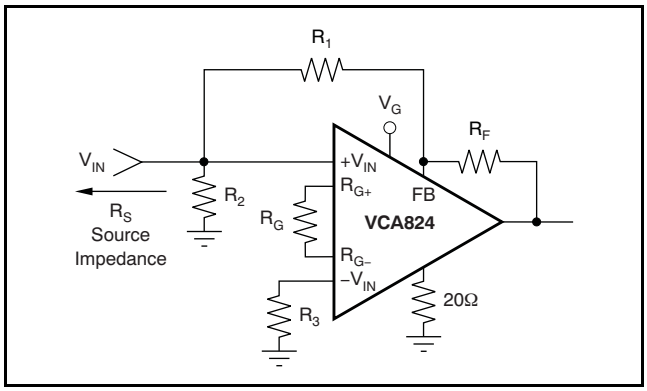

Figure 76. Four-Quadrant Multiplier Circuit

Figure 77 illustrates the behavior of this circuit. Keeping the input amplitude of a 1MHz signal constant and varying the V_G voltage (100kHz, $2V_{PP}$) gives the modulated output voltage shown in Figure 77.

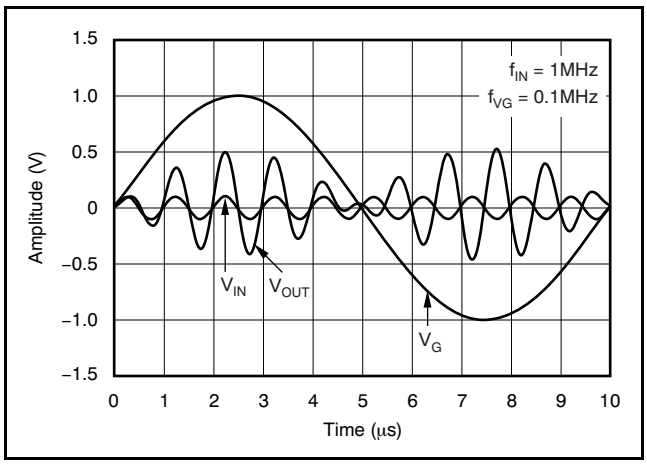

Figure 77. Modulated Output Signal of the 4-Quadrant Multiplexer Circuit

DIFFERENCE AMPLIFIER

Because both inputs of the VCA824 are high-impedance, a difference amplifier can be implemented without any major problem. Figure 78 shows this implementation. This circuit provides excellent common-mode rejection ratio (CMRR) as long as the input is within the CMRR range of –2.1V to +1.6V. Note that this circuit does not make use of the gain control pin, V_G. Also, it is recommended to choose R_S such that the pole formed by R_S and the parasitic input capacitance does not limit the bandwidth of the circuit. Figure 79 shows the common-mode rejection ratio for this circuit implemented in a gain of +10V/V for V_G = +1V. Note that because the gain control voltage is fixed and is normally set to +1V, the feedback element can be reduced in order to increase the bandwidth. When reducing the feedback element, make sure that the VCA824 is not limited by common-mode input voltage, the current flowing through R_G, or any other limitation described in this data sheet.

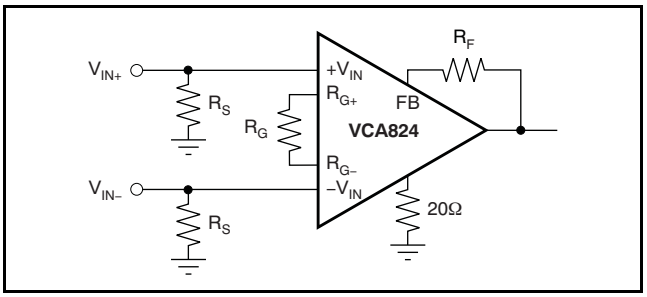

Figure 78. Difference Amplifier

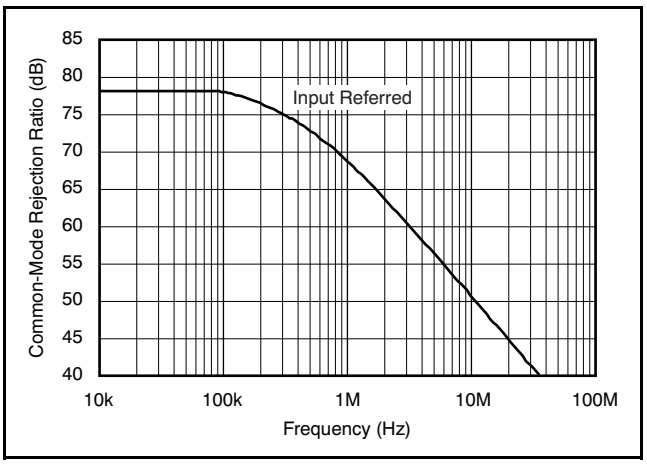

Figure 79. Common-Mode Rejection Ratio

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DIFFERENTIAL EQUALIZER

If the application requires frequency shaping (the transition from one gain to another), the VCA824 can be used advantageously because its architecture allows the application to isolate the input from the gain setting elements. Figure 80 shows an implementation of such a configuration. The transfer function is shown in Equation 3.

$$G = 2 \times \frac{R_F}{R_G} \times \frac{1 + sR_GC_1}{1 + sR_1C_1} \quad (3)$$

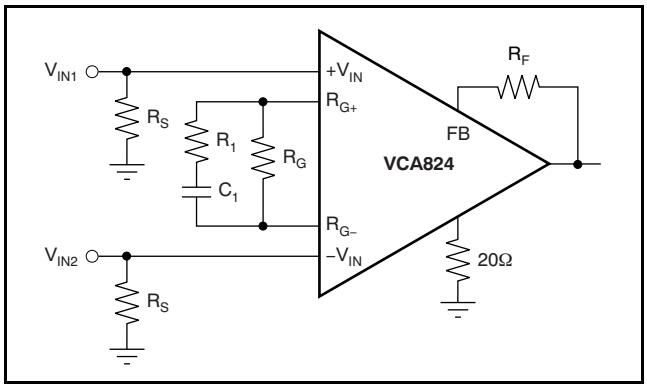

Figure 80. Differential Equalizer

This transfer function has one pole, P_1 (located at R_GC_1), and one zero, Z_1 (located at R_1C_1). When equalizing an RC load, R_L and C_L, compensate the pole added by the load located at R_LC_L with the zero Z_1. Knowing R_L, C_L, and R_G allows the user to select C_1 as a first step and then calculate R_1. Using R_L = 75Ω, C_L = 100pF and wanting the VCA824 to operate at a gain of +2V/V, which gives $R_F = R_G$ = 453kΩ, allows the user to select C_1 = 15.5pF to ensure a positive value for the resistor R_1. With all these values known, to achieve greater than 300MHz bandwidth, R_1 can be calculated to be 20Ω. Figure 81 shows the frequency response for both the initial, unequalized frequency response and the resulting equalized frequency response.

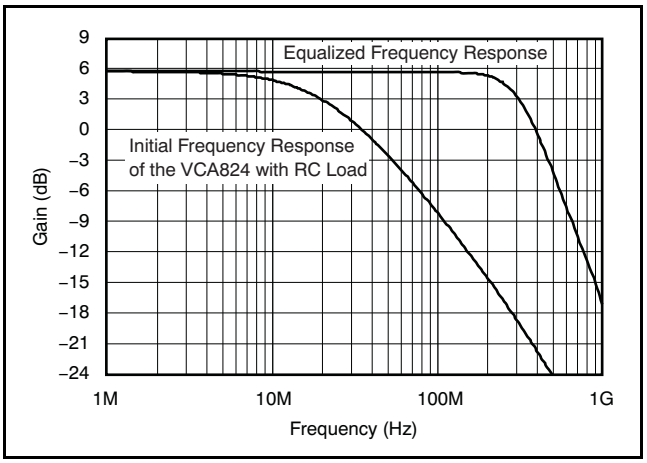

Figure 81. Differential Equalization of an RC Load

DIFFERENTIAL CABLE EQUALIZER

A differential cable equalizer can easily be implemented using the VCA824. An example of a cable equalization for 100 feet of Belden Cable 1694F is illustrated in Figure 83, with Figure 82 showing the result for this implementation. This implementation has a maximum error of 0.2dB from dc to 70MHz.

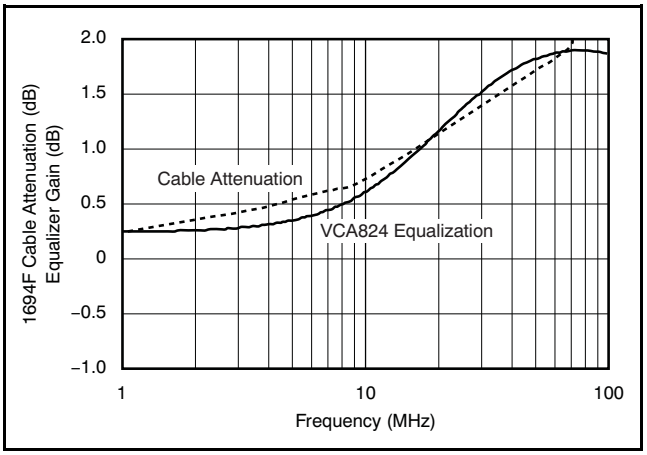

Figure 82. Cable Attenuation versus Equalizer Gain

Note that this implementation shows the cable attenuation side-by-side with the equalization in the same plot. For a given frequency, the equalization function realized with the VCA824 matches the cable attenuation. The circuit in Figure 83 is a driver circuit. To implement a receiver circuit, the signal is received differentially between the $+V_{IN}$ and $-V_{IN}$ inputs.

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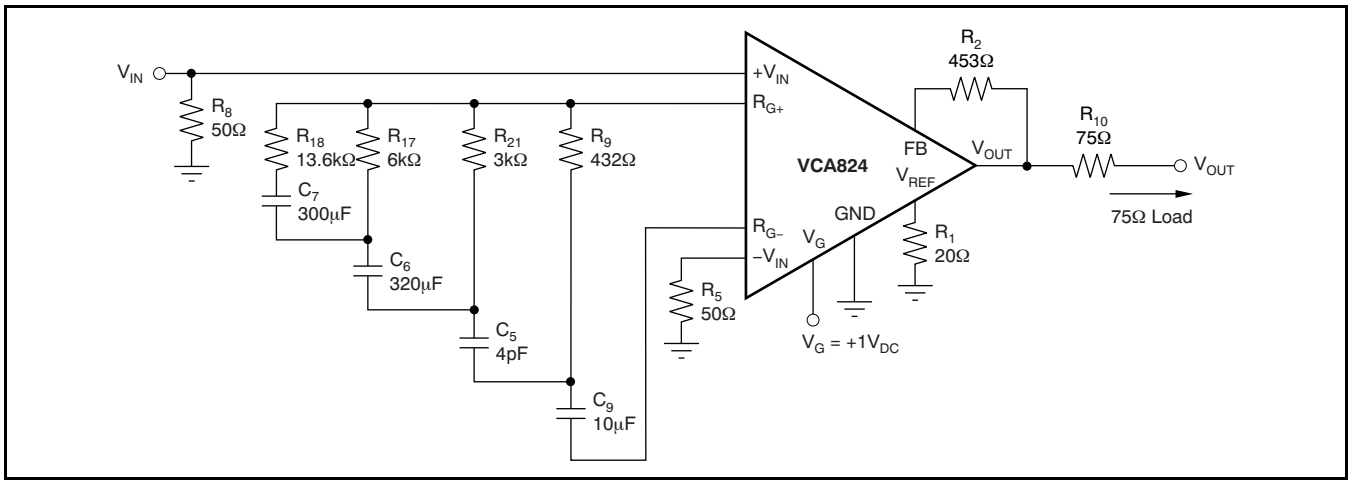

Figure 83. Differential Cable Equalizer

VOLTAGE-CONTROLLED LOW-PASS FILTER

In the circuit of Figure 84, the VCA824 serves as the variable-gain element of a voltage-controlled low-pass filter. This section discusses how this implementation expands the circuit voltage swing capability over that normally achieved with the equivalent multiplier implementation. The circuit control voltage, V_G, is calculated as according to the simplified relationship described in Equation 4:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1} \times \frac{1}{1 + s\frac{R_2C}{G}} \tag{4}$$

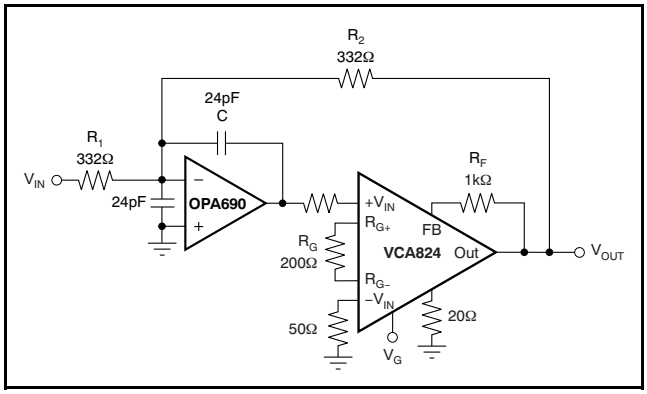

Figure 84. Voltage-Control Low-Pass Filter

The response control results from amplification of the feedback voltage applied to R_2. First, consider the case where the VCA824 produces G = 1V/V. Then this circuit performs as if the amplifier were replaced by a short circuit. Visually replacing the amplifier by a short leaves a simple voltage-feedback amplifier with a feedback resistor bypassed by a capacitor. Replacing this gain with a variable gain, G, the pole can be written as shown in Equation 5:

$$f_8 = \frac{G}{2\pi R_2 C} \tag{5}$$

Because the VCA824 is most linear in the midrange, the median of the adjustable pole should be set at V_G = 0V (see Figure 24, Figure 44, Figure 65, and Equation 6). Selecting $R_1 = R_2 = 332\Omega$, and targeting a median frequency of 10MHz, the capacitance (C) is 24pF. Because the OPA690 was selected for the circuit of Figure 84, and in order to limit peaking in the OPA690 frequency response, a capacitor equal to C was added on the inverting mode to ground. This architecture has the effect of setting the high-frequency noise gain of the OPA690 to +2V/V, ensuring stability and providing flat frequency response.

$$-0.8V \le V_G \le 0.8V \tag{6}$$

Once the median frequency is set, the maximum and minimum frequencies can be determined by using V_G = –0.8V and V_G = +0.8V in the gain equation of Equation 7. Note that this is a first-order analysis and does not take into consideration the open-loop gain limitation of the OPA690.

$$G = 2 \times \frac{R_F}{R_G} \times \frac{V_G + 1}{2} \tag{7}$$

With the components shown, the circuit provides a linear variation of the low-pass cutoff from 2MHz to 20MHz, using $-1V \le V_G \le +1V$.

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DESIGN-IN TOOLS

DEMONSTRATION BOARDS

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the VCA824 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. EVM Ordering Information

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE REQUEST NUMBER
VCA824ID	SO-14	DEM-VCA-SO-1B	SBOU050
VCA824IDGS	MSOP-10	DEM-VCA-MSOP-1A	SBOU051

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the VCA824 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This principle is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role in circuit performance. A SPICE model for the VCA824 is available through the TI web page. The applications group is also available for design assistance. The models available from TI predict typical small-signal ac performance, transient steps, dc performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the relevant product data sheet.

OPERATING SUGGESTIONS

Operating the VCA824 optimally for a specific application requires trade-offs between bandwidth, input dynamic range and the maximum input voltage, the maximum gain of operation and gain, output dynamic range and the maximum input voltage, the package used, loading, and layout and bypass recommendations. The Typical Characteristics have been defined to cover as much ground as possible to describe the VCA824 operation. There are four sections in the Typical Characteristics:

- V_S = ±5V DC Parameters and V_S = ±5V DC and Power-Supply Parameters, which include dc operation and the intrinsic limitation of a VCA824 design
- V_S = ±5V, A_{VMAX} = +2V/V Gain of +2V/V Operation
- V_S = ±5V, A_{VMAX} = +10V/V Gain of +10V/V Operation
- V_S = ±5V, A_{VMAX} = +40V/V Gain of +40V/V Operation

Where the Typical Characteristics describe the actual performance that can be achieved by using the amplifier properly, the following sections describe in detail the trade-offs needed to achieve this level of performance.

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PACKAGE CONSIDERATIONS

The VCA824 is available in both SO-14 and MSOP-10 packages. Each package has, for the different gains used in the typical characteristics, different values of R_F and R_G in order to achieve the same performance detailed in the Electrical Characteristics table.

Figure 85 shows a test gain circuit for the VCA824. Table 2 lists the recommended configuration for the SO-14 and MSOP-10 packages.

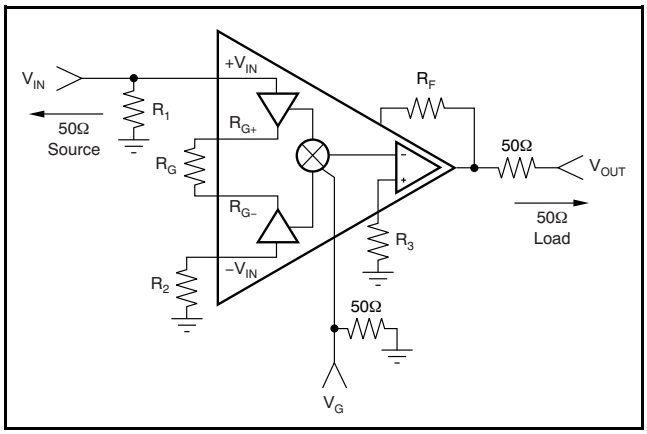

Figure 85. Test Circuit

Table 2. SO-14 and MSOP-10 R_F and R_G Configurations

	G = 2	G = 10	G = 100
R_F	453Ω	402Ω	402Ω
R_G	453Ω	80Ω	18Ω

There are no differences between the packages in the recommended values for the gain and feedback resistors. However, the bandwidth for the VCA824IDGS (MSOP-10 package) is lower than the bandwidth for the VCA824ID (SO-14 package). This difference is true for all gains, but especially true for gains greater than 5V/V, as can be seen in Figure 86 and Figure 87. Note that the scale must be changed to a linear scale to view the details.

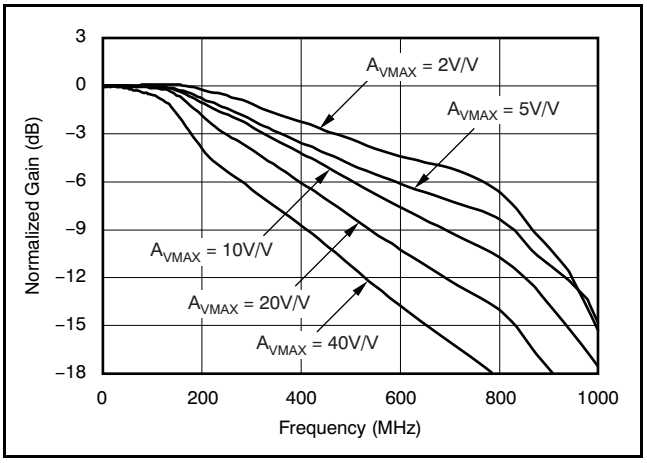

Figure 86. SO-14 Recommended R_F and R_G versus A_{VMAX}

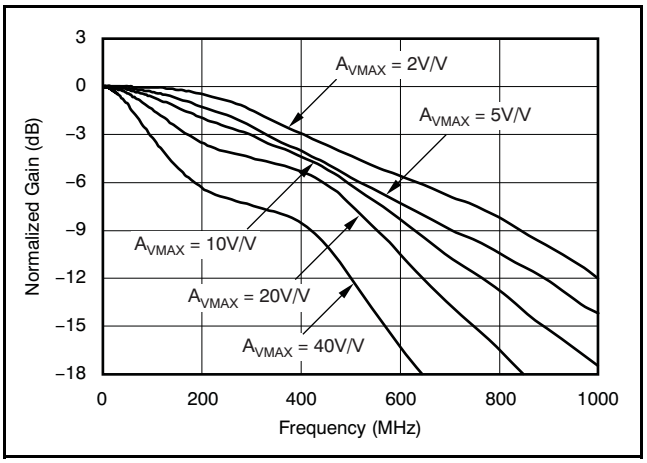

Figure 87. MSOP-10 Recommended R_F and R_G versus A_{VMAX}

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MAXIMUM GAIN OF OPERATION

This section describes the use of the VCA824 in a fixed-gain application in which the V_G control pin is set at V_G = +1V. The tradeoffs described here are with bandwidth, gain, and output voltage range.

In the case of an application that does not make use of the V_{GAIN}, but requires some other characteristic of the VCA824, the R_G resistor must be set such that the maximum current flowing through the resistance I_{RG} is less than ±2.6mA typical, or 5.2mA$_{PP}$ as defined in the Electrical Characteristics table, and must follow Equation 8.

$$I_{RG} = \frac{V_{OUT}}{A_{VMAX} \times R_G} \tag{8}$$

As Equation 8 illustrates, once the output dynamic range and maximum gain are defined, the gain resistor is set. This gain setting in turn affects the bandwidth, because in order to achieve the gain (and with a set gain element), the feedback element of the output stage amplifier is set as well. Keeping in mind that the output amplifier of the VCA824 is a current-feedback amplifier, the larger the feedback element, the lower the bandwidth because the feedback resistor is the compensation element.

Limiting the discussion to the input voltage only and ignoring the output voltage and gain, Figure 1 illustrates the tradeoff between the input voltage and the current flowing through the gain resistor.

OUTPUT CURRENT AND VOLTAGE

The VCA824 provides output voltage and current capabilities that are unsurpassed in a low-cost monolithic VCA. Under no-load conditions at +25°C, the output voltage typically swings closer than 1V to either supply rails; the +25°C swing limit is within 1.2V of either rails. Into a 15Ω load (the minimum tested load), it is tested to deliver more than ±160mA.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage × current, or *V-I product*, that is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot (Figure 49) in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the VCA824 output drive capabilities, noting that the graph is bounded by a *Safe Operating Area* of 1W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the VCA824 can drive ±2.5V into 25Ω or ±3.5V into 50Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±3.9V output swing capability, as shown in the Typical Characteristics.

The minimum specified output voltage and current over-temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup do the output current and voltage decrease to the numbers shown in the Electrical Characteristic tables. As the output transistors deliver power, the respective junction temperatures increase, thereby increasing the available output voltage swing and output current.

In steady-state operation, the available output voltage and current are always greater than the temperature shown in the over-temperature specifications because the output stage junction temperatures are higher than the specified operating ambient.

INPUT VOLTAGE DYNAMIC RANGE

The VCA824 has a input dynamic range limited to +1.6V and –2.1V. Increasing the input voltage dynamic range can be done by using an attenuator network on the input. If the VCA824 is trying to regulate the amplitude at the output, such as in an AGC application, the input voltage dynamic range is directly proportional to Equation 9.

$$V_{IN(PP)} = R_G \times I_{RG(PP)} \tag{9}$$

As such, for unity-gain or under-attenuated conditions, the input voltage must be limited to the CMIR of ±1.6V (3.2V$_{PP}$) and the current (I_{RQ}) must flow through the gain resistor, ±2.6mA (5.2mA$_{PP}$). This configuration sets a minimum value for R_E such that the gain resistor must be greater than Equation 10.

$$R_{GMIN} = \frac{3.2V_{PP}}{5.2mA_{PP}} = 615.4\Omega \tag{10}$$

Values lower than 615.4Ω are gain elements that result in reduced input range, as the dynamic input range is limited by the current flowing through the gain resistor R_G (I_{RG}). If the I_{RG} current limits the performance of the circuit, the input stage of the VCA824 goes into overdrive, resulting in limited output voltage range. Such I_{RG}-limited overdrive conditions are shown in Figure 51 for the gain of +10V/V and Figure 71 for the +40V/V gain.

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OUTPUT VOLTAGE DYNAMIC RANGE

With its large output current capability and its wide output voltage swing of ±3.9V typical on 100Ω load, it is easy to forget other types of limitations that the VCA824 can encounter. For these limitations, careful analysis must be done to avoid input stage limitation: either voltage or I_{RG} current. Note that if control pin V_G varies, the gain limitation may affect other aspects of the circuit.

BANDWIDTH

The output stage of the VCA824 is a wideband current-feedback amplifier. As such, the feedback resistance is the compensation of the last stage. Reducing the feedback element and maintaining the gain constant limits the useful range of I_{RG}, and therefore, reduces the gain adjust range. For a given gain, reducing the gain element limits the maximum achievable output voltage swing.

OFFSET ADJUSTMENT

As a result of the internal architecture used on the VCA824, the output offset voltage originates from the output stage and from the input stage and multiplier core. Figure 88 shows how to compensate both sources of the output offset voltage. Use this procedure to compensate the output offset voltage: starting with the output stage compensation, set V_G = –1V to eliminate all offset contribution of the input stage and multiplier core. Adjust the output stage offset compensation potentiometer. Finally, set V_G = +1V to the maximum gain and adjust the input stage and multiplier core potentiometer. This procedure effectively eliminates all offset contribution at the maximum gain. Because adjusting the gain modifies the contribution of the input stage and the multiplier core, some residual output offset voltage remains.

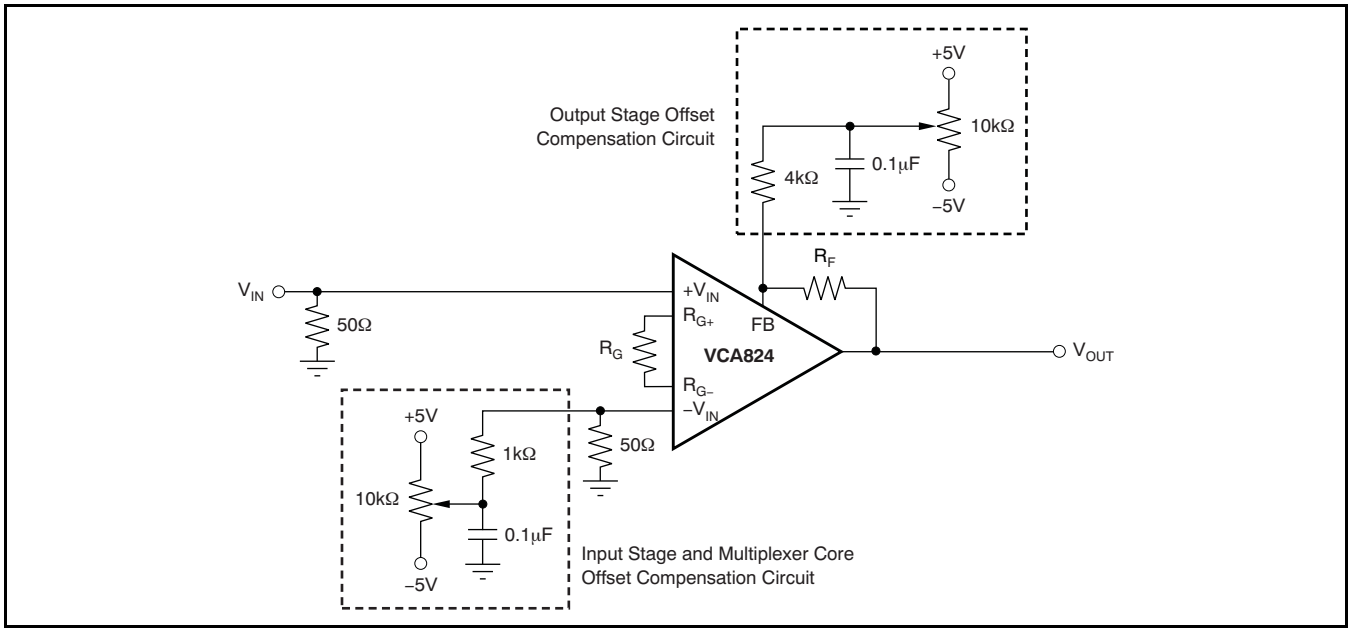

Figure 88. Adjusting the Input and Output Voltage Sources

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NOISE

The VCA824 offers 6nV/√Hz input-referred voltage noise density at a gain of +10V/V and 2.6pA/√Hz input-referred current noise density. The input-referred voltage noise density considers that all noise terms (except the input current noise but including the thermal noise of both the feedback resistor and the gain resistor) are expressed as one term.

This model is formulated in Equation 11 and Figure 89.

$$e_O = A_{VMAX} \times \sqrt{2 \times (R_S \times i_n)^2 + e_n^2 + 2 \times 4kTR_S} \quad (11)$$

A more complete model is shown in Figure 90. For additional information on this model and the actual modeled noise terms, please contact the High-Speed Product Application Support team at www.ti.com.

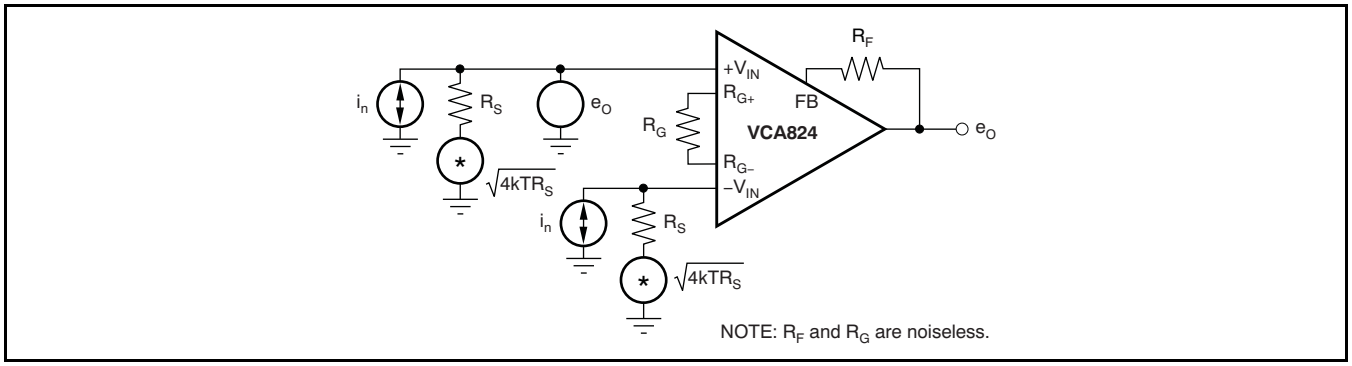

Figure 89. Simple Noise Model

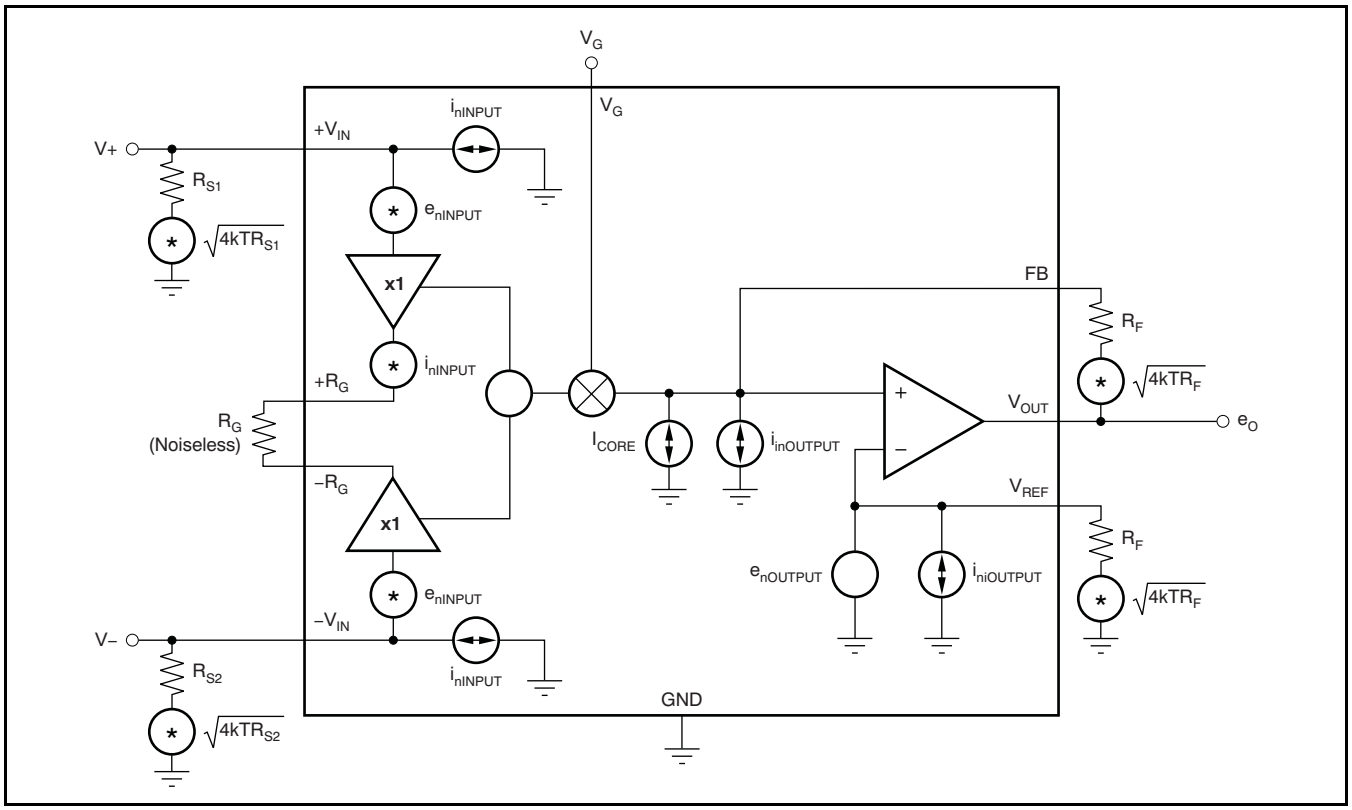

Figure 90. Full Noise Model

THERMAL ANALYSIS

The VCA824 does not require heatsinking or airflow in most applications. The maximum desired junction temperature sets the maximum allowed internal power dissipation as described in this section. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by Equation 12:

$$T_J = T_A + P_D \times \theta_{JA} \quad (12)$$

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load; for a grounded resistive load, however, it is at a maximum when the output is fixed at a voltage equal to one-half of either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S^2/(4 \times R_L)$, where R_L is the resistive load.

Note that it is the power in the output stage and not in the load that determines internal power dissipation. As a worst-case example, compute the maximum T_J using a VCA824ID (SO-14 package) in the circuit of Figure 75 operating at maximum gain and at the maximum specified ambient temperature of +85°C.

$$P_D = 10V(38.5mA) + 5^2/(4 \times 100\Omega) = 447.5mW \quad (13)$$

$$\text{Maximum } T_J = +85°C + (0.449W \times 80°C/W) = 120.8°C \quad (14)$$

This maximum operating junction temperature is well below most system level targets. Most applications should be lower because an absolute worst-case output stage power was assumed in this calculation of $V_{CC}/2$, which is beyond the output voltage range for the VCA824.

BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier such as the VCA824 requires careful attention to printed circuit board (PCB) layout parasitics and external component types. Recommendations to optimize performance include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. This recommendation includes the ground pin (pin 2). Parasitic capacitance on the output can cause instability: on both the inverting input and the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board. Place a small series resistance (greater than 25Ω) with the input pin connected to ground to help decouple package parasitics.

b) Minimize the distance (less than 0.25 inches) from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These capacitors may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components preserve the high-frequency performance of the VCA824. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Because the output pin is the most sensitive to parasitic capacitance, always position the series output resistor, if any, as close as possible to the output pin. Other network components, such as inverting or non-inverting input termination resistors, should also be placed close to the package.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils, or 1.27mm to 2.54mm) should be used, preferably with ground and power planes opened up around them.

e) Socketing a high-speed part like the VCA824 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the VCA824 onto the board.

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INPUT AND ESD PROTECTION

The VCA824 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table.

All pins on the VCA824 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply, as shown in Figure 91. These diodes begin to conduct when the pin voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To ensure long-term reliability, however, diode current should be externally limited to 10mA whenever possible.

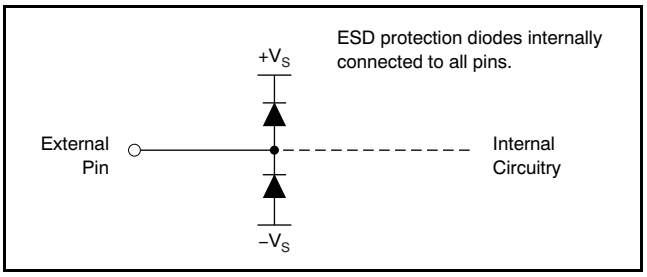

Figure 91. Internal ESD Protection

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2008) to Revision C	Page
• Revised second paragraph in the *Wideband Variable Gain Amplifier Operation* section describing pin 9	19

Changes from Revision A (December 2007) to Revision B	Page
• Changed storage temperature range rating in *Absolute Maximum Ratings* table from –40°C to +125°C to –65°C to +125°C	2

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
VCA824ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
VCA824IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
VCA824IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
VCA824IDGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
VCA824IDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
VCA824IDGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
VCA824IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
VCA824IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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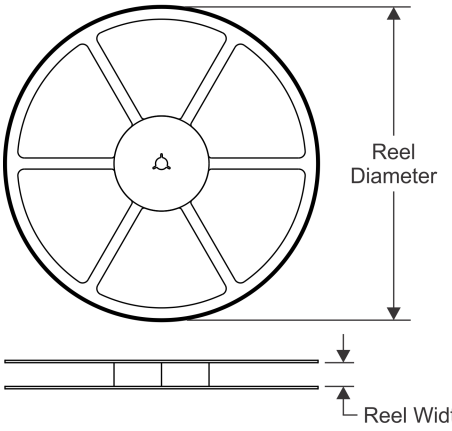
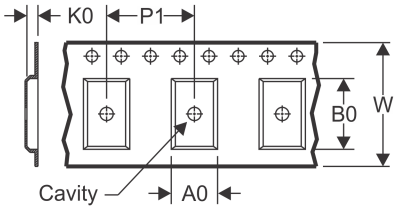
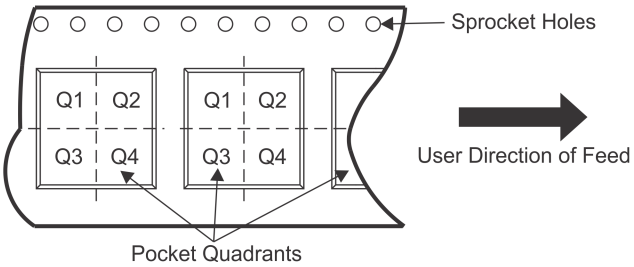


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

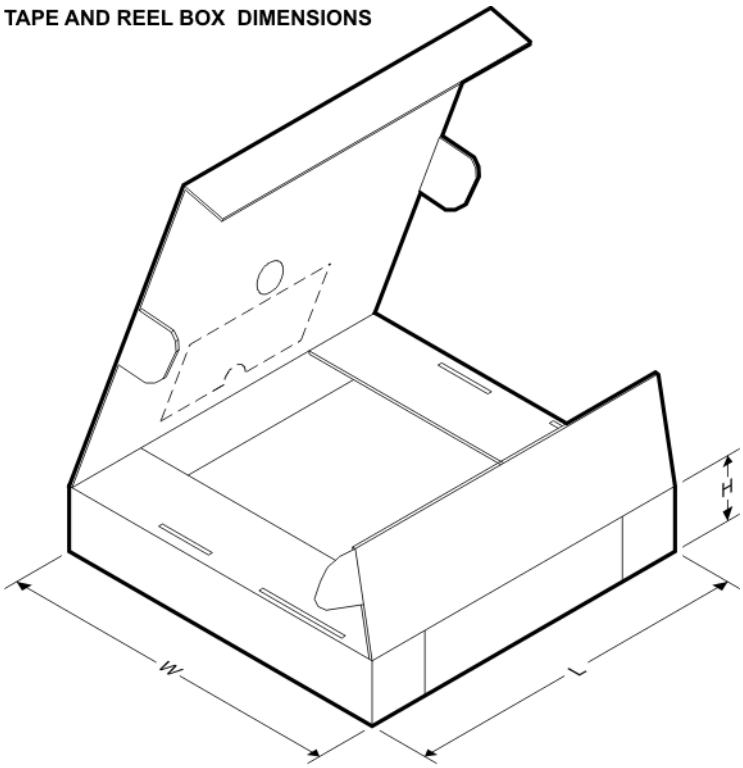
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VCA824IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
VCA824IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
VCA824IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

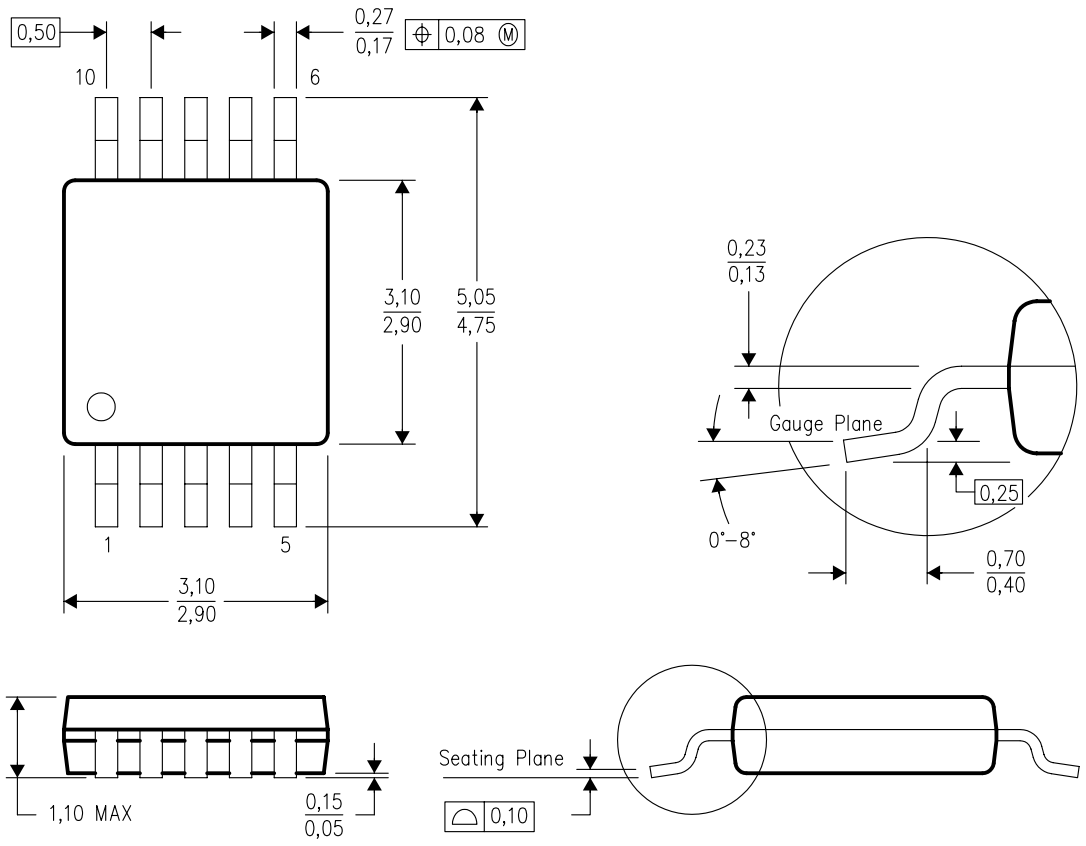
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VCA824IDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
VCA824IDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
VCA824IDR	SOIC	D	14	2500	367.0	367.0	38.0

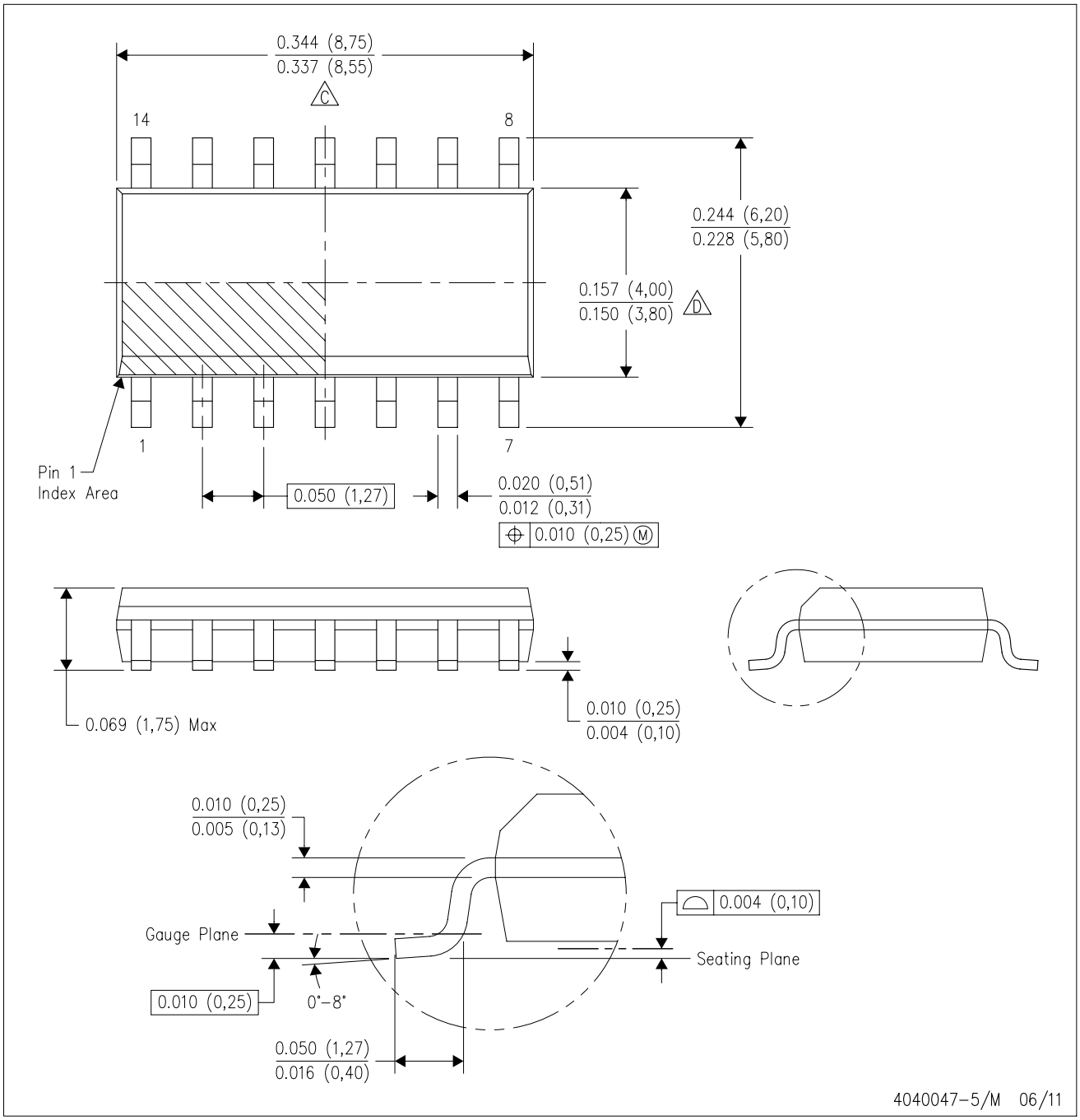
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



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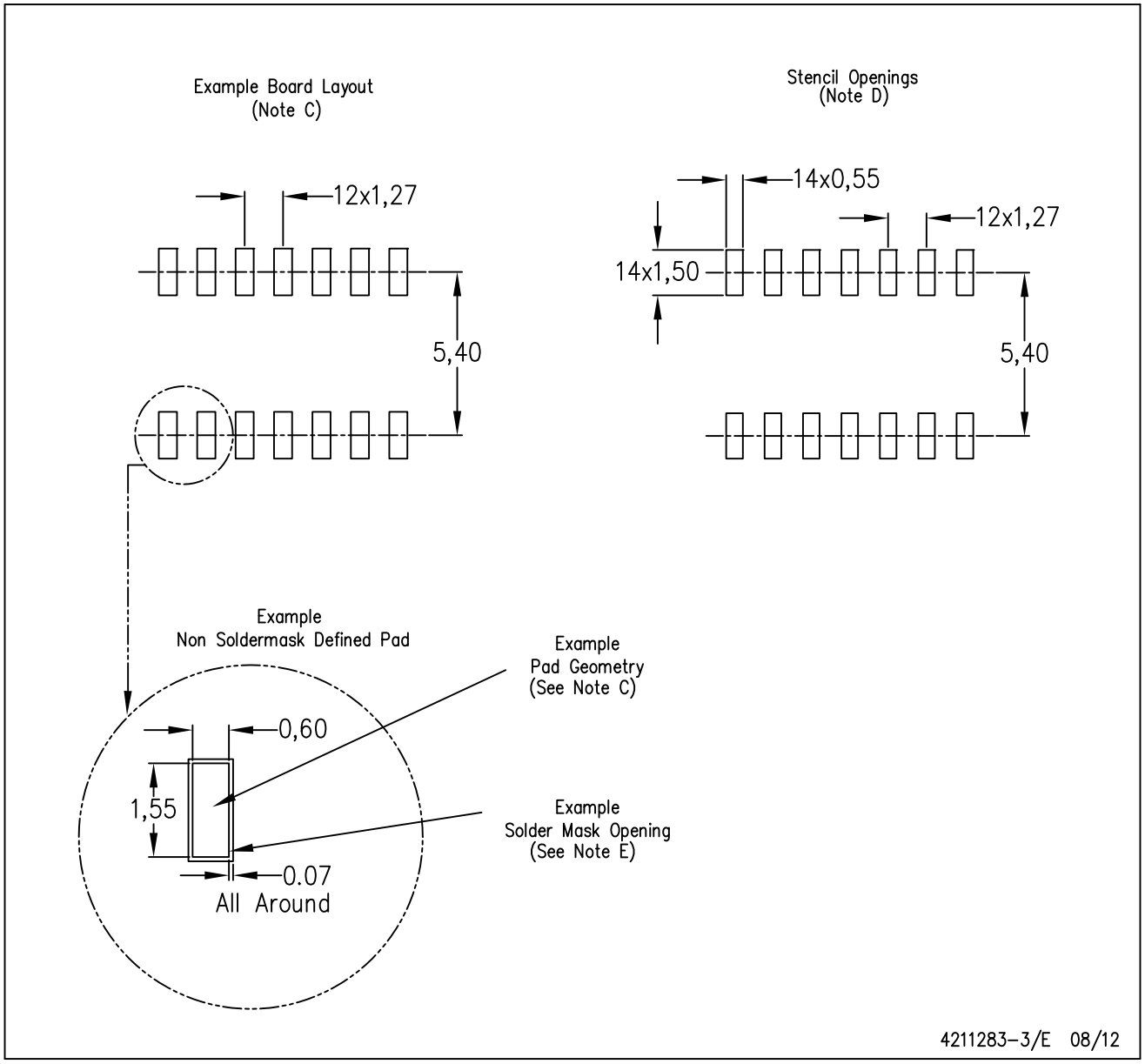
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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