3.3 VOLT CMOS SyncFIFO™ 64 x 36

IDT72V3611

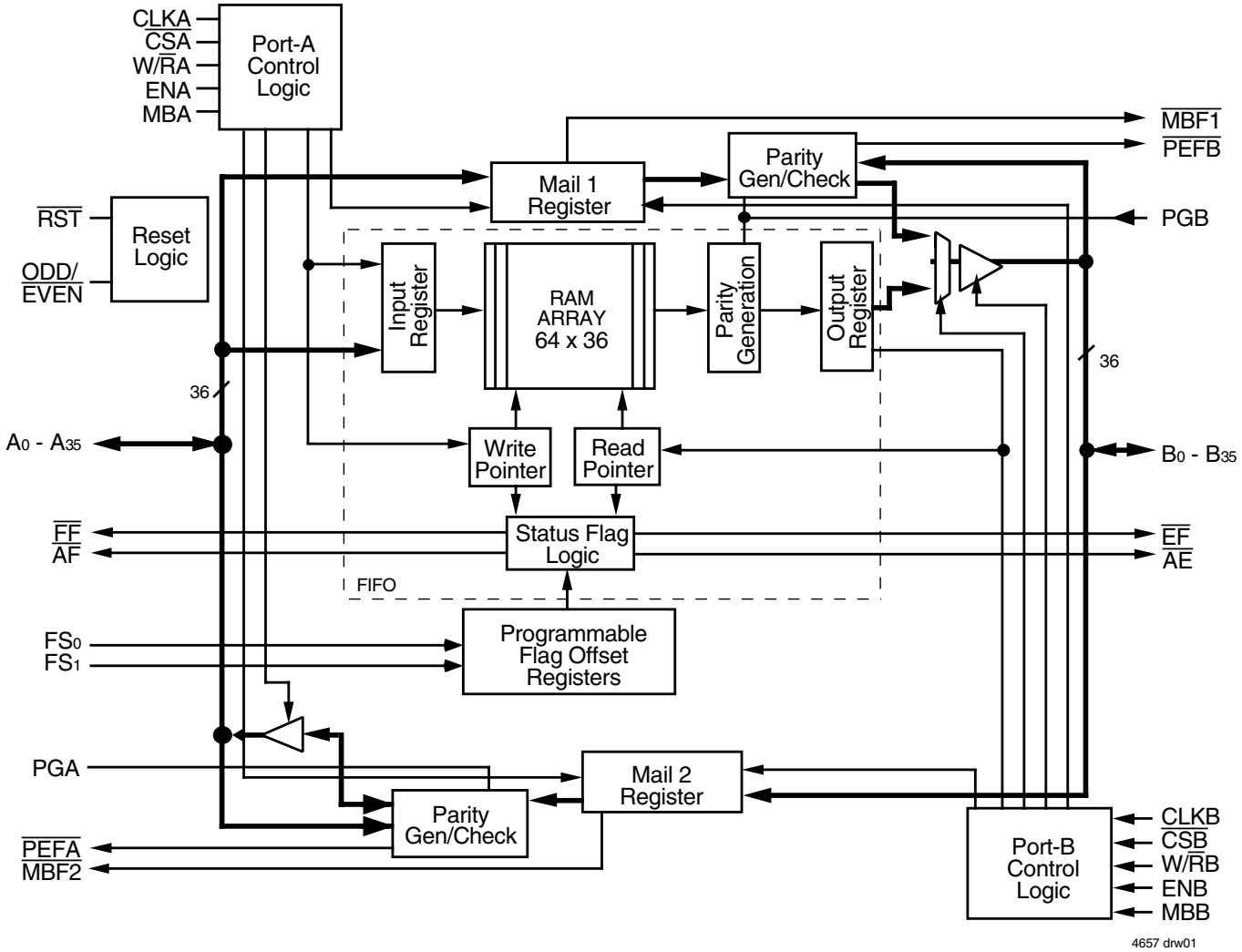
FEATURES:

- 64 x 36 storage capacity
- Supports clock frequencies up to 67MHz
- Fast access times of 10ns
- Free-running CLKA and CLKB may be asynchronous or coincident (permits simultaneous reading and writing of data on a single clock edge)
- Synchronous data buffering from Port A to Port B
- Mailbox bypass register in each direction
- Programmable Almost-Full ($\overline{AF}$) and Almost-Empty ($\overline{AE}$) flags
- Microprocessor Interface Control Logic
- Full Flag ($\overline{FF}$) and Almost-Full ($\overline{AF}$) flags synchronized by CLKA
- Empty Flag ($\overline{EF}$) and Almost-Empty ($\overline{AE}$) flags synchronized by CLKB
- Passive parity checking on each Port
- Parity Generation can be selected for each Port
- Available in space-saving 120-pin Thin Quad Flatpack (PF)
- Green parts available, see ordering information

DESCRIPTION:

The IDT72V3611 is designed to run off a 3.3V supply for exceptionally low power consumption. This device is a monolithic, high-speed, low-power, CMOS Synchronous (clocked) FIFO memory which supports clock frequencies up to 67MHz and has read access times as fast as 10ns. The 64 x 36 dual-port FIFO buffers data from Port A to Port B. The FIFO operates in IDT Standard mode and has flags to indicate empty and full conditions, and two programmable flags, Almost-Full ($\overline{AF}$) and Almost-Empty ($\overline{AE}$), to indicate when a selected number of words is stored in memory. Communication between each port can take place through two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if not desired. Parity generation can be selected

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION (CONTINUED)

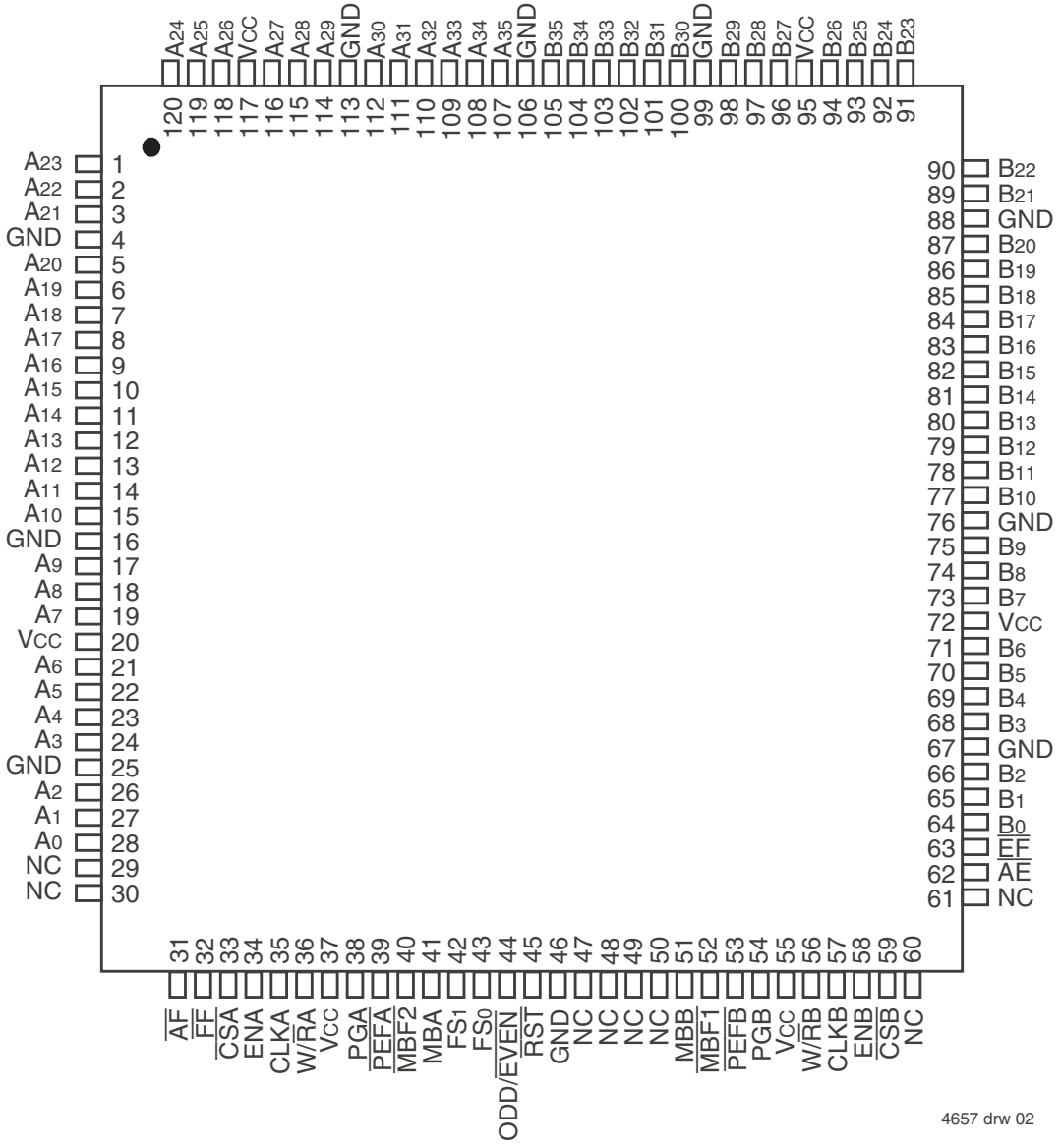
for data read from each port. Two or more devices may be used in parallel to create wider data paths.

The IDT72V3611 is a synchronous (clocked) FIFO, meaning each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The Full Flag ($\overline{FF}$) and Almost-Full ($\overline{AF}$) flag of the FIFO are two-stage synchronized to the port clock that writes data into its array (CLKA). The Empty Flag ($\overline{EF}$) and Almost-Empty ($\overline{AE}$) flag of the FIFO are two-stage synchronized to the port clock that reads data from its array.

The IDT72V3611 is characterized for operation from 0°C to 70°C. This device is fabricated using high speed, submicron CMOS technology.

PIN CONFIGURATION



4657 drw 02

NOTES:
1. Pin 1 identifier in corner.
2. NC = No internal connection

TQFP (PNG120, order code: PF)
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
A0-A35	Port-A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AE}$	Almost-Empty Flag	O	Programmable Almost-Empty flag synchronized to CLKB. It is LOW when the number of words in the FIFO is less than or equal to the value in the offset register, X.
$\overline{AF}$	Almost-Full Flag	O	Programmable Almost-Full flag synchronized to CLKA. It is LOW when the number of empty locations in the FIFO is less than or equal to the value in the Offset register, X.
B0-B35	Port-B Data.	I/O	36-bit bidirectional data port for side B.
CLKA	Port-A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through port-A and can be asynchronous or coincident to CLKB. $\overline{FF}$ and $\overline{AF}$ are synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port-B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through port-B and can be asynchronous or coincident to CLKA. $\overline{EF}$ and $\overline{AE}$ are synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port-A Chip Select	I	$\overline{CSA}$ must be LOW to enable a LOW-to-HIGH transition of CLKA to read or write data on port-A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port-B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on port-B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EF}$	Empty Flag	O	$\overline{EF}$ is synchronized to the LOW-to-HIGH transition of CLKB. When $\overline{EF}$ is LOW, the FIFO is empty, and reads from its memory are disabled. Data can be read from the FIFO to its output register when $\overline{EF}$ is HIGH. $\overline{EF}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKB after data is loaded into empty FIFO memory.
ENA	Port-A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on port-A.
ENB	Port-B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on port-B.
$\overline{FF}$	Full Flag	O	$\overline{FF}$ is synchronized to the LOW-to-HIGH transition of CLKA. When $\overline{FF}$ is LOW, the FIFO is full, and writes to its memory are disabled. $\overline{FF}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after reset.
FS1, FS0	Flag-Offset Selects	I	The LOW-to-HIGH transition of $\overline{RST}$ latches the values of FS0 and FS1, which loads one of four preset values into the Almost-Full and Almost-Empty Offset register (X).
MBA	Port-A Mailbox Select	I	A HIGH level on MBA chooses a mailbox register for a port-A read or write operation.
MBB	Port-B Mailbox Select	I	A HIGH level on MBB chooses a mailbox register for a port-B read or write operation. When the B0-B35 outputs are active, a HIGH level on MBB selects data from the mail1 register for output, and a LOW level selects the FIFO output register data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is set LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a port-B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH when the device is reset.
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a port-A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH when the device is reset.
ODD/ $\overline{EVEN}$	Odd/Even Parity Select	I	Odd parity is checked on each port when ODD/$\overline{EVEN}$ is HIGH, and even parity is checked when ODD/$\overline{EVEN}$ is LOW. ODD/$\overline{EVEN}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{PEFA}$	Port-A Parity Error Flag	O [Port A)	When any byte applied to terminals A0-A35 fails parity, $\overline{PEFA}$ is LOW. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the A0-A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is setup by having $\overline{CSA}$ LOW, ENA HIGH, W/$\overline{RA}$ LOW, MBA HIGH, and PGA HIGH, the $\overline{PEFA}$ flag is forced HIGH regardless of the state of A0-A35 inputs.

PIN DESCRIPTION (CONTINUED)

Symbol	Name	I/O	Description
$\overline{PEFB}$	Port-B Parity Error Flag	O (Port B)	When any byte applied to terminals B0-B35 fails parity, $\overline{PEFB}$ is LOW. Bytes are organized as B0-B8, B9-B17, B18-B26, B27-B35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the B0-B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is setup by having $\overline{CSB}$ LOW, ENB HIGH, W/$\overline{RB}$ LOW, MBB HIGH, and PGB HIGH, the $\overline{PEFB}$ flag is forced HIGH regardless of the state of the B0-B35 inputs
PGA	Port-A Parity Generation	I	Parity is generated for mail2 register reads from port A when PGA is HIGH. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35. The generated parity bits are output in the most significant bit of each byte.
PGB	Port-B Parity Generation	I	Parity is generated for data reads from port B when PGB is HIGH. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as B0-B8, B9-B17, B18-B26, and B27-B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{RST}$	Reset	I	To reset the device, four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST}$ is LOW. This sets the $\overline{AF}$, $\overline{MBF1}$, and $\overline{MBF2}$ flags HIGH and the $\overline{EF}$, $\overline{AE}$, and $\overline{FF}$ flags LOW. The LOW-to-HIGH transition of $\overline{RST}$ latches the status of the FS1 and FS0 inputs to select Almost-Full and Almost-Empty flag offset.
W/$\overline{RA}$	Port-A Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the high-impedance state when W/$\overline{RA}$ is HIGH.
W/$\overline{RB}$	Port-B Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the high-impedance state when W/$\overline{RB}$ is HIGH.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)(1)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	–0.5 to +4.6	V
V_I(2)	Input Voltage Range	–0.5 to V_{CC}+0.5	V
V_O(2)	Output Voltage Range	–0.5 to V_{CC}+0.5	V
I_{IK}	Input Clamp Current, (V_I < 0 or V_I > V_{CC})	±20	mA
I_{OK}	Output Clamp Current, (V_O = < 0 or V_O > V_{CC})	±50	mA
I_{OUT}	Continuous Output Current, (V_O = 0 to V_{CC})	±50	mA
I_{CC}	Continuous Current Through V_{CC} or GND	±500	mA
T_{STG}	Storage Temperature Range	–65 to 150	°C

NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	High-Level Input Voltage	2	—	V_{CC}+0.5	V
V_{IL}	Low-Level Input Voltage	—	—	0.8	V
I_{OH}	High-Level Output Current	—	—	–4	mA
I_{OL}	Low-Level Output Current	—	—	8	mA
T_A	Operating Free-Air Temperature	0	—	70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)

Symbol	Parameter	Test Conditions		IDT72V3611 Commercial t_{CLK} = 15 ns			Unit
				Min.	Typ.(1)	Max.	
V_{OH}	Output Logic "1" Voltage	V_{CC} = 3.0V,	I_{OH} = –4 mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage	V_{CC} = 3.0V,	I_{OL} = 8 mA	—	—	0.5	V
I_{LI}	Input Leakage Current (Any Input)	V_{CC} = 3.6V,	V_I = V_{CC} or 0	—	—	±5	µA
I_{LO}	Output Leakage Current	V_{CC} = 3.6V,	V_O = V_{CC} or 0	—	—	±5	µA
I_{CC}(2)	Standby Current	V_{CC} = 3.6V,	V_I = V_{CC} - 0.2V or 0	—	—	500	µA
C_{IN}	Input Capacitance	V_I = 0,	f = 1 MHz	—	4	—	pF
C_{OUT}	Output Capacitance	V_O = 0,	f = 1 MHZ	—	8	—	pF

NOTES:
1. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
2. For additional I_{CC} information, see Figure 1, *Typical Characteristics: Supply Current (I_{CC}) vs. Clock Frequency (fs)*.

DETERMINING ACTIVE CURRENT CONSUMPTION AND POWER DISSIPATION

The $I_{CC(f)}$ data for the graph was taken while simultaneously reading and writing the FIFO on the IDT72V3611 with CLKA and CLKB operating at frequency f_S. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitance load per data-output channel is known, the power dissipation can be calculated with the equation below.

CALCULATING POWER DISSIPATION

With $I_{CC(f)}$ taken from Figure 1, the maximum power dissipation (PT) of the IDT72V3611 may be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \sum_{N}(C_L \times (V_{OH} - V_{OL})^2 \times f_O)$$

where:

N	=	number of outputs = 36
C_L	=	output capacitance load
f_O	=	switching frequency of an output
V_{OH}	=	output high-level voltage
V_{OL}	=	output low-level voltage

When no read or writes are occurring on this device, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_S is calculated by:

$$P_T = V_{CC} \times f_S \times 0.025 \text{ mA/MHz}$$

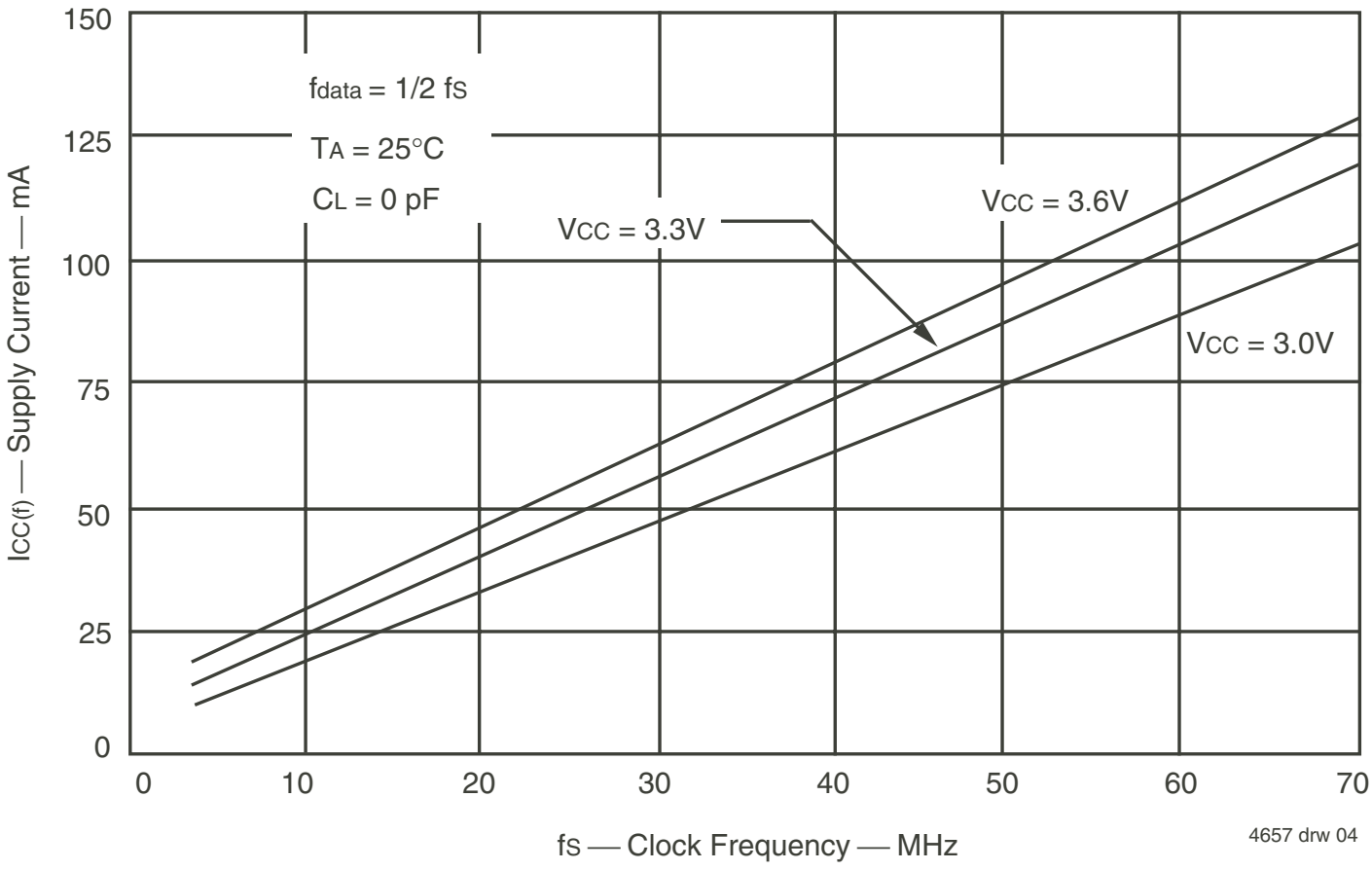


Figure 1. Typical Characteristics: Supply Current (I_{CC}) vs. Clock Frequency (f_S)

TIMING REQUIREMENTS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURES

Symbol	Parameter	IDT72V3611L15		Unit
		Min.	Max.	
f_S	Clock Frequency, CLKA or CLKB	–	66.7	Mhz
t_{CLK}	Clock Cycle Time, CLKA or CLKB	15	–	Mhz
t_{CLKH}	Pulse Duration, CLKA or CLKB HIGH	6	–	ns
t_{CLKL}	Pulse Duration, CLKA or CLKB LOW	6	–	ns
t_{DS}	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	4	–	ns
t_{ENS1}	$\overline{CSA}$, W/$\overline{RA}$, before CLKA↑; $\overline{CSB}$, W/$\overline{RB}$ before CLKB↑	6	–	ns
t_{ENS2}	ENA before CLKA↑; ENB before CLKB↑	4	–	ns
t_{ENS3}	MBA before CLKA↑; $\overline{ENB}$ before CLKB↑	4	–	ns
t_{PGS}	Setup Time, ODD/$\overline{EVEN}$ and PGB before CLKB↑[1]	4	–	ns
t_{RSTS}	Setup Time, $\overline{RST}$ LOW before CLKA↑ or CLKB↑[2]	5	–	ns
t_{FSS}	Setup Time, FS0 and FS1 before $\overline{RST}$ HIGH	5	–	ns
t_{DH}	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	1	–	ns
t_{ENH1}	$\overline{CSA}$, W/$\overline{RA}$ after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$ after CLKB↑	1	–	ns
t_{ENH2}	ENA after CLKA↑; ENB after CLKB↑	1		ns
t_{ENH3}	MBA after CLKA↑; MBB after CLKB↑	1		ns
t_{PGH}	Hold Time, ODD/$\overline{EVEN}$ and PGB after CLKB↑[1]	0	–	ns
t_{RSTH}	Hold Time, $\overline{RST}$ LOW after CLKA↑ or CLKB↑[2]	6	–	ns
t_{FSH}	Hold Time, FS0 and FS1 after $\overline{RST}$ HIGH	4	–	ns
t_{SKEW1}[3]	Skew Time, between CLKA↑ and CLKB↑ for $\overline{EF}$, $\overline{FF}$	8	–	ns
t_{SKEW2}[3,4]	Skew Time, between CLKA↑ and CLKB↑ for $\overline{AE}$, $\overline{AF}$	14	–	ns

NOTES:
1. Only applies for a rising edge of CLKB that does a FIFO read.
2. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
3. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.
4. Design simulated, not tested.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, C_L = 30 pF

Symbol	Parameter	IDT72V3611L15 Min.	IDT72V3611L15 Max.	Unit
f_S	Clock Frequency, CLKA or CLKB	–	66.7	MHz
t_A	Access Time, CLKB↑ to B0-B35	2	10	ns
t_{WFF}	Propagation Delay Time, CLKA↑ to $\overline{FF}$	2	10	ns
t_{REF}	Propagation Delay Time, CLKB↑ to $\overline{EF}$	2	10	ns
t_{PAE}	Propagation Delay Time, CLKB↑ to $\overline{AE}$	2	10	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AF}$	2	10	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	1	9	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to B0-B35[1] and CLKB↑ to A0-A35[2]	2	10	ns
t_{MDV}	Propagation Delay Time, MBB to B0-B35 Valid	1	10	ns
t_{PDPE}	Propagation Delay Time, A0-A35 Valid to $\overline{PEFA}$ Valid; B0-B35 Valid to $\overline{PEFB}$ Valid	2	10	ns
t_{POPE}	Propagation Delay Time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	2	10	ns
t_{POPB}[3]	Propagation Delay Time, ODD/$\overline{EVEN}$ to Parity Bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	10	ns
t_{PEPE}	Propagation Delay Time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to $\overline{PEFA}$; $\overline{CSB}$, ENB, W/$\overline{RB}$, MBB, or PGB to $\overline{PEFB}$	1	10	ns
t_{PEPB}[3]	Propagation Delay Time, $\overline{CSA}$, ENA W/$\overline{RA}$, MBA, or PGA to Parity Bits (A8, A17, A26, A35); $\overline{CSB}$, ENB, W/$\overline{RB}$, MBB, or PGB to Parity Bits (B8, B17, B26, B35)	2	10	ns
t_{RSF}	Propagation Delay Time, $\overline{RST}$ to $\overline{AE}$ LOW and ($\overline{AF}$, $\overline{MBF1}$, $\overline{MBF2}$) HIGH	1	15	ns
t_{EN}	Enable Time, $\overline{CSA}$ and W/$\overline{RA}$ LOW to A0-A35 Active and $\overline{CSB}$ LOW and $\overline{W}$/RB HIGH to B0-B35 Active	2	10	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{RA}$ HIGH to A0-A35 at high impedance and $\overline{CSB}$ HIGH or $\overline{W}$/RB LOW to B0-B35 at high impedance	1	9	ns

NOTES:
1. Writing data to the mail1 register when the B0-B35 outputs are active and MBB is HIGH.
2. Writing data to the mail2 register when the A0-A35 outputs are active and MBA is HIGH.
3. Only applies when reading data from a mail register.

SIGNAL DESCRIPTION

RESET ($\overline{RST}$)

The IDT72V3611 is reset by taking the Reset ($\overline{RST}$) input LOW for at least four port-A clock (CLKA) and four port B clock (CLKB) LOW-to-HIGH transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of the FIFO and forces the Full Flag ($\overline{FF}$) LOW, the Empty Flag ($\overline{EF}$) LOW, the Almost-Empty flag ($\overline{AE}$) LOW, and the Almost-Full flag ($\overline{AF}$) HIGH. A reset also forces the Mailbox Flags ($\overline{MBF1}$, $\overline{MBF2}$) HIGH. After a reset, $\overline{FF}$ is set HIGH after two LOW-to-HIGH transitions of CLKA. The device must be reset after power up before data is written to its memory.

A LOW-to-HIGH transition on the $\overline{RST}$ input loads the Almost-Full and Almost-Empty Offset register (X) with the value selected by the Flag Select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1. For the relevant Reset timing and preset value loading timing diagram, see Figure 2. The relevant Write timing diagram for Port A can be found in Figure 3.

TABLE 1 – FLAG PROGRAMMING

Almost-Full and Almost-Empty Flag Offset Register (X)	FS1	FS0	$\overline{RST}$
16	H	H	↑
12	H	L	↑
8	L	H	↑
4	L	L	↑

FIFO WRITE/READ OPERATION

The state of the port-A data (A0-A35) outputs is controlled by the port-A Chip Select ($\overline{CSA}$) and the port-A Write/Read select (W/$\overline{RA}$). The A0-A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW. Data is loaded into the FIFO from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH, MBA is LOW, and $\overline{FF}$ is HIGH (see Table 2).

The port-B control signals are identical to those of port A. The state of the port-B data (B0-B35) outputs is controlled by the port-B Chip Select ($\overline{CSB}$) and the port-B Write/Read select (W/$\overline{RB}$). The B0-B35 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is HIGH. The B0-B35 outputs are active when both $\overline{CSB}$ and W/$\overline{RB}$ are LOW. Data is read from the FIFO to the B0-B35 outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, W/$\overline{RB}$ is LOW, ENB is HIGH, MBB is LOW, and $\overline{EF}$ is HIGH (see Table 3). The relevant Read timing diagram for Port B can be found in Figure 4.

The setup and hold-time constraints to the port clocks for the port Chip Selects ($\overline{CSA}$, $\overline{CSB}$) and Write/Read selects (W/$\overline{RA}$, W/$\overline{RB}$) are only for enabling write and read operations and are not related to HIGH-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port's Chip Select and Write/Read select can change states during the setup and hold-time window of the cycle.

TABLE 2 – PORT-A ENABLE FUNCTION TABLE

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	Data A (A0-A35) I/O	Port Functions
H	X	X	X	X	Input	None
L	H	L	X	X	Input	None
L	H	H	L	↑	Input	FIFO Write
L	H	H	H	↑	Input	Mail1 Write
L	L	L	L	X	Output	None
L	L	H	L	↑	Output	None
L	L	L	H	X	Output	None
L	L	H	H	↑	Output	Mail2 Read (set $\overline{MBF2}$ HIGH)

TABLE 3 – PORT-B ENABLE FUNCTION TABLE

$\overline{CSB}$	W/$\overline{RB}$	ENB	MBB	CLKB	Data B (B0-B35) I/O	Port Functions
H	X	X	X	X	Input	None
L	H	L	X	X	Input	None
L	H	H	L	↑	Input	None
L	H	H	H	↑	Input	Mail2 Write
L	L	L	L	X	Output	None
L	L	H	L	↑	Output	FIFO Read
L	L	L	H	X	Output	None
L	L	H	H	↑	Output	Mail1 Read (set $\overline{MBF1}$ HIGH)

SYNCHRONIZED FIFO FLAGS

Each FIFO flag is synchronized to its port clock through two flip-flop stages. This is done to improve the flags' reliability by reducing the probability of metastable events on their outputs when CLKA and CLKB operate asynchronously to one another. $\overline{FF}$ and $\overline{AF}$ are synchronized to CLKA. $\overline{EF}$ and $\overline{AE}$ are synchronized to CLKB. Table 4 shows the relationship of the flags to the level of FIFO fill.

EMPTY FLAG ($\overline{EF}$)

The FIFO Empty Flag is synchronized to the port clock that reads data from its array (CLKB). When the $\overline{EF}$ is HIGH, new data can be read to the FIFO output register. When the $\overline{EF}$ is LOW, the FIFO is empty and attempted FIFO reads are ignored.

The FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an $\overline{EF}$ monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is empty, empty+1, or empty+2. A word written to the FIFO can be read to the FIFO output register in a minimum of three port-B clock (CLKB) cycles. Therefore, an $\overline{EF}$ is LOW if a word in memory is the next data to be sent to the FIFO output register and two CLKB cycles have not elapsed since the time the word was written. The $\overline{EF}$ of the FIFO is set HIGH by the second LOW-to-HIGH transition of CLKB, and the new data word can be read to the FIFO output register in the following cycle.

A LOW-to-HIGH transition on CLKB begins the first synchronized cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 5).

FULL FLAG ($\overline{FF}$)

The FIFO Full Flag is synchronized to the port clock that writes data to its array (CLKA). When the $\overline{FF}$ is HIGH, a FIFO memory location is free to receive new data. No memory locations are free when the $\overline{FF}$ is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to the FIFO, its write pointer is incremented. The state machine that controls the $\overline{FF}$ monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is full, full-1, or full-2. From the time a word is read from the FIFO, its previous memory location is ready to be written in a minimum of three port-A clock cycles. Therefore, a $\overline{FF}$ is LOW if less than two CLKA cycles have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on CLKA after the read sets the $\overline{FF}$ HIGH and data can be written in the following clock cycle.

A LOW-to-HIGH transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 6).

TABLE 4 – FIFO FLAG OPERATION

Number of Words in the FIFO	Synchronized to CLKB		Synchronized to CLKA	
	$\overline{EF}$	$\overline{AE}$	$\overline{AF}$	$\overline{FF}$
0	L	L	H	H
1 to X	H	L	H	H
(X+1) to [64-(X+1)]	H	H	H	H
(64-X) to 63	H	H	L	H
64	H	H	L	L

NOTE:
1. X is the value in the Almost-Empty flag and Almost-Full flag register.

ALMOST-EMPTY FLAG ($\overline{AE}$)

The FIFO Almost-Empty flag is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls the $\overline{AE}$ flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is almost-empty, almost-empty+1, or almost-empty+2. The almost-empty state is defined by the value of the Almost-Full and Almost-Empty Offset register (X). This register is loaded with one of four preset values during a device reset (see the Reset section). The $\overline{AE}$ flag is LOW when the FIFO contains X or less words in memory and is HIGH when the FIFO contains (X+1) or more words.

Two LOW-to-HIGH transitions on the port-B clock (CLKB) are required after a FIFO write for the $\overline{AE}$ flag to reflect the new level of fill. Therefore, the $\overline{AE}$ flag of a FIFO containing (X+1) or more words remains LOW if two CLKB cycles have not elapsed since the write that filled the memory to the (X+1) level. The $\overline{AE}$ flag is set HIGH by the second CLKB LOW-to-HIGH transition after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition on CLKB begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 7).

ALMOST-FULL FLAG ($\overline{AF}$)

The FIFO Almost-Full flag is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an $\overline{AF}$ flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is almost-full, almost- full-1, or almost-full-2. The almost-full state is defined by the value of the Almost-Full and Almost-Empty Offset register (X). This register is loaded with one of four preset values during a device reset (see the Reset section). The $\overline{AF}$ flag is LOW when the FIFO contains (64-X) or more words in memory and is HIGH when the FIFO contains [64-(X+1)] or less words.

Two LOW-to-HIGH transitions on the port-A clock (CLKA) are required after a FIFO read for the $\overline{AF}$ flag to reflect the new level of fill. Therefore, the $\overline{AF}$ flag of a FIFO containing [64-(X+1)] or less words remains LOW if two CLKA cycles have not elapsed since the read that reduced the number of words in memory to [64-(X+1)]. The $\overline{AF}$ flag is set HIGH by the second CLKA LOW-to-HIGH transition after the FIFO read that reduces the number of words in memory to [64-(X+1)]. A LOW-to-HIGH transition on CLKA begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of words in memory to [64-(X+1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 8).

MAILBOX REGISTERS

Two 36-bit bypass registers are on the IDT72V3611 to pass command and control information between port A and port B. The Mailbox select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A LOW-to-HIGH transition on CLKA writes A0-A35 data to the mail1 register when port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH. A LOW-to-HIGH transition on CLKB writes B0-B35 data to the mail2 register when port-B write is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB with MBB HIGH. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while its mail flag is LOW.

When the port-B data (B0-B35) outputs are active, the data on the bus comes from the FIFO output register when the port-B Mailbox select (MBB) input

is LOW and from the mail1 register when MBB is HIGH. Mail2 data is always present on the port-A data (A0-A35) outputs when they are active. The Mail1 Register Flag ($\overline{MBF1}$) is set HIGH by a LOW-to-HIGH transition on CLKB when a port-B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB with MBB HIGH. The Mail2 Register Flag ($\overline{MBF2}$) is set HIGH by a LOW-to-HIGH transition on CLKA when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH. The data in a mail register remains intact after it is read and changes only when new data is written to the register. For relevant mail register and mail register flag timing diagrams, see Figure 9 and Figure 10.

PARITY CHECKING

The port-A (A0-A35) inputs and port-B (B0-B35) inputs each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the input bus is reported by a LOW level on the port Parity Error Flag ($\overline{PEFA}$, $\overline{PEFB}$). Odd or even parity checking can be selected, and the Parity Error Flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the Odd/Even parity (ODD/$\overline{EVEN}$) select input. A parity error on one or more bytes of a port is reported by a LOW level on the corresponding port Parity Error Flag ($\overline{PEFA}$, $\overline{PEFB}$) output. Port-A bytes are arranged as A0-A8, A9-A17, A18-A26, and A27-A35, and port-B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35. When Odd/Even parity is selected, a port Parity Error Flag ($\overline{PEFA}$, $\overline{PEFB}$) is LOW if any byte on the port has an odd/even number of LOW levels applied to its bits.

The four parity trees used to check the A0-A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA=HIGH). When port-A read from the mail2 register with parity generation is selected with $\overline{CSA}$ LOW, ENA HIGH, W/$\overline{RA}$ LOW, MBA HIGH, and PGA HIGH, the port-A Parity Error Flag ($\overline{PEFA}$) is held HIGH regardless of the levels applied to the A0-A35 inputs. Likewise, the parity trees used to check the B0-B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB=HIGH). When a port-B read from the mail1 register with parity generation is selected with $\overline{CSB}$ LOW, ENB HIGH, W/$\overline{RB}$ LOW, MBB HIGH, and PGB HIGH, the port-B Parity Error Flag ($\overline{PEFB}$) is held HIGH regardless of the levels applied to the B0-B35 inputs.

PARITY GENERATION

A HIGH level on the port-A Parity Generate select (PGA) or port-B Parity Generate select (PGB) enables the IDT72V3611 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all thirty-six inputs regardless of the state of the Parity Generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{EVEN}$ select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from the FIFO RAM and before the data is written to the output register. Therefore, the port-B Parity Generate select (PGB) and ODD/$\overline{EVEN}$ have setup and hold time constraints to the port-B clock (CLKB) for a rising edge of CLKB used to read a new word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0-B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port-A bus (A0-A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port Write/Read select (W/$\overline{RA}$, W/$\overline{RB}$) input is LOW, the port Mail select (MBA, MBB) input is HIGH, Chip Select ($\overline{CSA}$, $\overline{CSB}$) is LOW, Enable (ENA, ENB) is HIGH, and the port Parity Generate select (PGA, PGB) is HIGH. Generating parity for mail register data does not change the contents of the register (see Figure 13 and Figure 14).

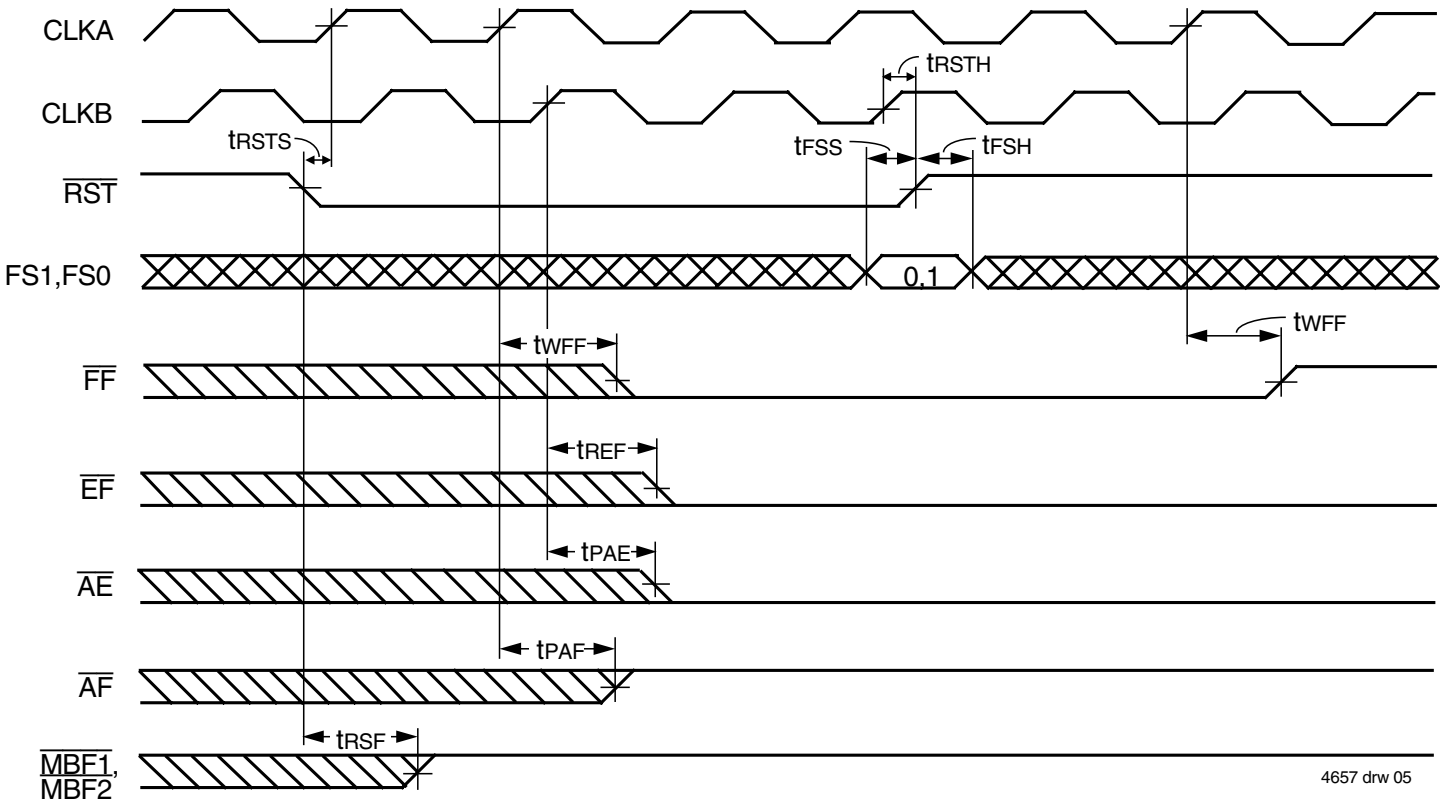


Figure 2. Device Reset and Loading the X Register with the Value of Eight

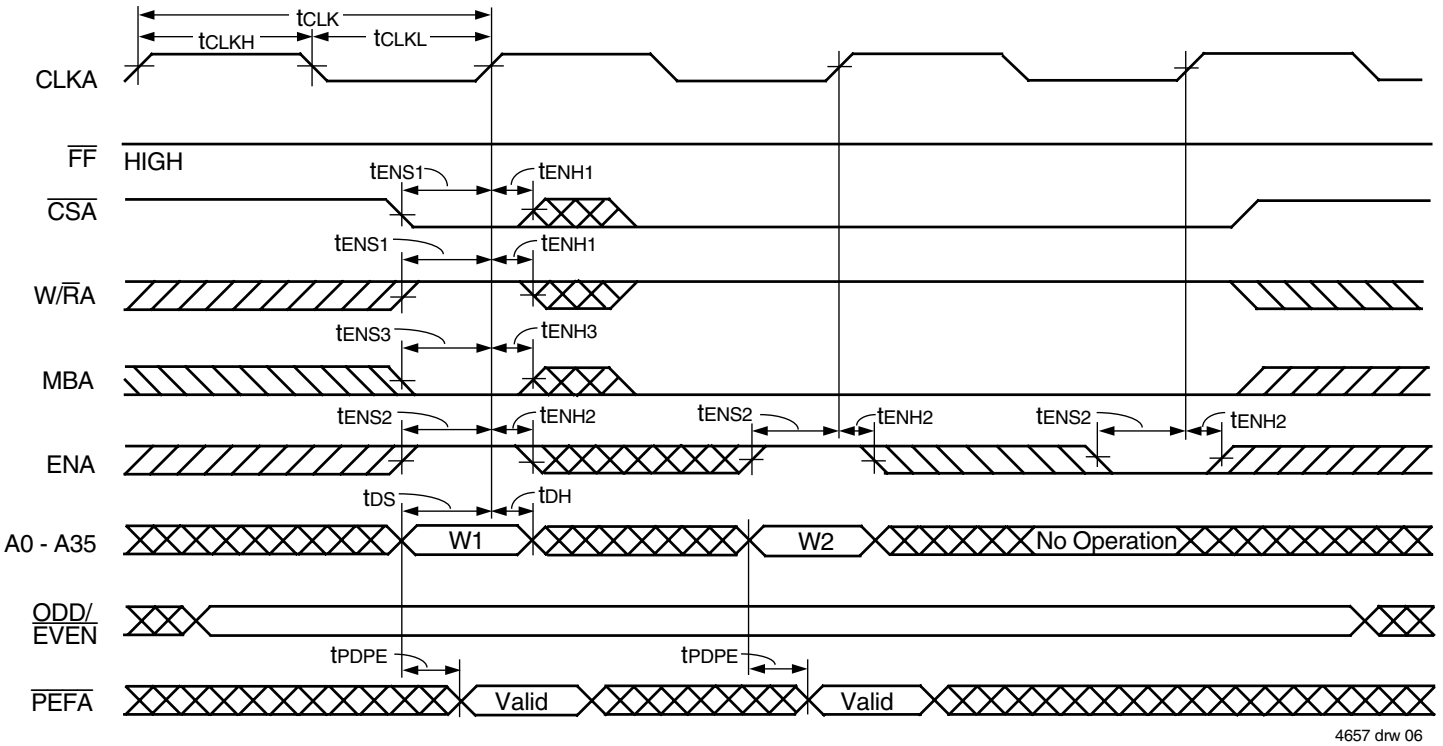


Figure 3. FIFO Write Cycle Timing

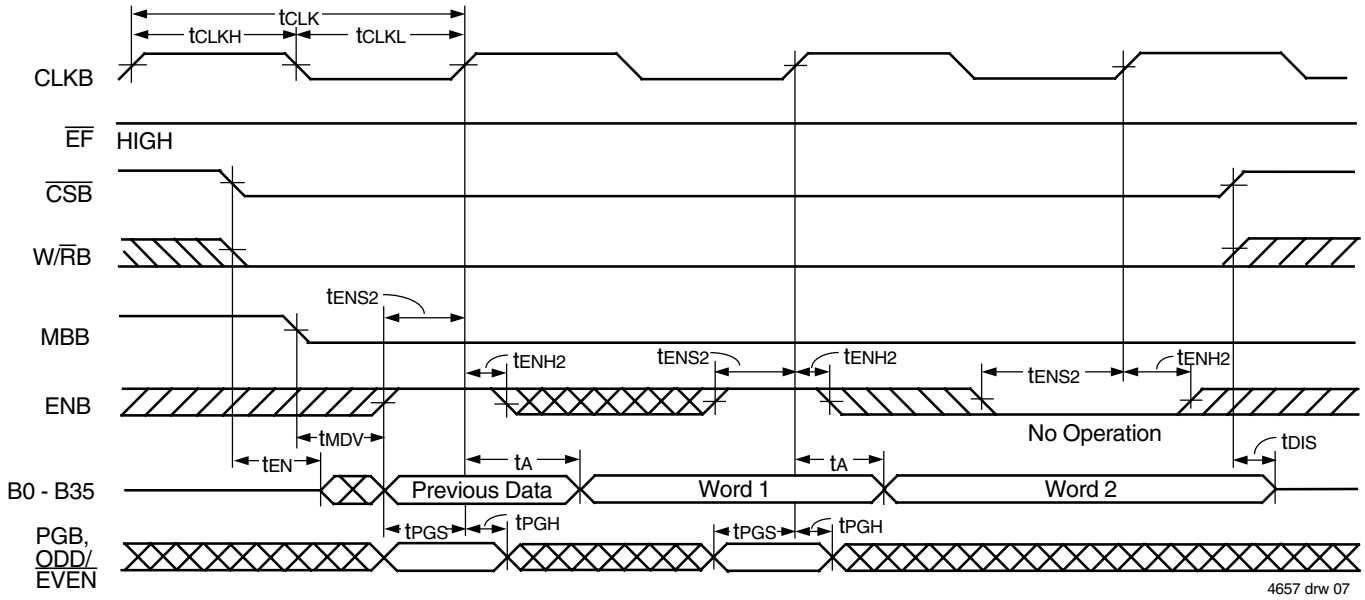
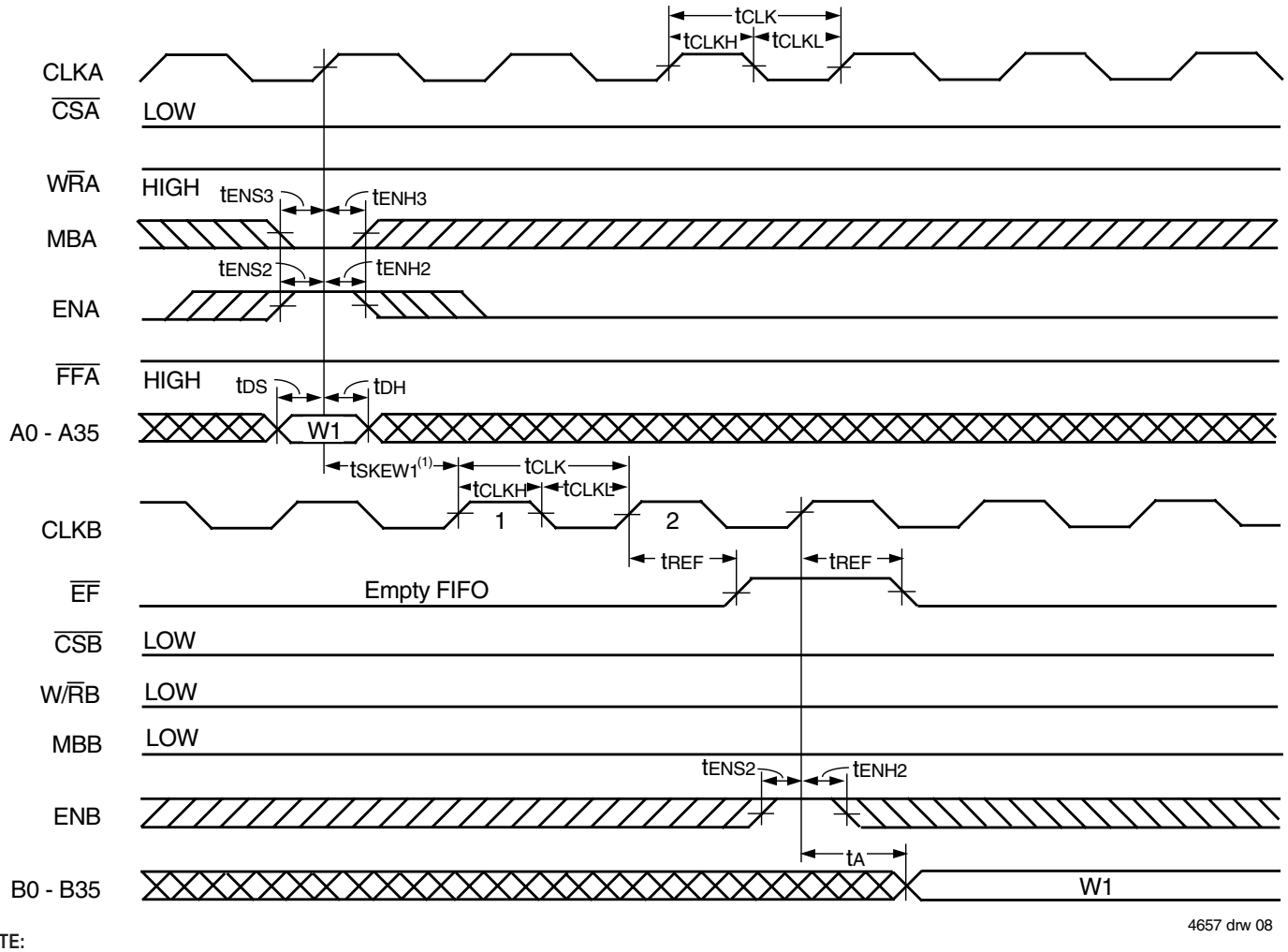


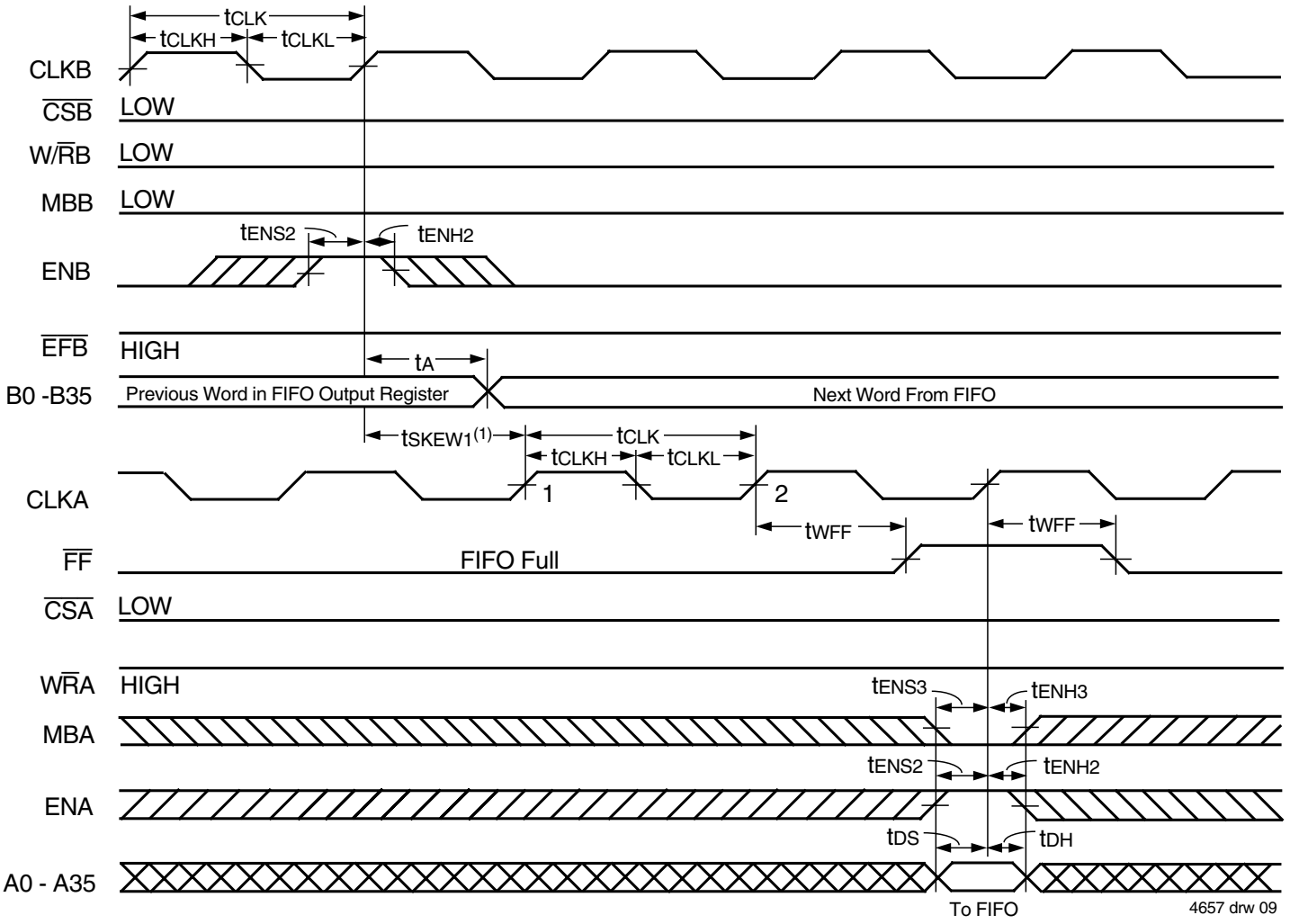
Figure 4. FIFO Read Cycle Timing



NOTE:

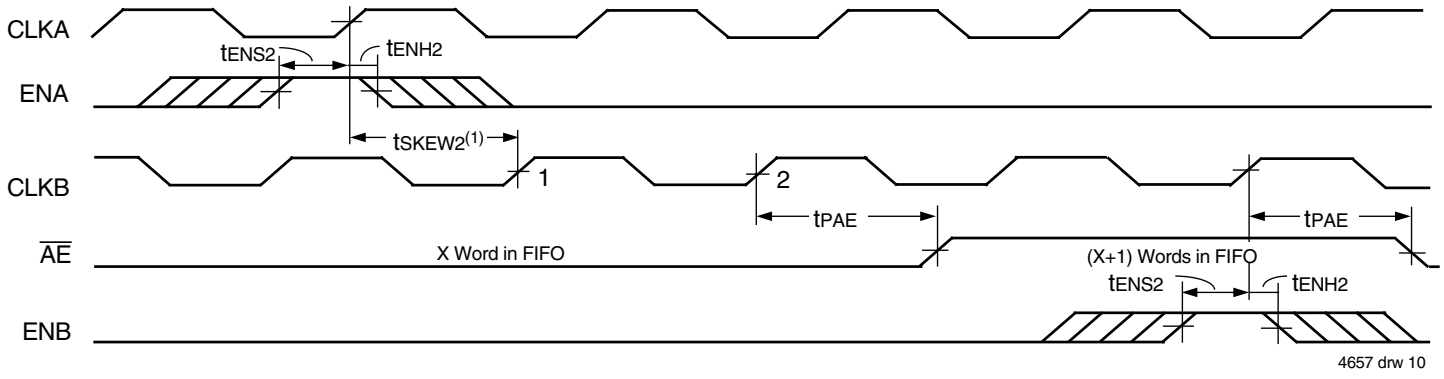
1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EF}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of $\overline{EF}$ HIGH may occur one CLKB cycle later than shown.

Figure 5. $\overline{EF}$ Flag Timing and First Data Read when the FIFO is Empty



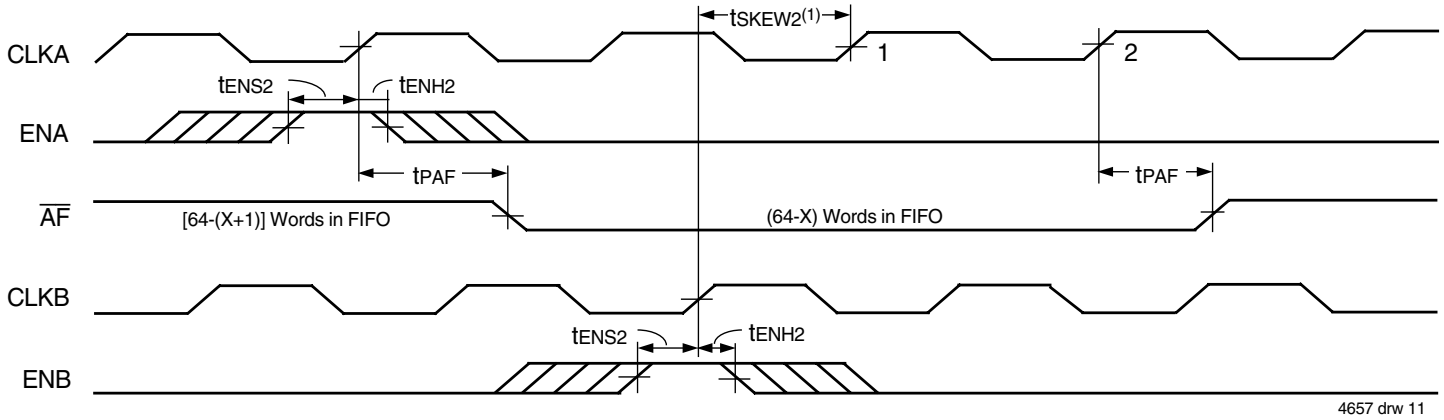
NOTE:
1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FF}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of $\overline{FF}$ HIGH may occur one CLKA cycle later than shown.

Figure 6. $\overline{FF}$ Flag Timing and First Available Write when the FIFO is Full



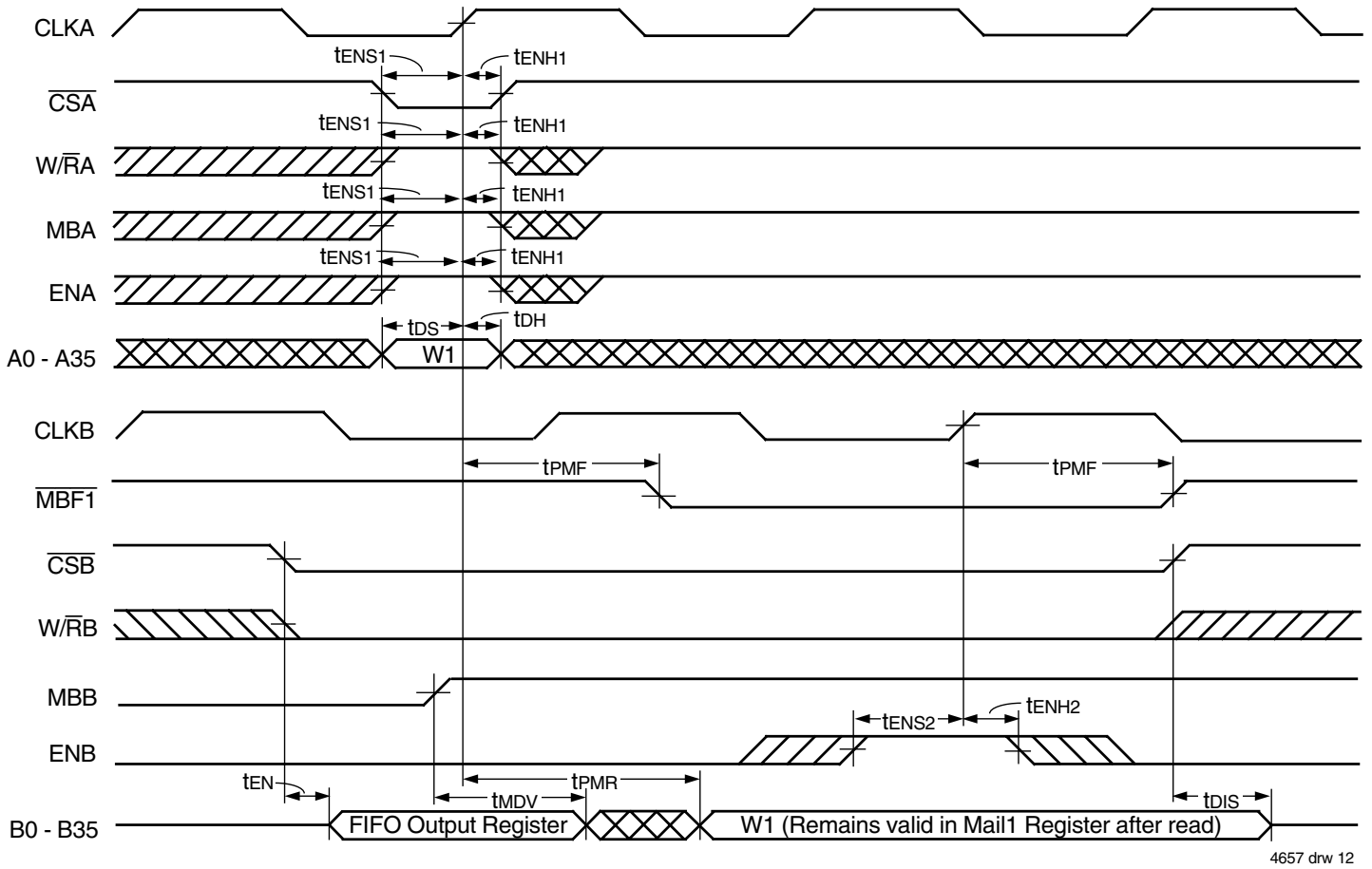
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AE}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

Figure 7. Timing for $\overline{AE}$ when the FIFO is Almost-Empty



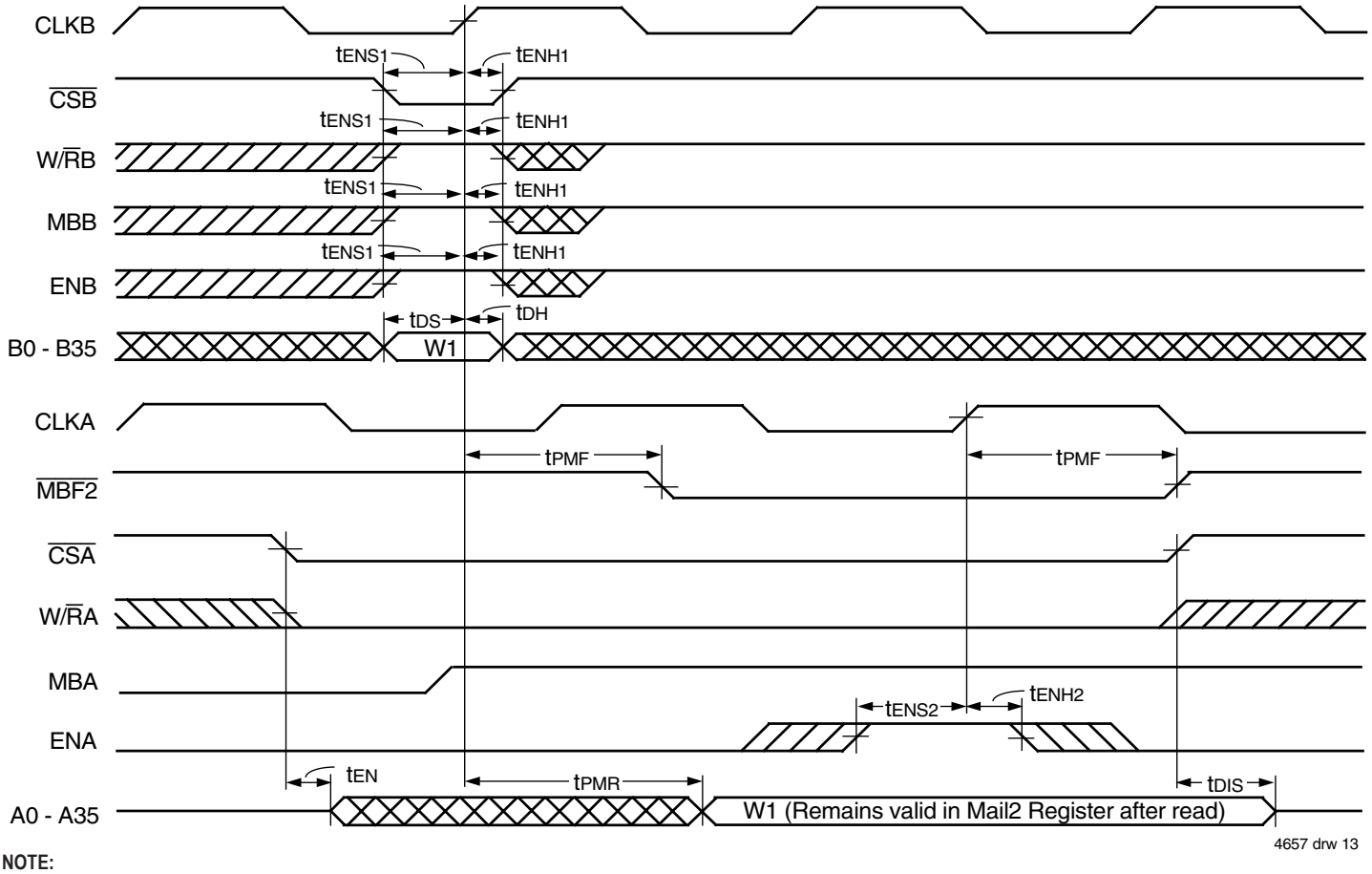
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AF}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

Figure 8. Timing for $\overline{AF}$ when the FIFO is Almost-Full



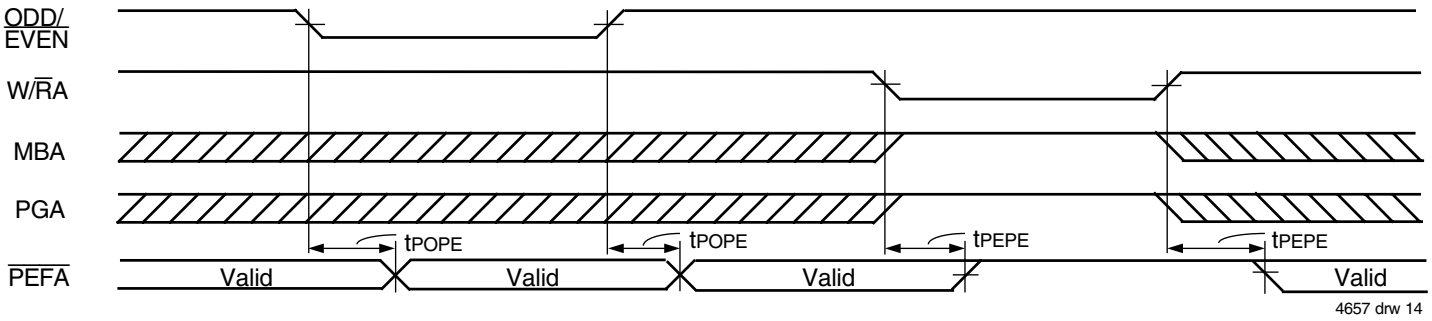
NOTE:
1. Port-B parity generation off (PGB = L)

Figure 9. Timing for Mail1 Register and $\overline{MBF1}$ Flag



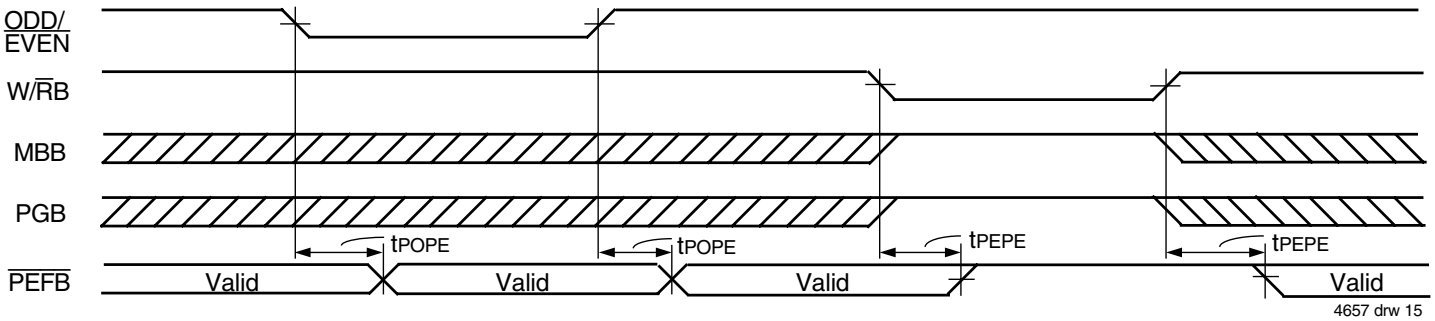
NOTE:
1. Port-A parity generation off (PGA = L)

Figure 10. Timing for Mail2 Register and $\overline{MBF2}$ Flag



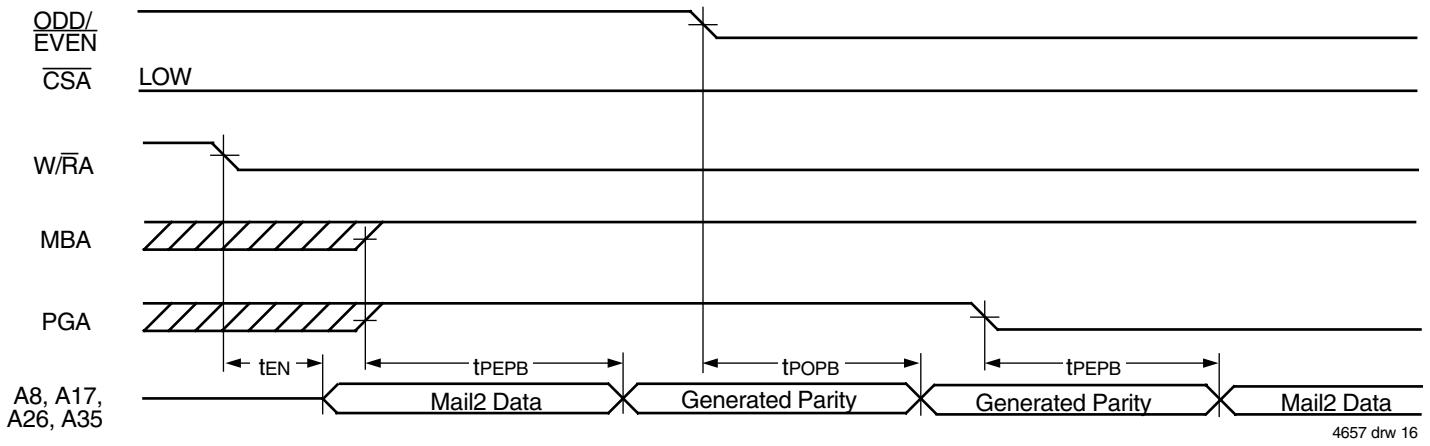
NOTE:
1. $\overline{CSA}$ = L and ENA = H.

Figure 11. ODD/$\overline{EVEN}$, W/RA, MBA, and PGA to $\overline{PEFA}$ Timing



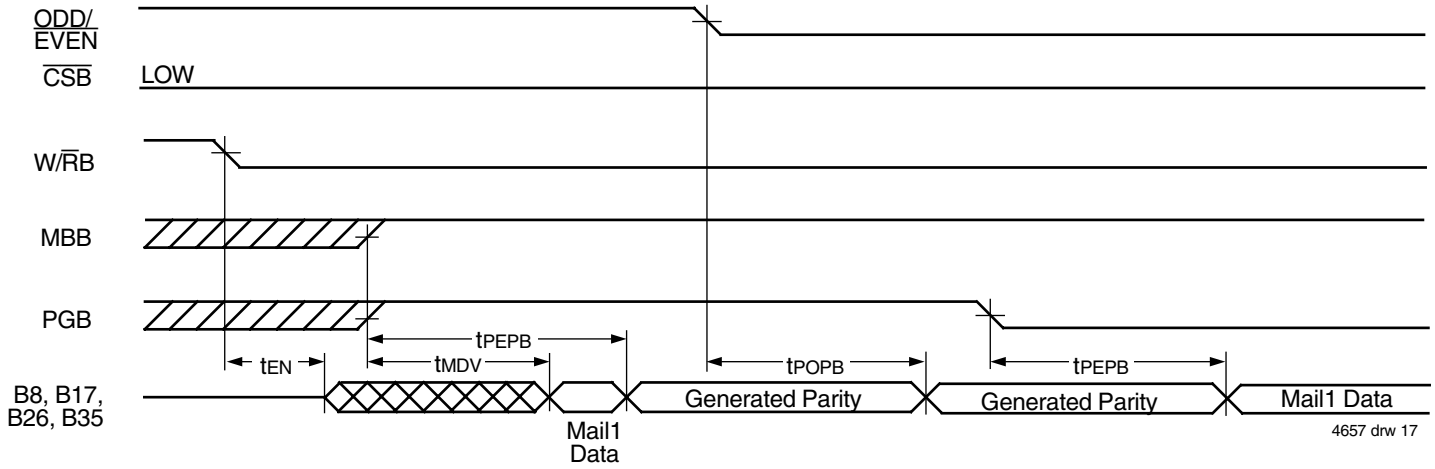
NOTE:
1. $\overline{CSB}$ = L and ENB = H.

Figure 12. ODD/$\overline{EVEN}$, W/RB, MBB, and PGB to $\overline{PEFB}$ Timing



NOTE:
1. ENA = H.

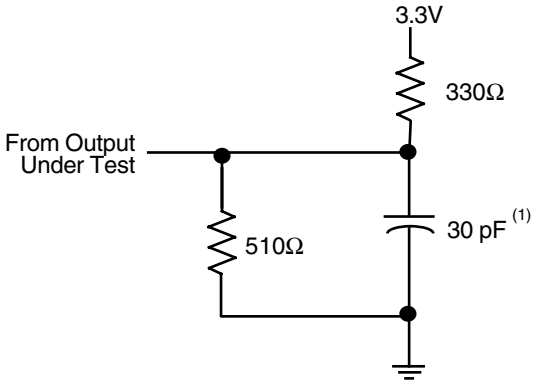
Figure 13. Parity Generation Timing when reading from the Mail2 Register



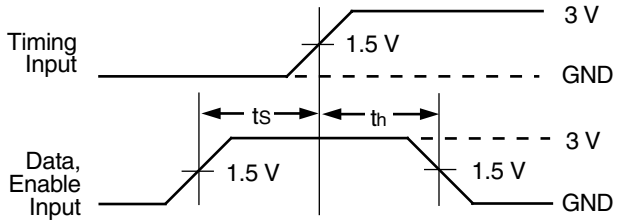
NOTE:
1. ENB = H.

Figure 14. Parity Generation Timing when reading from the Mail1 Register

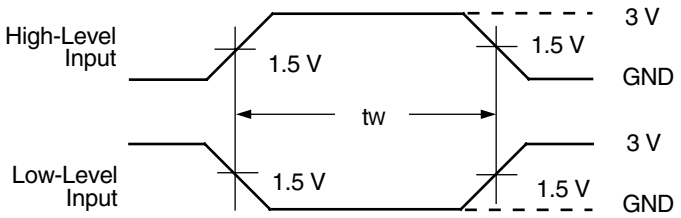
PARAMETER MEASUREMENT INFORMATION



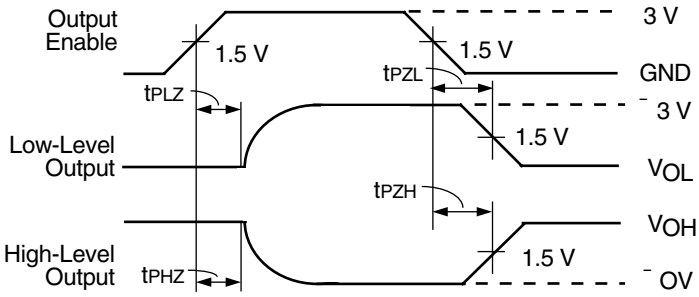
**PROPAGATION DELAY
LOAD CIRCUIT**



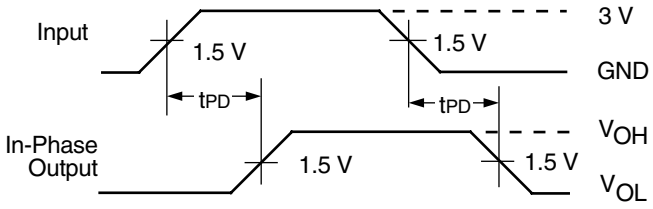
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATIONS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**



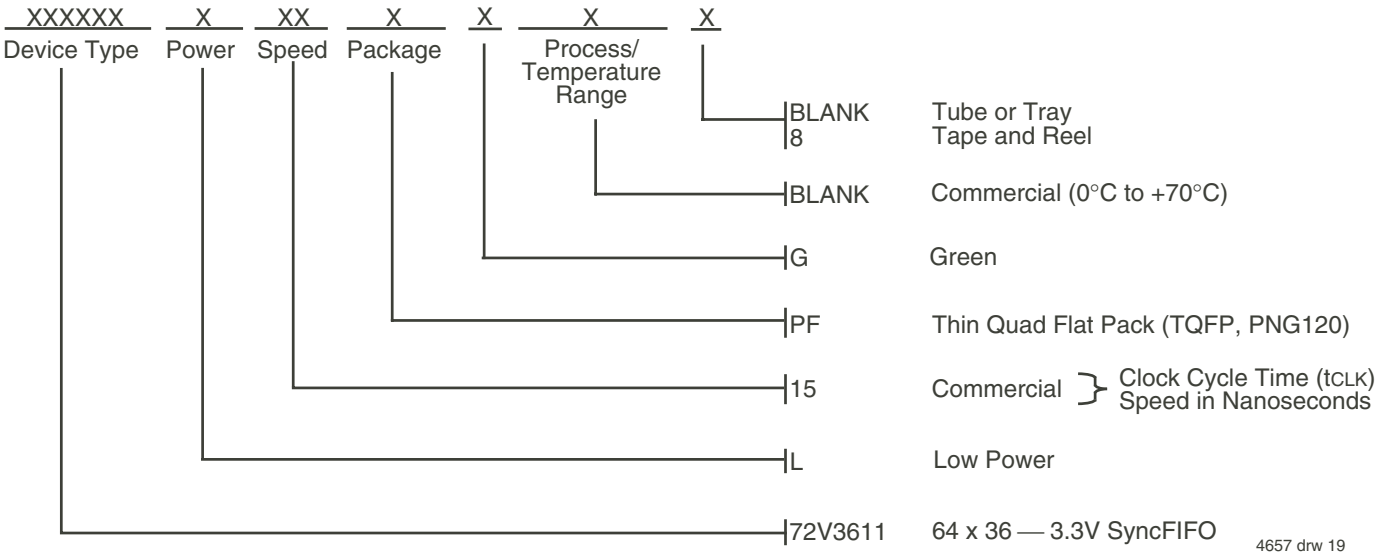
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

4657 drw 18

NOTE:
1. Includes probe and jig capacitance.

Figure 15. Load Circuit and Voltage Waveforms

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

07/10/2000	pg. 1
05/27/2003	pg. 6.
06/07/2005	pgs. 1, 2, 3 and 20.
02/10/2009	pg. 20.
11/07/2013	pgs. 1, 2, 5, 7, 8, 10 and 19.
01/09/2014	pg. 2.

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