ATA6663/ATA6664

LIN Transceiver

DATASHEET

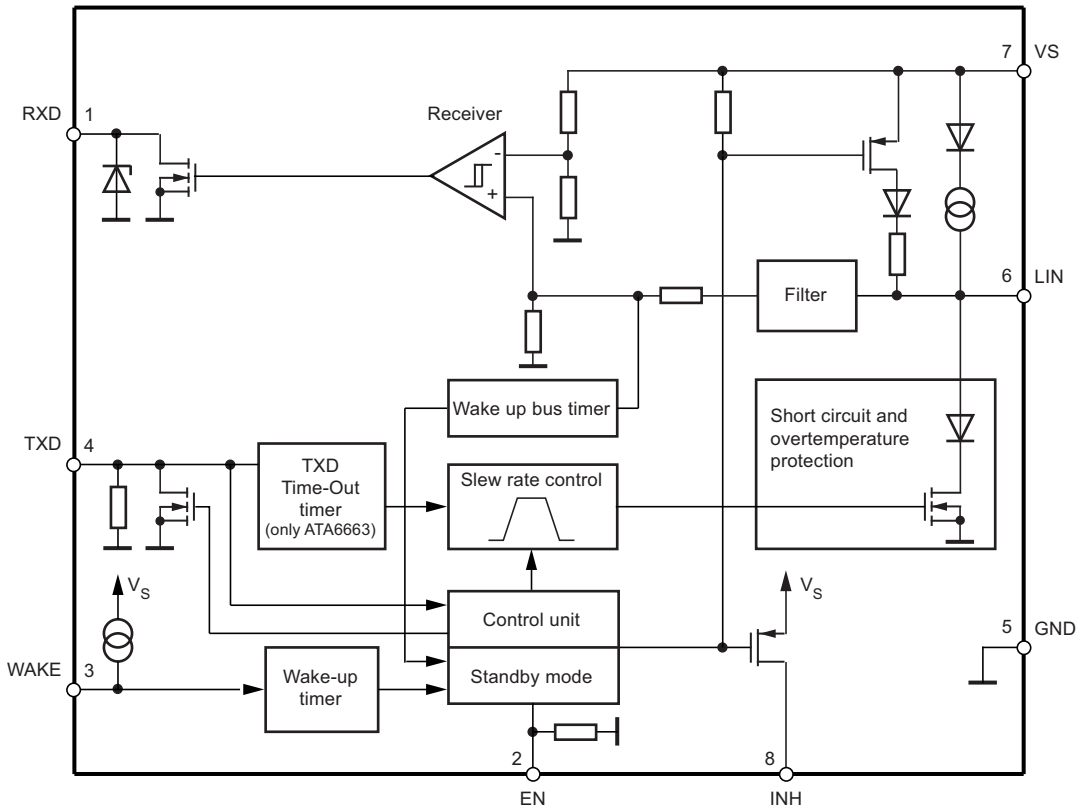
Features

- Operating range from 5V to 27V
- Baud rate up to 20Kbaud
- Improved slew rate control according to LIN specification 2.0, 2.1 and SAEJ2602-2
- Fully compatible with 3.3V and 5V devices
- Atmel® ATA6663: TXD Time-out Timer, Atmel ATA6664: No TXD Time-out Timer
- Normal and Sleep Mode
- Wake-up capability via LIN bus (90µs dominant)
- External wake-up via WAKE Pin (35µs low level)
- INH output to control an external voltage regulator or to switch the master pull-up
- Very low standby current during Sleep Mode (10µA)
- Wake-up source recognition
- Bus pin short-circuit protected versus GND and battery
- LIN input current < 2µA if V_{BAT} is disconnected
- Overtemperature protection
- High EMC level
- Interference and damage protection according to ISO/CD 7637
- Fulfills the OEM “Hardware Requirements for LIN in Automotive Applications Rev.1.1”
- Packages: SO8, DFN8

Description

The Atmel ATA6663 is a fully integrated LIN transceiver complying with the LIN specification 2.0, 2.1 and SAEJ2602-2. The Atmel ATA6664 is an identical version, the only difference is that the TXD-dominant Time-out function is disabled so the device is able to send a static low signal to the LIN bus. It interfaces the LIN protocol handler and the physical layer. The device is designed to handle the low-speed data communication in vehicles, for example, in convenience electronics. Improved slope control at the LIN driver ensures secure data communication up to 20Kbaud. Sleep Mode guarantees minimal current consumption even in the case of a floating bus line or a short circuit on the LIN bus to GND. The ATA6663/ATA6664 feature advanced EMI and ESD performance.

Figure 1. Block Diagram



1. Pin Configuration

Figure 1-1. Pinning SO8, DFN8

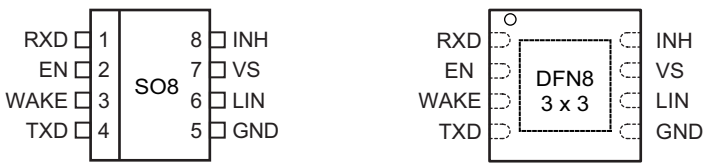


Table 1-1. Pin Description

Pin	Symbol	Function
1	RXD	Receive data output (open drain)
2	EN	Enables normal mode; when the input is open or low, the device is in sleep mode
3	WAKE	High voltage input for local wake-up request. If not needed, connect directly to VS
4	TXD	Transmit data input; active low output (strong pull-down) after a local wake-up request
5	GND	Ground, heat sink
6	LIN	LIN bus line input/output
7	VS	Battery supply
8	INH	Battery-related inhibit output for controlling an external voltage regulator or to switch-off the LIN master pull-up resistor; active high after a wake-up request

2. Functional Description

2.1 Physical Layer Compatibility

Since the LIN physical layer is independent from higher LIN layers (e.g., the LIN protocol layer), all nodes with a LIN physical layer according to LIN2.x can be used along with LIN physical layer nodes, which are according to older versions (i.e., LIN1.0, LIN1.1, LIN1.2, LIN1.3), without any restrictions.

2.2 Supply Pin (V_S)

Undervoltage detection is implemented to disable transmission if V_S falls to a value below 5V in order to avoid false bus messages. After switching on V_S, the IC switches to fail-safe mode and INHIBIT is switched on. The supply current in sleep mode is typically 10µA.

2.3 Ground Pin (GND)

The Atmel ATA6663/ATA6664 does not affect the LIN Bus in the case of a GND disconnection. It is able to handle a ground shift up to 11.5% of V_S.

2.4 Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown, and an internal pull-up resistor are implemented as specified by LIN2.x. The voltage range is from –27V to +40V. This pin exhibits no reverse current from the LIN bus to V_S, even in the case of a GND shift or V_{Batt} disconnection. The LIN receiver thresholds are compatible to the LIN protocol specification.The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope controlled. The output has a self-adapting short-circuit limitation: During current limitation, as the chip temperature increases, the current is reduced.

Note: The internal pull-up resistor is only active in normal and fail-safe mode.

2.5 Input/Output Pin (TXD)

In Normal Mode the TXD pin is the microcontroller interface to control the state of the LIN output. TXD must be at Low- level in order to have a low LIN Bus. If TXD is high, the LIN output transistor is turned off and the Bus is in recessive state. The TXD pin is compatible to both a 3.3V or 5V supply. During fail-safe Mode, this pin is used as output and is signalling the wake- up source (see Section 2.14 “Wake-up Source Recognition” on page 8). It is current limited to < 8mA.

2.6 TXD Dominant Time-out Function (only Atmel ATA6663)

The TXD input has an internal pull-down resistor. An internal timer prevents the bus line from being driven permanently in dominant state. If TXD is forced to low longer than t_{DOM} > 40ms, the pin LIN will be switched off (recessive mode). To reset this mode, TXD needs to be switched to high (> 10µs) before switching LIN to dominant again.

Note: The ATA6664 does not provide this functionality.

2.7 Output Pin (RXD)

This pin forwards information on the state of the LIN bus to the microcontroller. LIN high (recessive) is indicated by a high level at RXD, LIN low (dominant) is reported by a low voltage at RXD. The output is an open drain, therefore, it is compatible to a 3.3V or 5V power supply. The AC characteristics are defined by a pull-up resistor of 5kΩ to 5V and a load capacitor of 20pF. The output is short-current protected. In unpowered mode (V_S = 0V), RXD is switched off. For ESD protection a Zener diode with V_Z = 6.1V is integrated.

2.8 Enable Input Pin (EN)

This pin controls the operation mode of the device. If EN = 1, the device is in normal mode, with the transmission path from TXD to LIN and from LIN to RXD both active. At a falling edge on EN, while TXD is already set to high, the device switches to sleep mode and transmission is not possible. In sleep mode, the LIN bus pin is connected to V_S with a weak pull-up current source. The device can transmit only after being woken up (see Section 2.9, “Inhibit Output Pin (INH)”).

During sleep mode the device is still supplied from the battery voltage. The supply current is typically 10µA. The pin EN provides a pull-down resistor in order to force the transceiver into sleep mode in case the pin is disconnected.

2.9 Inhibit Output Pin (INH)

This pin is used to control an external voltage regulator or to switch on/off the LIN Master pull-up resistor in case the device is used in a Master node. The inhibit pin provides an internal switch towards pin V_S which is protected by temperature monitoring. If the device is in normal or fail-safe mode, the inhibit high-side switch is turned on. When the device is in sleep mode, the inhibit switch is turned off, thus disabling the voltage regulator or other connected external devices.

A wake-up event on the LIN bus or at pin WAKE will switch the INH pin to the V_S level. After a system power-up (V_S rises from zero), the pin INH switches automatically to the V_S level.

2.10 Wake-up Input Pin (WAKE)

This pin is a high-voltage input used to wake-up the device from sleep mode. It is usually connected to an external switch in the application to generate a local wake-up. A pull-up current source with typically –10µA is implemented. The voltage threshold for a wake-up signal is 3V below the VS voltage with an output current of typically –3µA.

If a local wake-up is not needed in the application, pin WAKE can directly be connected to pin VS.

2.11 Operation Modes

1. Normal Mode
   This is the normal transmitting and receiving mode. All features are available.
2. Sleep Mode
   In this mode the transmission path is disabled and the device is in low-power mode. Supply current from V_{Batt} is typically 10µA. A wake-up signal from the LIN bus or via pin WAKE will be detected and will switch the device to fail-safe mode. If EN then switches to high, normal mode is activated. Input debounce timers at pin WAKE (t_{WAKE}), LIN (t_{BUS}) and EN (t_{sleep},t_{nom}) prevent unwanted wake-up events due to automotive transients or EMI. In sleep mode the INH pin remains floating.
   The internal termination between pin LIN and pin V_S is disabled. Only a weak pull-up current (typical 10 µA) between pin LIN and pin V_S is present. Sleep mode can be activated independently from the actual level on pin LIN or WAKE.
3. Fail-safe Mode
   At system power-up or after a wake-up event, the device automatically switches to fail-safe mode. It switches the INH pin to a high state, to the V_S level when VS exceeds 5V. LIN communication is switched off. The microcontroller of the application will then confirm normal mode by setting the EN pin to high.

Figure 2-1. Modes of Operation

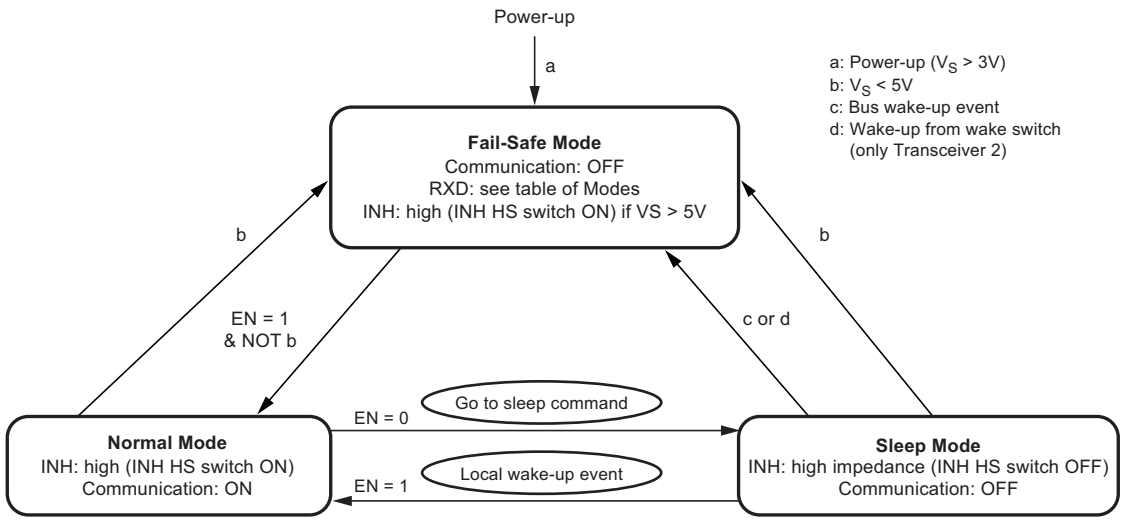


Table 2-1. Table of Operation Modes

Mode of Operation	Transceiver	INH	RXD	LIN
Fail-safe	Off	On, except VS < 5V	High, except after wake-up	Recessive
Normal	On	On	LIN depending	TXD depending
Sleep	Off	Off	High ohmic	Recessive

Wake-up events from sleep mode:

- LIN bus
- EN pin
- WAKE pin
- VS undervoltage

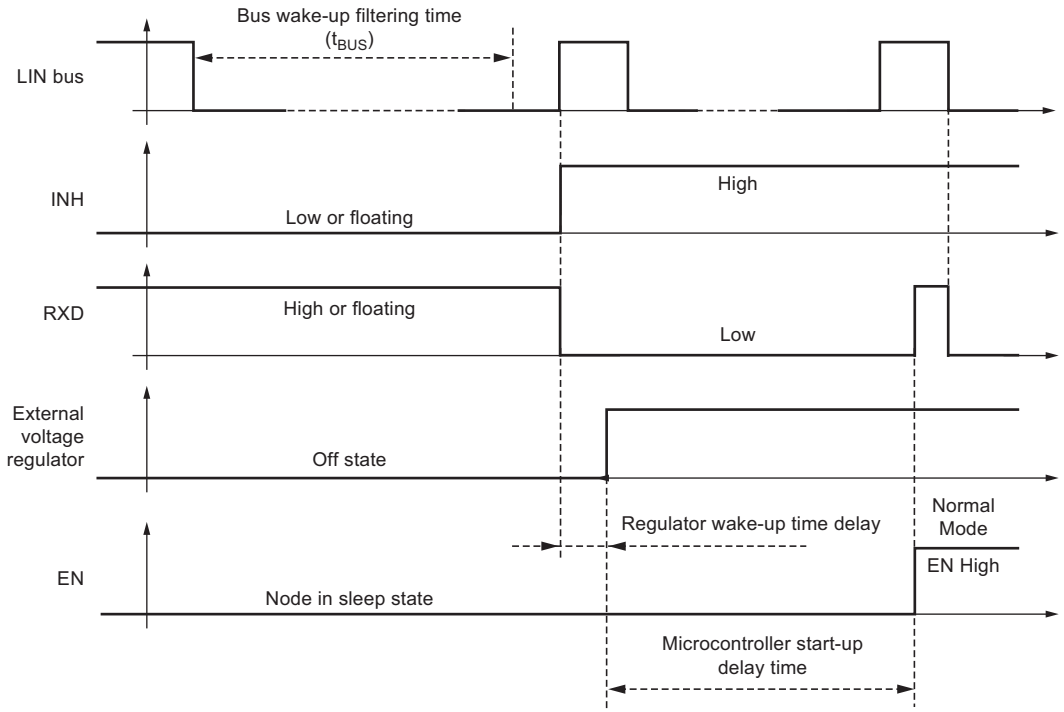
Figure 2-1 on page 4, Figure 2-2 on page 5 and Figure 2-5 on page 8 show the details of wake-up operations.

2.12 Remote Wake-up via Dominant Bus State

A voltage lower than the LIN pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver and starts the wake-up detection timer.

A falling edge at pin LIN, followed by a dominant bus level V_{BUSdom} maintained for a certain time period (> t_{BUS}) and a rising edge at pin LIN results in a remote wake-up request. The device switches to fail-safe mode. Pin INH is activated (switches to V_S) and the internal termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller (see Figure 2-2).

Figure 2-2. LIN Wake-up Waveform Diagram

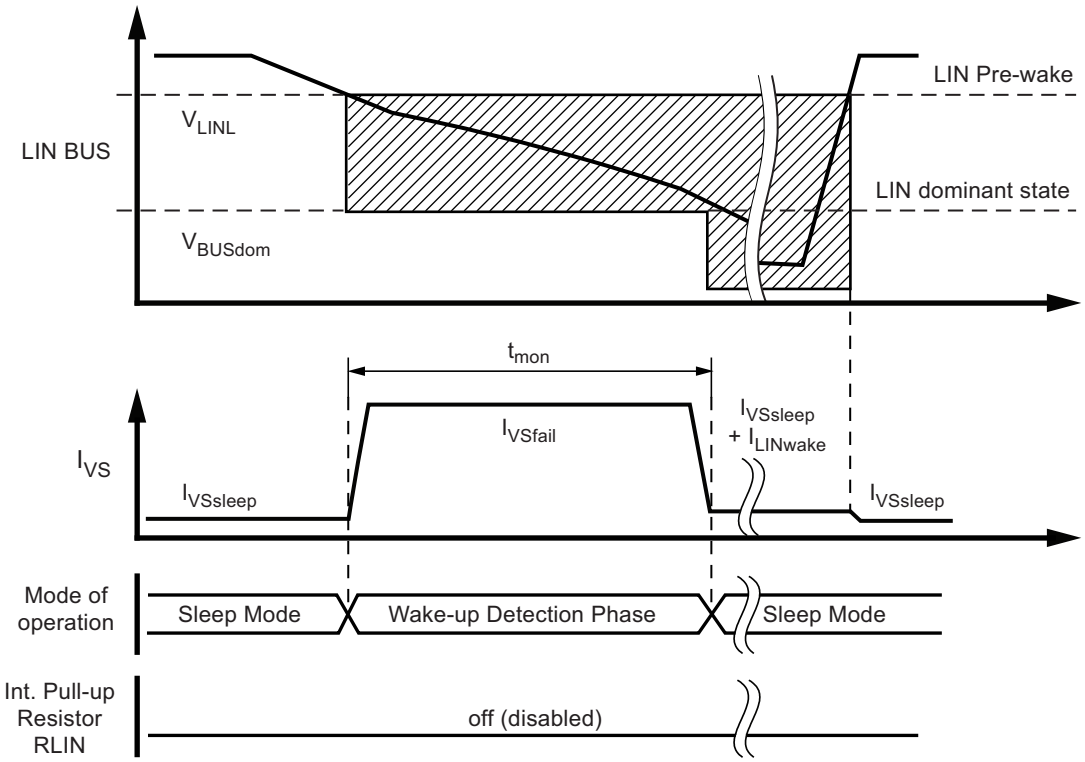


In sleep mode the device has a very low current consumption, even during short-circuits or floating conditions on the bus. A floating bus can arise if the Master pull-up resistor is missing, e.g., in case it is switched off when the LIN Master is in sleep mode or if the power supply of the Master node is switched off.

To minimize the current consumption I_{VS} during voltage levels at the LIN-pin below the LIN pre-wake threshold, the receiver is activated only for a specific time t_{mon}. If t_{mon} elapses while the voltage at the bus is lower than pre-wake detection low (V_{LINL}) and higher than the LIN dominant level, the receiver is switched off again and the circuit reverts to sleep mode. The current consumption is then the result of $I_{VSsleep}$ plus $I_{LINwake}$. If a dominant state is reached on the bus no wake-up will occur. Even if the voltage exceeds the pre-wake detection high (V_{LINH}), the IC will remain in sleep mode (see Figure 2-3 on page 6).

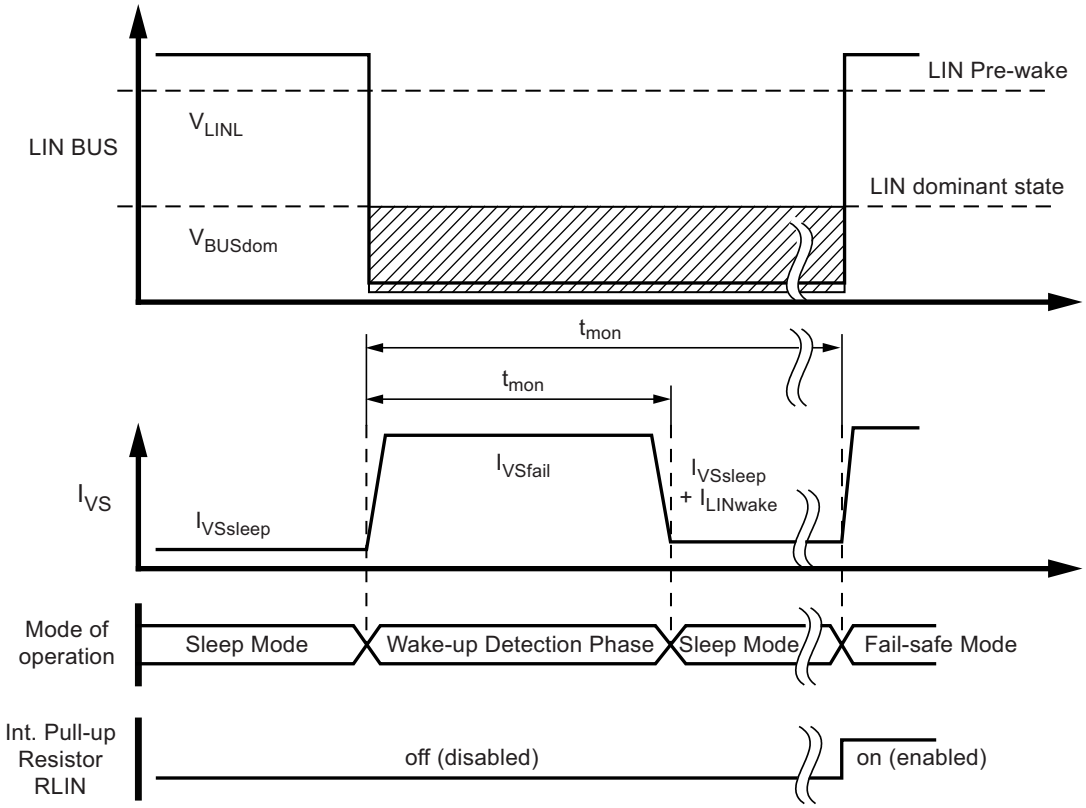
This means the LIN bus must be above the Pre-wake detection threshold V_{LINH} for a few microseconds before a new LIN wake-up is possible.

Figure 2-3. Floating LIN Bus During Sleep Mode



If the Atmel® ATA6663/ATA6664 is in sleep mode and the voltage level at the LIN is in dominant state ($V_{LIN} < V_{BUSdom}$) for a time period exceeding t_{mon} (during a short circuit at LIN, for example), the IC switches back to sleep mode. The VS current consumption then consists of $I_{VSsleep}$ plus $I_{LINWAKE}$. After a positive edge at pin LIN the IC switches directly to fail-safe mode (see Figure 2-4).

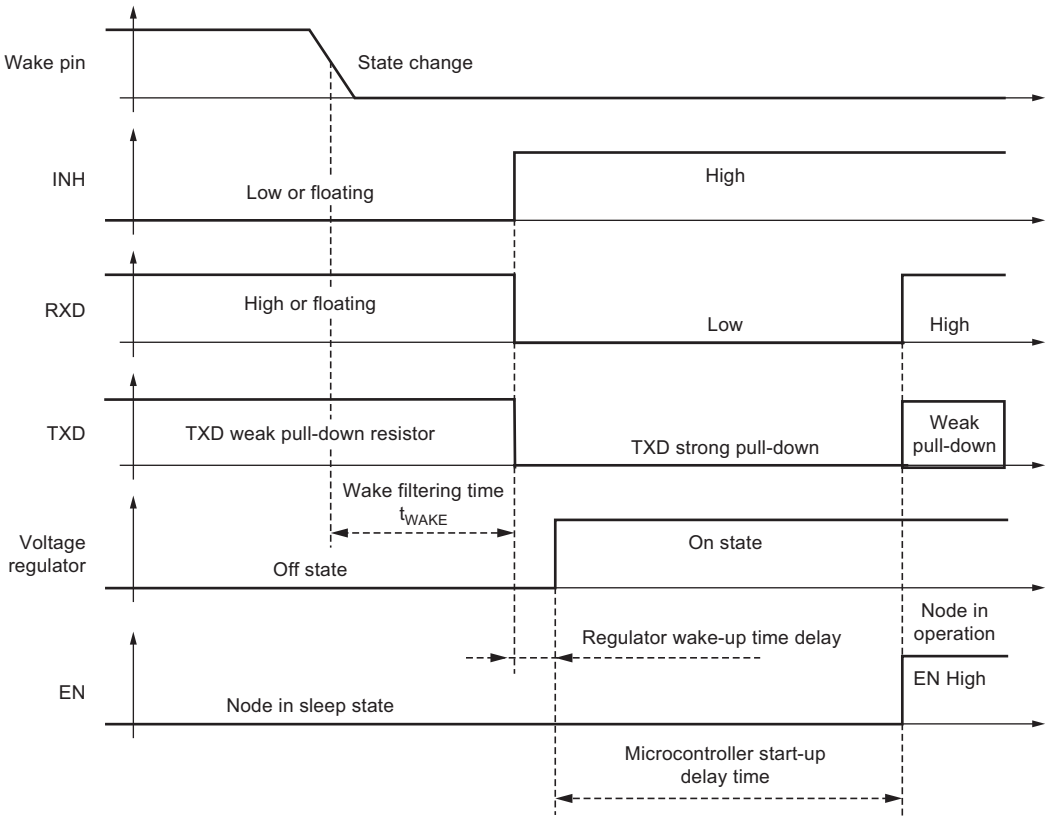
Figure 2-4. Short Circuit to GND on the LIN Bus During Sleep Mode



2.13 Local Wake-up via Pin WAKE

A falling edge at pin WAKE, followed by a low level maintained for a certain time period (> t_{WAKE}), results in a local wake-up request. According to ISO7637, the wake-up time ensures that no transient creates a wake-up. The device then switches to fail-safe mode. Pin INH is activated (switches to V_S) and the internal termination resistor is switched on. The local wake-up request is indicated both by a low level at pin RXD to interrupt the microcontroller and by a strong pull-down at pin TXD (see Figure 2-5). The voltage threshold for a wake-up signal is 3V below the VS voltage with an output current of typically –3µA. Even in case of a continuous low at pin WAKE it is possible to switch the IC into sleep mode via a low level at pin EN. The IC will remain in sleep mode for an unlimited time. To generate a new wake-up at pin WAKE, a high signal > 6µs is required. A negative edge then starts the wake-up filtering time again.

Figure 2-5. Wake-up from Wake-up Switch



2.14 Wake-up Source Recognition

The device can distinguish between a local wake-up request (pin WAKE) and a remote wake-up request (LIN bus). The wake-up source can be read at pin TXD in fail-safe mode. If an external pull-up resistor (typically 5kΩ) has been added on pin TXD to the power supply of the microcontroller, a high level indicates a remote wake-up request (weak pull-down at pin TXD), a low level indicates a local wake-up request (strong pull-down at pin TXD). The wake-up request flag (indicated at pin RXD) as well as the wake-up source flag (indicated at pin TXD) are reset immediately if the microcontroller sets pin EN to high (see Figure 2-2 on page 5 and Figure 2-5 on page 8).

2.15 Fail-safe Features

- During a short-circuit at LIN to V_{BAT}, the output limits the output current to IBUS_LIM. Due to the power dissipation, the chip temperature exceeds T_{off}, and the LIN output is switched off. The chip cools down, and after a hysteresis of T_{hys}, it switches the output on again.
- During a short-circuit from LIN to GND the IC can be switched to sleep mode, and even in this case the current consumption is lower than 45µA. When the short-circuit has elapsed, the IC starts with a remote wake-up.
- If the Atmel® ATA6663/ATA6664 is in sleep mode and a floating condition occurs on the bus, the IC switches back to sleep mode automatically. The current consumption is lower than 45µA in this case.
- The reverse current is < 2µA at pin LIN during loss of V_{BAT}. This is the best behavior for bus systems where some slave nodes are supplied from battery or ignition.
- Pin EN provides a pull-down resistor to force the transceiver into sleep mode if EN is disconnected
- Pin RXD is set floating if V_{BAT} is disconnected
- Pin TXD provides a pull-down resistor to provide a static low if TXD is disconnected
- After switching the IC into Normal Mode the TXD pin must be pulled to high longer than 10µs in order to activate the LIN driver. This feature prevents the bus from being driven into dominant state when the IC is switched into Normal Mode and TXD is low.
- The INH output transistor is protected by temperature monitoring

3. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
V_S - Continuous supply voltage		–0.3		+40	V
Wake DC and transient voltage (with 2.7kΩ serial resistor) - Transient voltage according to ISO7637 (coupling 1nF)		–3 –150		+40 +100	V V
Logic pins (RXD, TXD, EN)		–0.3		+5.5	V
LIN - DC voltage - Transient voltage according to ISO7637 (coupling 1nF)		 –27 –150		 +40 +100	 V V
INH - DC voltage		–0.3		V_S + 0.3	V
ESD according to IBEE LIN EMC Test specification 1.0 according to IEC 61000-4-2 - Pin VS, LIN to GND - Pin WAKE (2.7kΩ serial resistor)		 ±8 ±6			 KV KV
ESD HBM according to STM5.1 with 1.5kΩ / 100pF - Pin VS, LIN, WAKE, INH to GND		±6			KV
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002)		±3			KV
CDM ESD STM 5.3.1		±750			V
Machine Model ESD AEC-Q100-Rev.F (003)		±200			V
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_{stg}	–55		+150	°C

4. Thermal Characteristics SO8

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction ambient	R_{thJA}			145	K/W
Special heat sink at GND (pin 5) on PCB (fused lead frame to pin 5)	R_{thJA}		80		K/W
Thermal shutdown	T_{off}	150	165	180	°C
Thermal shutdown hysteresis	T_{hys}	5	10	20	°C

5. Thermal Characteristics DFN8

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction to heat slug	R_{thJC}		10		K/W
Thermal resistance junction to ambient, where heat slug is soldered to PCB according to JEDEC	R_{thJA}		50		K/W
Thermal shutdown	T_{off}	150	165	180	°C
Thermal shutdown hysteresis	T_{hys}	5	10	20	°C

6. Electrical Characteristics

$5V < V_S < 27V$, $T_j = –40°C$ to $+150°C$

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	V_S Pin								
1.1	DC voltage range nominal		7	V_S	5	13.5	27	V	A
1.2	Supply current in sleep mode	Sleep mode $V_{LIN} > V_S – 0.5V$ $V_S < 14V$	7	$I_{VSsleep}$		10	20	µA	A
		Sleep mode, bus shorted to GND $V_{LIN} = 0V$ $V_S < 14V$	7	$I_{VSsleep\_sc}$		23	45	µA	A
1.3	Supply current in normal mode	Bus recessive $V_S < 14V$	7	I_{VSrec}		0.9	1.3	mA	A
1.4		Bus dominant $V_S < 14V$ Total bus load > 500Ω	7	I_{VSdom}		1.2	2	mA	A
1.5	Supply current in fail-safe mode	Bus recessive $V_S < 14V$	7	I_{VSfail}	0.5		1.1	mA	A
1.6	V_S undervoltage threshold on		7	V_{Sth}	4		4.95	V	A
1.7	V_S undervoltage threshold off		7	V_{Sth}	4.05		5	V	A
1.8	V_S undervoltage threshold hysteresis		7	V_{Sth_hys}	50		500	mV	A
2	RXD Output Pin (Open Drain)								
2.1	Low-level output sink current	Normal mode $V_{LIN} = 0V$, $V_{RXD} = 0.4V$	1	I_{RXDL}	1.3	2.5	8	mA	A
2.2	RXD saturation voltage	5-kΩ pull-up resistor to 5V	1	$Vsat_{RXD}$			0.4	V	A
2.3	High-level leakage current	Normal mode $V_{LIN} = V_{BAT}$, $V_{RXD} = 5V$	1	I_{RXDH}	–3		+3	µA	A
2.4	ESD Zener diode	$I_{RXD} = 100µA$	1	VZ_{RXD}	5.8		8.6	V	A
3	TXD Input Pin								
3.1	Low-level voltage input		4	V_{TXDL}	–0.3		+0.8	V	A
3.2	High-level voltage input		4	V_{TXDH}	2		5.5	V	A
3.3	Pull-down resistor	$V_{TXD} = 5V$	4	R_{TXD}	125	250	600	kΩ	A
3.4	Low-level leakage current	$V_{TXD} = 0V$	4	I_{TXD_leak}	–3		+3	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

6. Electrical Characteristics (Continued)

5V < V_S < 27V, T_j = –40°C to +150°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.5	Low-level output sink current	Fail-safe mode, local wake-up V_{TXD} = 0.4V V_{LIN} = V_{BAT}	4	I_{TXD}	1.3	2.5	8	mA	A
4	EN Input Pin								
4.1	Low-level voltage input		2	V_{ENL}	–0.3		+0.8	V	A
4.2	High-level voltage input		2	V_{ENH}	2		5.5	V	A
4.3	Pull-down resistor	V_{EN} = 5V	2	R_{EN}	125	250	600	kΩ	A
4.4	Low-level input current	V_{EN} = 0V	2	I_{EN}	–3		+3	µA	A
5	INH Output Pin								
5.1	High-level voltage	Normal or fail-safe mode I_{INH} = –15mA	8	V_{INHH}	V_S – 0.75		V_S	V	A
5.2	Switch-on resistance between VS and INH	Normal or fail-safe mode	8	R_{INH}		30	50	Ω	A
5.3	Leakage current	Sleep mode V_{INH} = 0V/27V, V_S = 27V	8	I_{INHL}	–3		+3	µA	A
6	WAKE Pin								
6.1	High-level input voltage		3	V_{WAKEH}	V_S – 1V		V_S + 0.3V	V	A
6.2	Low-level input voltage	I_{WAKE} = typically –3µA	3	V_{WAKEL}	–1V		V_S – 3.3V	V	A
6.3	Wake pull-up current	V_S < 27V	3	I_{WAKE}	–30	–10		µA	A
6.4	High-level leakage current	V_S = 27V, V_{WAKE} = 27V	3	I_{WAKE}	–5		+5	µA	A
7	LIN Bus Driver								
7.1	Driver recessive output voltage	R_{LOAD} = 500Ω / 1kΩ	6	V_{BUSrec}	0.9 × V_S		V_S	V	A
7.2	Driver dominant voltage $V_{BUSdom\_DRV\_LoSUP}$	V_{VS} = 7V, R_{load} = 500Ω	6	$V_{\_LoSUP}$			1.2	V	A
7.3	Driver dominant voltage $V_{BUSdom\_DRV\_HiSUP}$	V_{VS} = 18V, R_{load} = 500Ω	6	$V_{\_HiSUP}$			2	V	A
7.4	Driver dominant voltage $V_{BUSdom\_DRV\_LoSUP}$	V_{VS} = 7V, R_{load} = 1000Ω	6	$V_{\_LoSUP\_1k}$	0.6			V	A
7.5	Driver dominant voltage $V_{BUSdom\_DRV\_HiSUP}$	V_{VS} = 18V, R_{load} = 1000Ω	6	$V_{\_HiSUP\_1k\_}$	0.8			V	A
7.6	Pull-up resistor to V_S	The serial diode is mandatory	6	R_{LIN}	20	30	47	kΩ	A
7.7	Voltage drop at the serial diodes	In pull-up path with R_{slave} $I_{SerDiode}$ = 10mA	6	$V_{SerDiode}$	0.4		1.0	V	D
7.8	LIN current limitation V_{BUS} = V_{BAT_max}		6	I_{BUS_LIM}	40	120	200	mA	A
7.9	Input leakage current at the receiver, including pull-up resistor as specified	Input leakage current Driver off V_{BUS} = 0V, V_S = 12V	6	$I_{BUS\_PAS\_dom}$	–1			mA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

6. Electrical Characteristics (Continued)

$5V < V_S < 27V$, $T_j = –40°C$ to $+150°C$

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.10	Leakage current LIN recessive	Driver off $8V < V_{BAT} < 18V$ $8V < V_{BUS} < 18V$ $V_{BUS} \geq V_{BAT}$	6	$I_{BUS\_PAS\_rec}$		10	20	µA	A
7.11	Leakage current at ground loss; control unit disconnected from ground; loss of local ground must not affect communication in the residual network	$GND_{Device} = V_S$ $V_{BAT} = 12V$ $0V < V_{BUS} < 18V$	6	$I_{BUS\_NO\_Gnd}$	–10	+0.5	+10	µA	A
7.12	Leakage current at loss of battery; node has to substain the current that can flow under this condition; bus must remain operational under this condition	V_{BAT} disconnected $V_{SUP\_Device} = GND$ $0V < V_{BUS} < 18V$	6	$I_{BUS\_NO\_Bat}$		0.1	2	µA	A
7.13	Capacitance on pin LIN to GND		6	C_{LIN}			20	pF	D
8	LIN Bus Receiver								
8.1	Center of receiver threshold	$V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec}) / 2$	6	V_{BUS_CNT}	$0.475 \times V_S$	$0.5 \times V_S$	$0.525 \times V_S$	V	A
8.2	Receiver dominant state	$V_{EN} = 5V$	6	V_{BUSdom}	–27		$0.4 \times V_S$	V	A
8.3	Receiver recessive state	$V_{EN} = 5V$	6	V_{BUSrec}	$0.6 \times V_S$		40	V	A
8.4	Receiver input hysteresis	$V_{HYS} = V_{th\_rec} – V_{th\_dom}$	6	V_{BUShys}	$0.028 \times V_S$	$0.1 \times V_S$	$0.175 \times V_S$	V	A
8.5	Pre-wake detection LIN High-level input voltage		6	V_{LINH}	V_S – 2V		V_S + 0.3V	V	A
8.6	Pre-wake detection LIN Low-level input voltage	Switches the LIN receiver on	6	V_{LINL}	–27V		V_S – 3.3V	V	A
8.7	LIN Pre-wake pull-up current	$V_S < 27V$ $V_{LIN} = 0V$	6	$I_{LINWAKE}$	–30	–10		µA	A
9	Internal Timers								
9.1	Dominant time for wake-up via LIN bus	$V_{LIN} = 0V$	6	t_{BUS}	30	90	150	µs	A
9.2	Time of low pulse for wake-up via pin WAKE	$V_{WAKE} = 0V$	3	t_{WAKE}	7	35	50	µs	A
9.3	Time delay for mode change from fail-safe mode to normal mode via pin EN	$V_{EN} = 5V$	2	t_{norm}	2	7	15	µs	A
9.4	Time delay for mode change from normal mode into sleep mode via pin EN	$V_{EN} = 0V$	2	t_{sleep}	7	15	24	µs	A
9.5	Atmel ATA6663: TXD dominant time out time	$V_{TXD} = 0V$	4	t_{dom}	40	60	85	ms	A
9.6	Power-up delay between $V_S = 5V$ until INH switches to high	$V_{VS} = 5V$	7, 8	t_{VS}			200	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

6. Electrical Characteristics (Continued)

5V < V_S < 27V, T_j = –40°C to +150°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9.7	Monitoring time for wake-up via LIN bus		6	t_{mon}	6	10	15	ms	A
10	LIN Bus Driver AC Parameter with Different Bus Loads Load 1 (small): 1nF, 1kΩ ; Load 2 (large): 10nF, 500Ω ; R_{RXD} = 5kΩ ; C_{RXD} = 20pF; Load 3 (medium): 6.8nF, 660Ω characterized on samples; 10.1 and 10.2 specifies the timing parameters for proper operation at 20Kbit/s, 10.3 and 10.4 at 10.4Kbit/s.								
10.1	Duty cycle 1	$TH_{Rec(max)} = 0.744 \times V_S$ $TH_{Dom(max)} = 0.581 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 50µs D1 = $t_{bus\_rec(min)} / (2 \times t_{Bit})$	6	D1	0.396				A
10.2	Duty cycle 2	$TH_{Rec(min)} = 0.422 \times V_S$ $TH_{Dom(min)} = 0.284 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 50µs D2 = $t_{bus\_rec(max)} / (2 \times t_{Bit})$	6	D2			0.581		A
10.3	Duty cycle 3	$TH_{Rec(max)} = 0.778 \times V_S$ $TH_{Dom(max)} = 0.616 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 96µs D3 = $t_{bus\_rec(min)} / (2 \times t_{Bit})$	6	D3	0.417				A
10.4	Duty cycle 4	$TH_{Rec(min)} = 0.389 \times V_S$ $TH_{Dom(min)} = 0.251 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 96µs D4 = $t_{bus\_rec(max)} / (2 \times t_{Bit})$	6	D4			0.590		A
11	Receiver Electrical AC Parameters of the LIN Physical Layer LIN receiver, RXD load conditions: C_{RXD} = 20pF, $R_{pull-up}$ = 5kΩ								
11.1	Propagation delay of receiver (see Figure 6-1 on page 14)	$t_{rec\_pd} = \max(t_{rx\_pdr}, t_{rx\_pdf})$ V_S = 7.0V to 18V	1	t_{rx_pd}			6	µs	A
11.2	Symmetry of receiver propagation delay rising edge minus falling edge	$t_{rx\_sym} = t_{rx\_pdr} – t_{rx\_pdf}$ V_S = 7.0V to 18V	1	t_{rx_sym}	–2		+2	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 6-1. Definition of Bus Timing Parameter

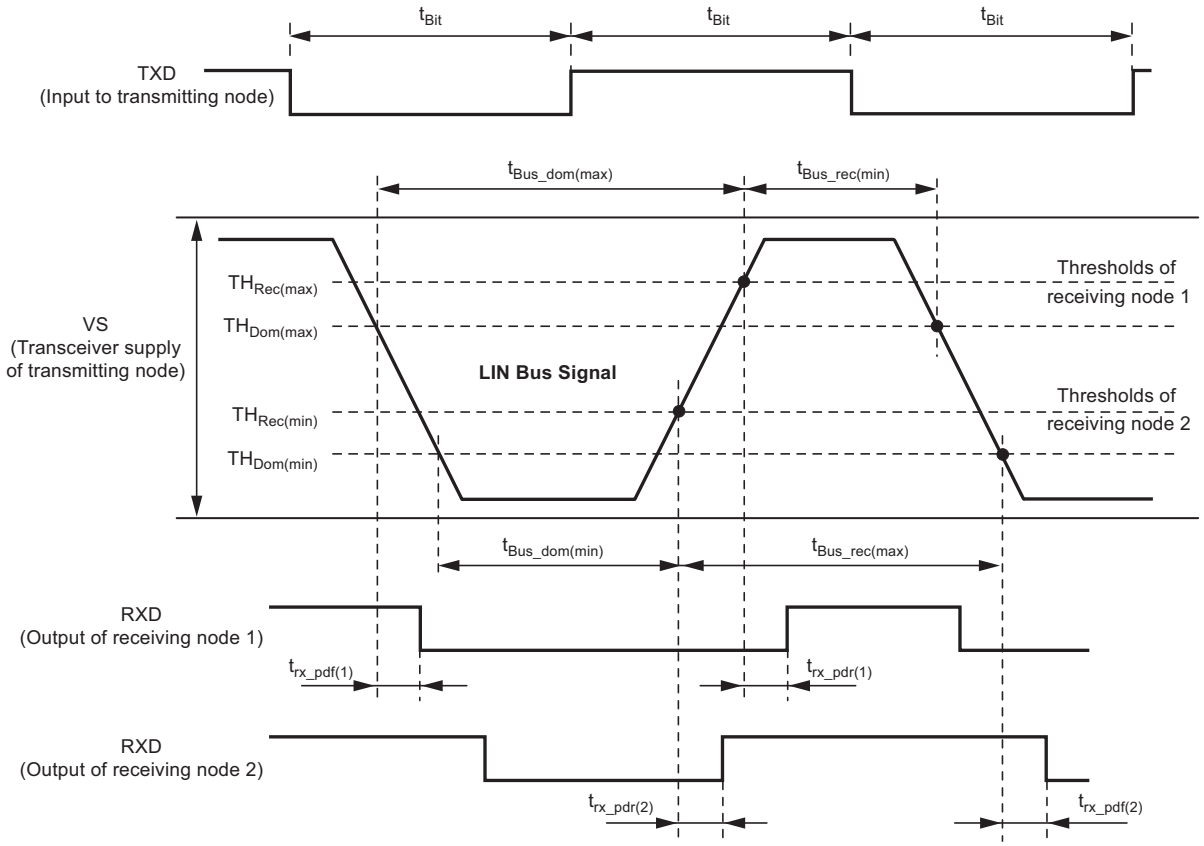
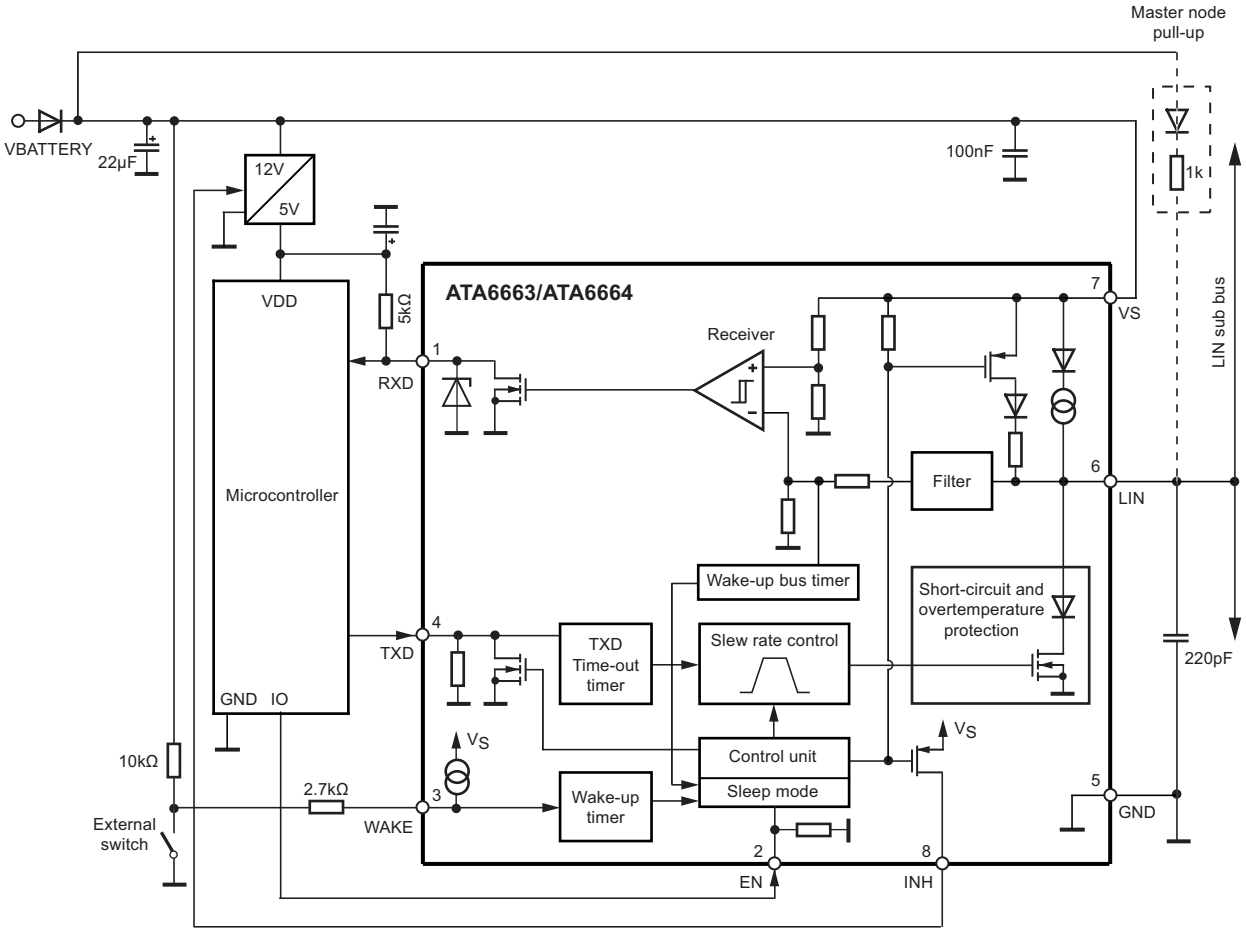


Figure 6-2. Application Circuit

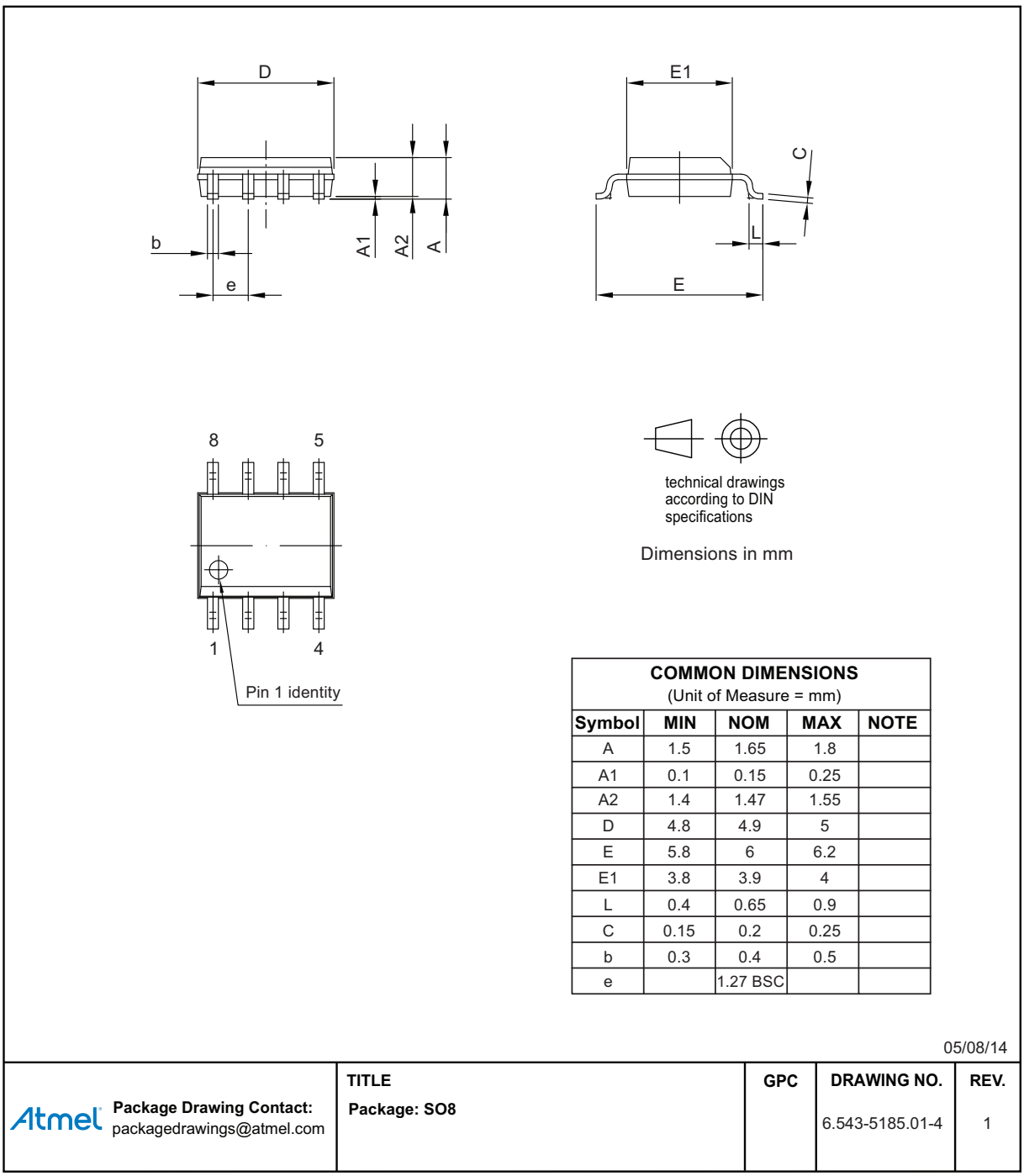


7. Ordering Information

Extended Type Number	Package	Remarks
ATA6663-FAQW-1	DFN8	LIN transceiver, Pb-free, 6k, taped and reeled
ATA6663-GAQW	SO8	LIN transceiver, Pb-free, 4k, taped and reeled
ATA6664-GAQW	SO8	LIN transceiver, Pb-free, 4k, taped and reeled

8. Package Information

Figure 8-1. SO8



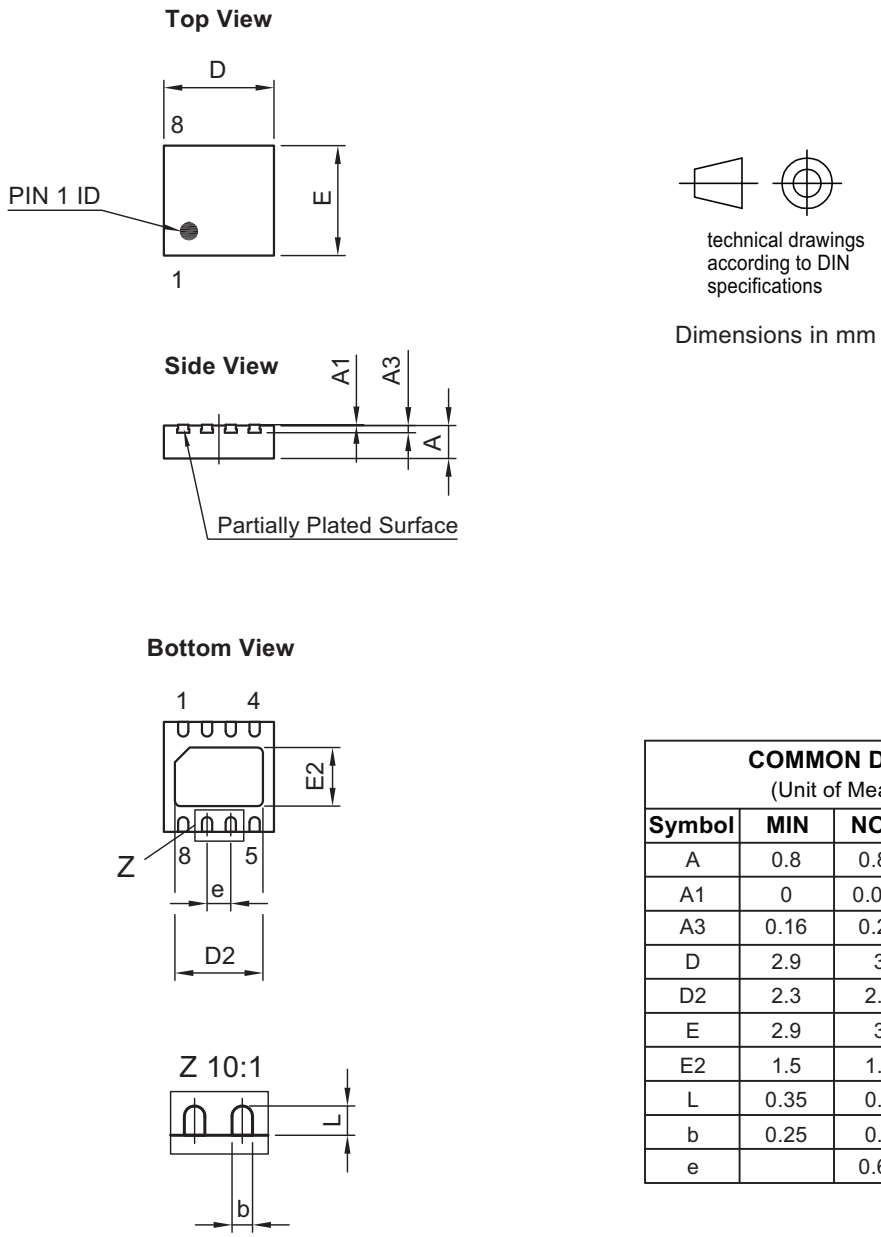
COMMON DIMENSIONS
(Unit of Measure = mm)

Symbol	MIN	NOM	MAX	NOTE
A	1.5	1.65	1.8	
A1	0.1	0.15	0.25	
A2	1.4	1.47	1.55	
D	4.8	4.9	5	
E	5.8	6	6.2	
E1	3.8	3.9	4	
L	0.4	0.65	0.9	
C	0.15	0.2	0.25	
b	0.3	0.4	0.5	
e		1.27 BSC		

05/08/14

Package Drawing Contact: packagedrawings@atmel.com	TITLE Package: SO8	GPC	DRAWING NO. 6.543-5185.01-4	REV. 1

Figure 8-2. DFN8



COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	0.8	0.85	0.9	
A1	0	0.035	0.05	
A3	0.16	0.21	0.26	
D	2.9	3	3.1	
D2	2.3	2.4	2.5	
E	2.9	3	3.1	
E2	1.5	1.6	1.7	
L	0.35	0.4	0.45	
b	0.25	0.3	0.35	
e		0.65		

10/11/13

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** packagedrawings@atmel.com	**Package: VDFN_3x3_8L** Exposed pad 2.4x1.6		6.543-5165.03-4	1

9. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9146I-AUTO-10/14	• Put datasheet in the latest template • Section 7 “Ordering Information” on page 16 updated • Section 8 “Package Information” on pages 16 to 17 updated
9146H-AUTO-03/14	• Section 7 “Ordering Information” on page 16: Order quantity of ATA6663-FAQW updated
9146G-AUTO-06/12	• Section 5“Electrical Characteristics” numbers 3.2 and 4.2 on page 10 to 11 updated
9146F-AUTO-10/11	• Section 6 “Thermal Characteristics DFN8” on page 10 implemented
9146E-AUTO-03/11	• Figure 1-1 “Block Diagram” on page 2 updated • Section 3.15 “Fail-safe Features” on page 9 updated
9146D-AUTO-09/10	• Section 7 “Ordering Information” on page 17 updated • Section 8 “Package Information” on pages 17 to 18 updated
9146C-AUTO-07/10	• Section 6 “Electrical Characteristics” numbers 9.4 and 9.5 on page 13 updated
9146B-AUTO-05/10	• Features updated • Headings 3.6 and 3.10: text updated • Abs.Max.Ratings table: row “ESD HBM according to STM5.1” updated

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