

### FEATURES

- 3.3V power supply
- 50ps output-to-output skew
- Low power
- Synchronous enable/disable
- Multiplexed clock input
- 75KΩ internal input pull-down resistors
- Available in 16-pin SOIC package



Precision Edge®

### DESCRIPTION

The SY100EL15L is a low skew 1:4 clock distribution IC designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. If a single-ended input is to be used the VBB output should be connected to the  $\overline{\text{CLK}}$  input and bypassed to ground via a 0.01μF capacitor. The VBB output is designed to act as the switching reference for the input of the EL15 under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The EL15 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pull-down resistor) the SEL pin will select the differential clock input.

The common enable ( $\overline{\text{EN}}$ ) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

When both differential inputs are left open, CLK input will pull down to VEE and  $\overline{\text{CLK}}$  input will bias around  $V_{cc}/2$ .

### PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
SCLK	Synchronous Clock Input
$\overline{\text{EN}}$	Synchronous Enable
SEL	Clock Select Input
VBB	Reference Output
Q0-3	Differential Clock Outputs

### TRUTH TABLE

CLK	SCLK	SEL	$\overline{\text{EN}}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

\* On next negative transition of CLK or SCLK

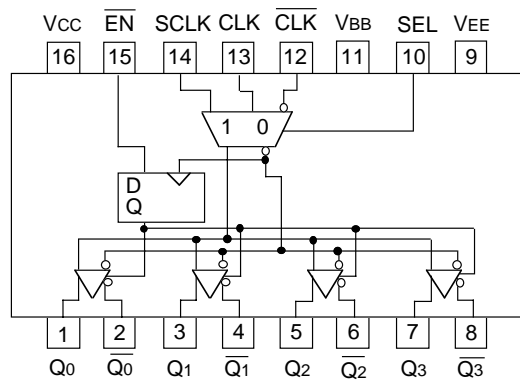
**PACKAGE/ORDERING INFORMATION**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100EL15LZC	Z16-2	Commercial	SY100EL15LZC	Sn-Pb
SY100EL15LZCTR <sup>(2)</sup>	Z16-2	Commercial	SY100EL15LZC	Sn-Pb
SY100EL15LZI	Z16-2	Industrial	SY100EL15LZI	Sn-Pb
SY100EL15LZITR <sup>(2)</sup>	Z16-2	Industrial	SY100EL15LZI	Sn-Pb
SY100EL15LZG <sup>(3)</sup>	Z16-2	Industrial	SY100EL15LZG with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EL15LZGTR <sup>(2, 3)</sup>	Z16-2	Industrial	SY100EL15LZG with Pb-Free bar-line indicator	Pb-Free NiPdAu

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.



**16-Pin SOIC (Z16-2)**

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Value	Unit
V <sub>EE</sub>	Power Supply (V <sub>CC</sub> = 0V)	-8.0 to 0	VDC
V <sub>IN</sub>	Input Voltage (V <sub>CC</sub> = 0V)	0 to -6.0	VDC
I <sub>OUT</sub>	Output Current -Continuous -Surge	50 100	mA
T <sub>LEAD</sub>	Lead Temperature (soldering, 20sec.)	+260	°C
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C

**Notes:**

1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
2. Parametric values specified at: 3 volt Power Supply Range 100EL15L Series -3.0V to -3.8V

**DC ELECTRICAL CHARACTERISTICS**V<sub>EE</sub> = 3.3V ±10%; V<sub>CC</sub> = GND<sup>(1)</sup>

Symbol	Parameter	T <sub>A</sub> = -40°C		T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C			T <sub>A</sub> = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage <sup>(2)</sup>	-1085	-880	-1025	-880	-1025	-955	-880	-1025	-880	mV
V <sub>OL</sub>	Output LOW Voltage <sup>(2)</sup>	-1830	-1555	-1810	-1620	-1810	-1705	-1620	-1810	-1620	mV
V <sub>OHA</sub>	Output HIGH Voltage <sup>(3)</sup>	-1095	—	-1035	—	-1035	—	—	-1035	—	mV
V <sub>OLA</sub>	Output LOW Voltage <sup>(3)</sup>	—	-1555	—	-1610	—	—	-1610	—	-1610	mV
V <sub>IH</sub>	Input HIGH Voltage	-1165	-880	-1165	-880	-1165	—	-880	-1165	-880	mV
V <sub>IL</sub>	Input LOW Voltage	-1810	-1475	-1810	-1475	-1810	—	-1475	-1810	-1475	mV
I <sub>IH</sub>	Input High Current	—	150	—	150	—	—	150	—	150	μA
I <sub>IL</sub>	Input LOW Current <sup>(4)</sup> CLK	0.5 -300	— —	0.5 -300	— —	0.5 -300	— —	— —	0.5 -300	— —	μA
I <sub>EE</sub>	Power Supply Current	—	35	—	35	—	25	35	—	38	mA
V <sub>BB</sub>	Output Reference Voltage	-1.38	-1.26	-1.38	-1.26	-1.38	—	-1.26	-1.38	-1.26	V

**Notes:**

1. This table replaces the three traditionally seen in ECL 100K data books. Outputs are terminated through a 50Ω resistor to -2.0V.
2. V<sub>IN</sub> = V<sub>IH</sub>(Max) or V<sub>IL</sub>(Min).
3. V<sub>IN</sub> = V<sub>IH</sub>(Min) or V<sub>IL</sub>(Max).
4. V<sub>IN</sub> = V<sub>IL</sub>(Max).

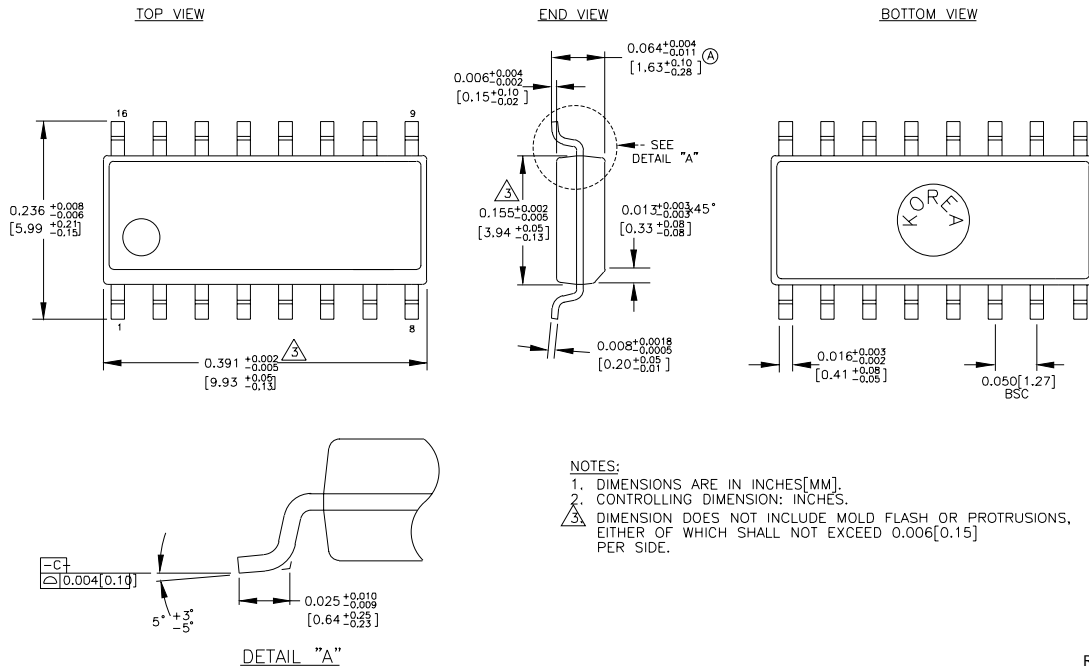
**AC ELECTRICAL CHARACTERISTICS**V<sub>EE</sub> = 3.3V ±10%; V<sub>CC</sub> = GND<sup>(1)</sup>

Symbol	Parameter	T <sub>A</sub> = -40°C		T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C			T <sub>A</sub> = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
t <sub>PD</sub>	Propagation Delay CLK to Q (Diff)	460	660	470	670	470	—	670	500	700	ps
	CLK to Q (SE)	410	710	420	720	420	—	720	450	750	
	SCLK to Q	410	710	420	720	420	—	720	470	750	
t <sub>skew</sub>	Part-to-Part Skew <sup>(1)</sup>	—	200	—	200	—	—	200	—	200	ps
	Within-Device Skew	—	50	—	50	—	—	50	—	50	
t <sub>S</sub>	Setup Time $\overline{EN}$	150	—	150	—	150	—	—	150	—	ps
t <sub>H</sub>	Hold Time $\overline{EN}$	400	—	400	—	400	—	—	400	—	ps
V <sub>PP</sub>	Minimum Input Swing CLK	250	—	250	—	250	—	—	250	—	mV
V <sub>CMR</sub>	Common Mode Range <sup>(2)</sup>										mV
	V <sub>PP</sub> < 500mV	-2.0	-0.4	-2.1	-0.4	-2.1	—	-0.4	-2.1	-0.4	
	V <sub>PP</sub> ≥ 500mV	-1.8	-0.4	-1.9	-0.4	-1.9	—	-0.4	-1.9	-0.4	
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times <sub>Q</sub> (20% – 80%)	375	625	325	575	325	—	575	325	575	ps

**Notes:**

- Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
- V<sub>CMR</sub> is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signals are within the V<sub>CMR</sub> range and the input swing is greater than V<sub>PP</sub>(Min.) and <1V. The lower end of the V<sub>CMR</sub> range varies 1:1 with V<sub>EE</sub>. The numbers in the spec table assume a nominal V<sub>EE</sub> = -3.3V. Note for PECL operation, the V<sub>CMR</sub>(Min) will be fixed at 3.3V - |V<sub>CMR</sub>(Min)|.

**16-PIN SOIC .150" WIDE (Z16-2)**



Rev. 02

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

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