

AT-213-PIN

Digital Attenuator
15.0 dB, 4-Bit, TTL Driver, DC-3.0 GHz

Rev. V5

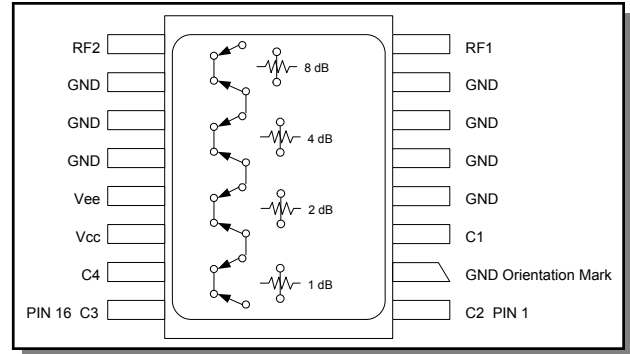
Features

- Attenuation: 1 dB steps to 15 dB
- Temperature Stability: ± 0.18 dB from -55°C to $+85^{\circ}\text{C}$ Typical
- Low DC Power Consumption
- Hermetic Surface Mount Package
- Integral TTL Driver
- 50 Ohms Nominal Impedance
- Lead-Free CR-11 Package
- 260°C Reflow Compatible
- RoHS* Compliant

Description

M/A-COM's AT-213-PIN is a 4-bit, 1 dB step digital attenuator in a hermetically sealed ceramic 16-lead surface mount package. The AT-213-PIN is ideally suited for use where high accuracy, fast switching, very low power consumption and low intermodulation products are required. Typical applications include dynamic range setting in a precision receiver circuits and other gain/leveling control circuits. Environmental screening is available. Contact the factory for information.

Functional Schematic



Ordering Information

| Part Number | Package |
|-------------|----------------|
| AT-213-PIN | Bulk Packaging |

Note: Reference Application Note M513 for reel size information.

Pin Configuration

| Pin No. | Function | Pin No. | Function |
|---------|----------|---------|----------|
| 1 | C2 | 9 | RF2 |
| 2 | GND | 10 | GND |
| 3 | C1 | 11 | GND |
| 4 | GND | 12 | GND |
| 5 | GND | 13 | Vee |
| 6 | GND | 14 | Vcc |
| 7 | GND | 15 | C4 |
| 8 | RF1 | 16 | C3 |

The metal bottom of the case must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Electrical Specifications: $T_A = -55^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ ¹

| Parameter | Test Conditions | Frequency | Units | Min | Typ | Max |
|-----------------------------------|--|------------------------------|---|------|-----|-------|
| Reference Insertion Loss | — | DC - 0.5 GHz | dB | — | — | 1.7 |
| | | DC - 1.0 GHz | dB | — | — | 1.9 |
| | | DC - 2.0 GHz | dB | — | — | 2.2 |
| | | DC - 3.0 GHz | dB | — | — | 2.5 |
| Attenuation Accuracy ² | Any Single Bit | DC - 2.0 GHz DC - 3.0 GHz | $\pm (0.15 \text{ dB} + 3\% \text{ of atten setting in dB}) \text{ dB}$ $\pm (0.2 \text{ dB} + 3\% \text{ of atten setting in dB}) \text{ dB}$ Or $\pm 0.4 \text{ dB}$, whichever is greater | | | |
| | Any Combination of Bits | DC - 2.0 GHz DC - 3.0 GHz | $\pm (0.2 \text{ dB} + 3\% \text{ of atten setting in dB}) \text{ dB}$ $\pm (0.2 \text{ dB} + 3\% \text{ of atten setting in dB}) \text{ dB}$ Or $\pm 0.4 \text{ dB}$, whichever is greater | | | |
| VSWR | — | — | Ratio | — | — | 1.6:1 |
| Trise, Tfall | 10% to 90% | — | ns | — | 9 | — |
| Ton, Toff | 50% Control to 90/10% RF | — | ns | — | 40 | — |
| Transients | In-Band (peak-peak) | — | mV | — | 30 | — |
| 1 dB Compression | Input Power Input Power | 0.05 GHz | dBm | — | +22 | — |
| | | 0.5 - 3.0 GHz | dBm | — | +28 | — |
| Input IP3 | For two-tone Input Power Up to +5 dBm | 0.05 GHz | dBm | — | +40 | — |
| | | 0.5 - 3.0 GHz | dBm | — | +50 | — |
| Input IP2 | For two-tone Input Power Up to +5 dBm | 0.05 GHz | dBm | — | +45 | — |
| | | 0.5 - 3.0 GHz | dBm | — | +68 | — |
| Vcc | — | — | V | 4.5 | 5.0 | 5.5 |
| Vee | — | — | V | -8.0 | — | -5.0 |
| Icc | Vcc = 4.5 to 5.5V Vctl = 0 to 0.8V, or Vcc – 2.1V to Vcc | — | mA | — | — | 4.0 |
| Iee | Vee = -5.0 to -8.0V | — | mA | — | — | 1.0 |
| Vctl Vctl | Logic 0 (TTL) Logic 1 (TTL) | — | V | 0.0 | — | 0.8 |
| | | — | V | 2.0 | — | 5.0 |
| Input Leakage Current (Low) | 0 to 0.8V | — | μA | — | — | 1.0 |
| Input Leakage Current (High) | 2.0 to 5.0V | — | μA | — | — | 1.0 |

1. All specifications apply when operated with bias voltages of +5V for Vcc and –5.0V for Vee.
2. This attenuator is guaranteed monotonic.

Absolute Maximum Ratings ^{3,4}

| Parameter | Absolute Maximum |
|---|---|
| Max Input Power 0.5 GHz 0.5 - 3.0 GHz | +27 dBm +34 dBm |
| V_{CC} | $-0.5V \leq V_{CC} \leq +7.0V$ |
| V_{EE} | $-8.5V \leq V_{EE} \leq +0.5V$ |
| $V_{CC} - V_{EE}$ | $-0.5V \leq V_{CC} - V_{EE} \leq 14.5V$ |
| V_{in}^5 | $-0.5V \leq V_{in} \leq V_{CC} + 0.5V$ |
| Operating Temperature | $-55^{\circ}C$ to $+125^{\circ}C$ |
| Storage Temperature | $-65^{\circ}C$ to $+150^{\circ}C$ |

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.
- Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

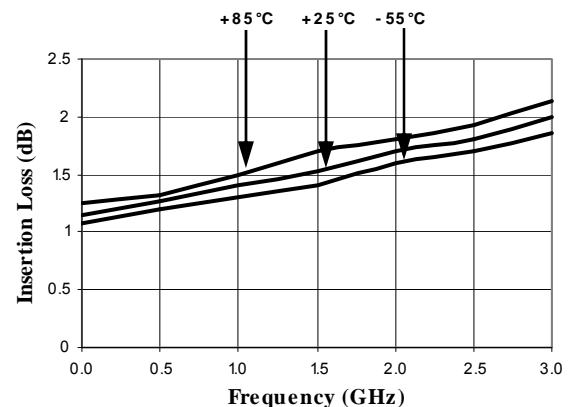
Truth Table (Digital Attenuator)

| Control Inputs | | | | |
|----------------|----|----|----|-------------|
| C4 | C3 | C2 | C1 | Attenuation |
| 0 | 0 | 0 | 0 | Reference |
| 0 | 0 | 0 | 1 | 1 dB |
| 0 | 0 | 1 | 0 | 2 dB |
| 0 | 1 | 0 | 0 | 4 dB |
| 1 | 0 | 0 | 0 | 8 dB |
| 1 | 1 | 1 | 1 | 15 dB |

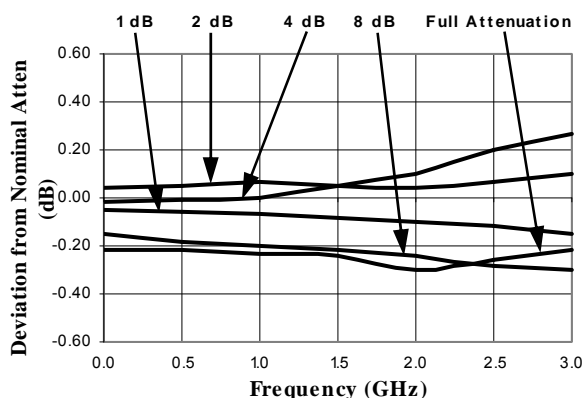
0 = TTL Low; 1 = TTL High

Typical Performance Curves

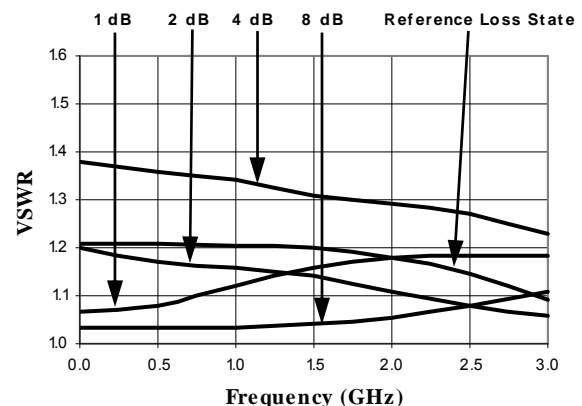
Ref. Insertion Loss vs. Frequency



Attenuation Accuracy vs. Frequency



RF1 VSWR vs. Frequency



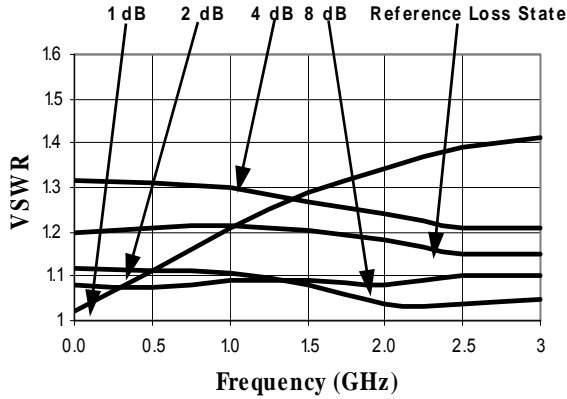
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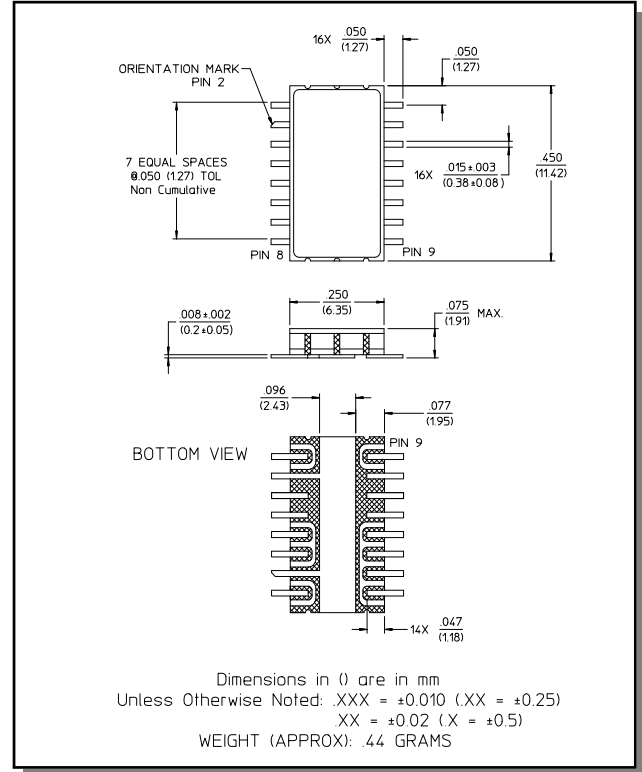
Rev. V5

Typical Performance Curves

RF2 VSWR vs. Frequency



Lead-Free, CR-11 Ceramic Package[†]



[†] Reference Application Note M538 for lead-free solder reflow recommendations.

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