Z86E33/733/E34
Z86E43/743/E44

CMOS Z8® OTP Microcontrollers

Product Specification

PS022901-0508

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Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page No
May 2008	01	Original issue.	All

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Architectural Overview

Zilog's Z86E33/733/E34, E43/743/E44 8-Bit One-Time Programmable (OTP) Microcontrollers are members of Zilog's single-chip Z8® MCU family featuring enhanced wake-up circuitry, programmable Watchdog Timers, Low Noise EMI options, and easy hardware/software system expansion capability.

Four basic address spaces support a wide range of memory configurations. The designer has access to three additional control registers that allow easy access to register mapped peripheral and I/O circuits.

For applications demanding powerful I/O capabilities, the Z86E33/733/E34 have 24 pins, and the Z86E43/743/E44 have 32 pins of dedicated input and output. These lines are grouped into four ports, eight lines per port, and are configurable under software control to provide timing, status signals, and parallel I/O with or without handshake, and address/data bus for interfacing external memory.

Note: *All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and $\overline{B}$/W, for which BYTE is active Low.*

Power connections follow these conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Features

Table 1 lists the features of Z86E33/733/E34, E43/743/E44.

Table 1. Z86E33/733/E34, E43/743/E44 Features

Device	ROM (KB)	RAM[1] (Bytes)	I/O Lines	Speed (MHz)
Z86E33	4	237	24	12
Z86733	8	237	24	12
Z86E34	16	237	24	12
Z86E43	4	236	32	12
Z86743	8	236	32	12

Table 1. Z86E33/733/E34, E43/743/E44 Features (Continued)

Device	ROM (KB)	RAM[1] (Bytes)	I/O Lines	Speed (MHz)
Z86E44	16	236	32	12

[1]General-Purpose

- Standard Temperature (V_{CC} = 3.5 V to 5.5 V)
- Extended Temperature (V_{CC} = 3.5 V to 5.5 V)
- Available Packages:
  - 28-Pin DIP/SOIC/PLCC OTP (E33/733/E34)
  - 40-Pin DIP OTP (E43/743/E44)
  - 44-Pin PLCC/LQFP OTP (E43/743/E44)
- Software Enabled Watchdog Timer (WDT)
- Push-Pull/Open-Drain Programmable on Port 0, Port 1, and Port 2
- 24/32 Input/Output Lines
- Clock-Free WDT Reset
- Auto Power-On Reset (POR)
- Programmable OTP Options:
  - RC Oscillator
  - EPROM Protect
  - Auto Latch Disable
  - Permanently Enabled WDT
  - Crystal Oscillator Feedback Resistor Disable
  - RAM Protect
- Low-Power Consumption: 60 mW
- Fast Instruction Pointer: 0.75 µs
- Two Standby Modes: STOP and HALT
- Digital Inputs CMOS Levels, Schmitt-Triggered
- Software Programmable Low EMI Mode
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Two Comparators

- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive

Functional Block Diagram

Figure 1 displays the functional block diagram.

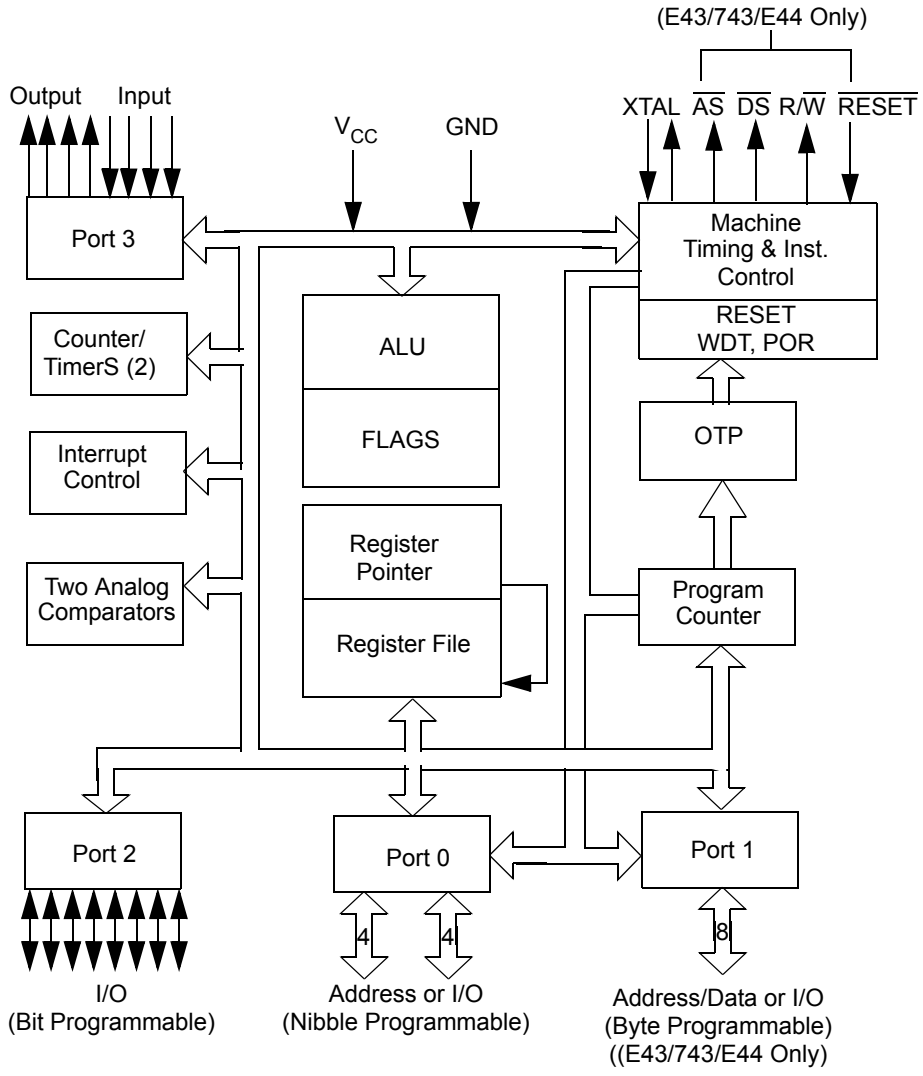


Figure 1. Functional Block Diagram

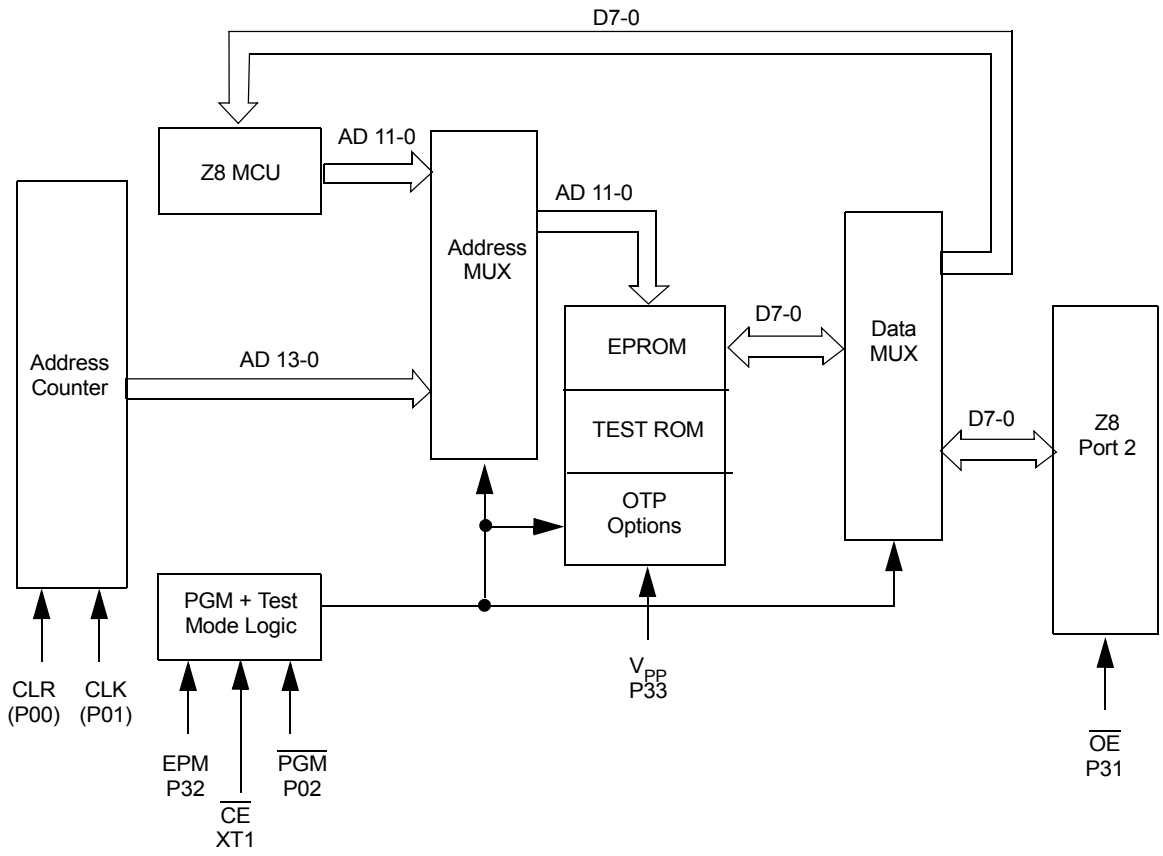


Figure 2. EPROM Programming Block Diagram

Pin Description

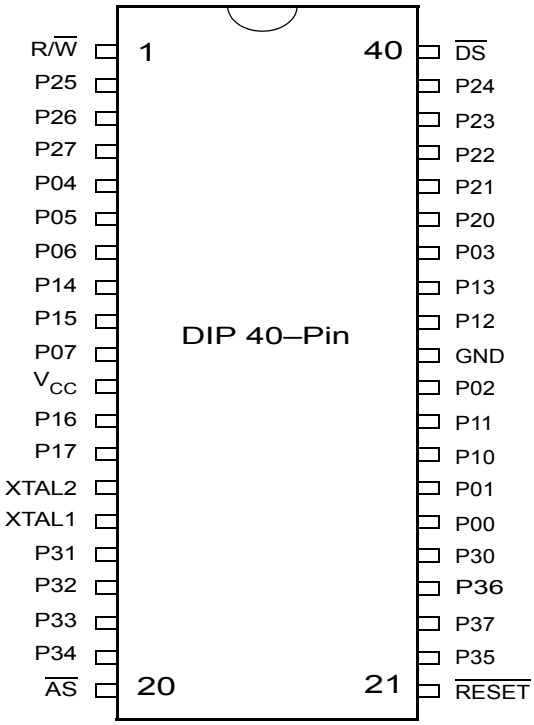


Figure 3. 40-Pin DIP Pin Configuration Standard Mode

Table 2. 40-Pin DIP Pin Identification Standard Mode

Pin No	Symbol	Function	Direction
1	R/$\overline{W}$	Read/Write	Output
2-4	P25-P27	Port 2, Pins 5,6,7	Input/Output
5-7	P04-P06	Port 0, Pins 4,5,6	Input/Output
8-9	P14-P15	Port 1, Pins 4,5	Input/Output
10	P07	Port 0, Pin 7	Input/Output
11	V_{CC}	Power Supply	
12-13	P16-P17	Port 1, Pins 6,7	Input/Output
14	XTAL2	Crystal Oscillator	Output

Table 2. 40-Pin DIP Pin Identification Standard Mode (Continued)

Pin No	Symbol	Function	Direction
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	AS	Address Strobe	Output
21	RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	Input/Output
28-29	P10-P11	Port 1, Pins 0,1	Input/Output
30	P02	Port 0, Pin 2	Input/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	Input/Output
34	P03	Port 0, Pin 3	Input/Output
35-39	P20-P24	Port 2, Pins 0, 1,2,3,4	Input/Output
40	DS	Data Strobe	Output

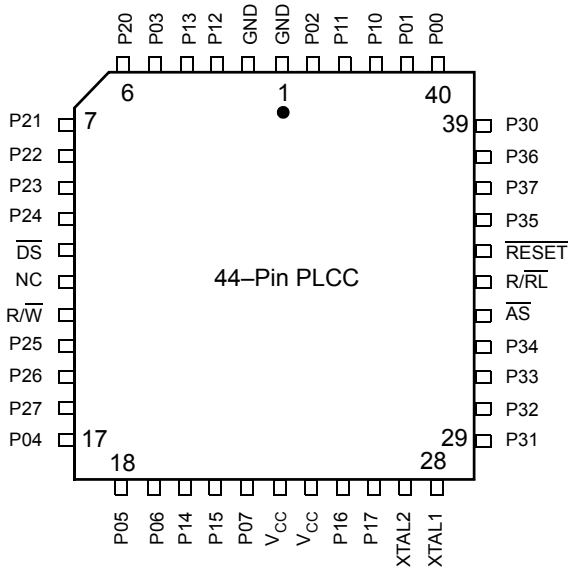


Figure 4. 44-Pin PLCC Pin Configuration Standard Mode

Table 3. 44-Pin PLCC Pin Identification

Pin No	Symbol	Function	Direction
1-2	GND	Ground	
3-4	P12-P13	Port 1, Pins 2,3	Input/Output
5	P03	Port 0, Pin 3	Input/Output
6-10	P20-P24	Port 2, Pins 0,1,2,3,4	Input/Output
11	DS	Data Strobe	Output
12	NC	No Connection	
13	R/$\overline{W}$	Read/Write	Output
14-16	P25-P27	Port 2, Pins 5,6,7	Input/Output
17-19	P04-P06	Port 0, Pins 4,5,6	Input/Output
20-21	P14-P15	Port 1, Pins 4,5	Input/Output
22	P07	Port 0, Pin 7	Input/Output
23-24	V_{CC}	Power Supply	
25-26	P16-P17	Port 1, Pins 6,7	Input/Output

Table 3. 44-Pin PLCC Pin Identification (Continued)

Pin No	Symbol	Function	Direction
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29-31	P31-P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output
33	AS	Address Strobe	Output
34	R//RL	ROM/ROMless select Input	
35	RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40-41	P00-P01	Port 0, Pins 0,1	Input/Output
42-43	P10-P11	Port 1, Pins 0,1	Input/Output
44	P02	Port 0, Pin 2	Input/Output

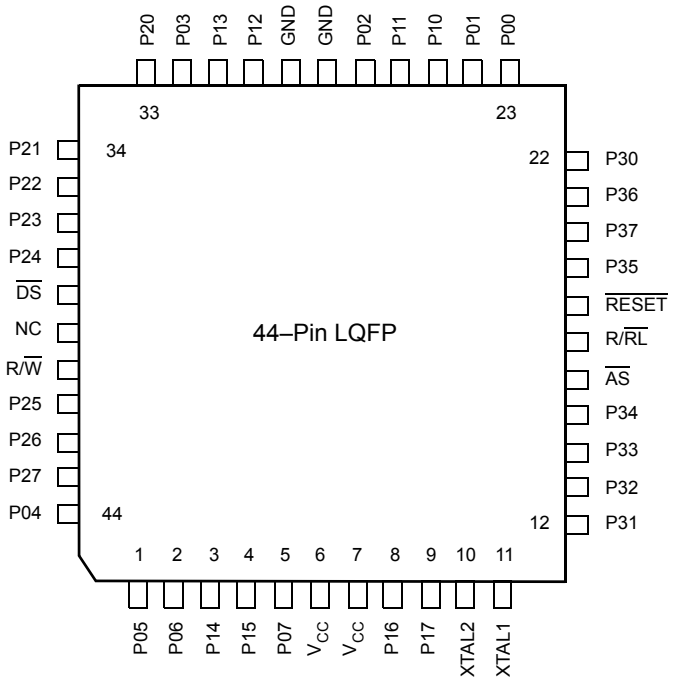


Figure 5. 44-Pin LQFP Pin Configuration Standard Mode

Table 4. 44-Pin LQFP Pin Identification

Pin No	Symbol	Function	Direction
1-2	P05-P06	Port 0, Pins 5,6	Input/Output
3-4	P14-P15	Port 1, Pins 4,5	Input/Output
5	P07	Port 0, Pin 7	Input/Output
6-7	V_{CC}	Power Supply	
8-9	P16-P17	Port 1, Pins 6,7	Input/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12-14	P31-P33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	AS	Address Strobe	Output
17	R//RL	ROM/ROMless select	Input

Table 4. 44-Pin LQFP Pin Identification (Continued)

Pin No	Symbol	Function	Direction
18	RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23-24	P00-P01	Port 0, Pin 0,1	Input/Output
25-26	P10-P11	Port 1, Pins 0,1	Input/Output
27	P02	Port 0, Pin 2	Input/Output
28-29	GND	Ground	
30-31	P12-P13	Port 1, Pins 2,3	Input/Output
32	P03	Port 0, Pin 3	Input/Output
33-37	P20-24	Port 2, Pins 0,1,2,3,4	Input/Output
38	DS	Data Strobe	Output
39	NC	No Connection	
40	R/$\overline{W}$	Read/Write	Output
41-43	P25-P27	Port 2, Pins 5,6,7	Input/Output
44	P04	Port 0, Pin 4	Input/Output

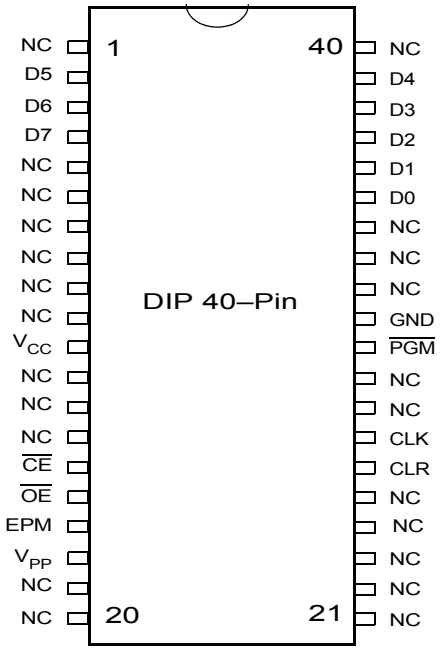


Figure 6. 40-Pin DIP Pin Configuration EPROM Mode

Table 5. 40-Pin DIP Package Pin Identification EPROM Mode

Pin No	Symbol	Function	Direction
1	NC	No Connection	
2-4	D5-D7	Data 5,6,7	Input/Output
5-10	NC	No Connection	
11	V_{CC}	Power Supply	
12-14	NC	No Connection	
15	CE	Chip Select	Input
16	OE	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	V_{PP}	Prog. Voltage	Input
19-25	NC	No Connection	
26	CLR	Clear	Input
27	CLK	Clock	Input
28-29	NC	No Connection	

Table 5. 40-Pin DIP Package Pin Identification EPROM Mode (Continued)

Pin No	Symbol	Function	Direction
30	/PGM	Prog. Mode	Input
31	GND	Ground	
32-34	NC	No Connection	
35-39	D0-D4	Data 0,1,2,3,4	Input/Output
40	NC	No Connection	

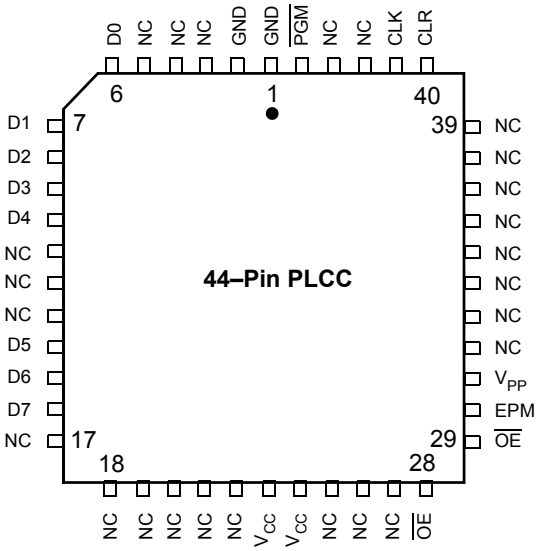


Figure 7. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Pin No	Symbol	Function	Direction
1-2	GND	Ground	
3-5	NC	No Connection	
6-10	D0-D4	Data 0,1,2,3,4	Input/Output
11-13	NC	No Connection	
14-16	D5-D7	Data 5,6,7	Input/Output
17-22	NC	No Connection	
23-24	V_{CC}	Power Supply	
25-27	NC	No Connection	
28	CE	Chip Select	Input
29	OE	Output Enable	Input
30	EPM	EPROM Prog. Mode	Input
31	V_{PP}	Prog. Voltage	Input

Table 6. 44-Pin PLCC Pin Configuration EPROM Programming Mode (Continued)

Pin No	Symbol	Function	Direction
32-39	NC	No Connection	
40	CLR	Clear	Input
41	CLK	Clock	Input
42-43	NC	No Connection	
44	/PGM	Prog. Mode	Input

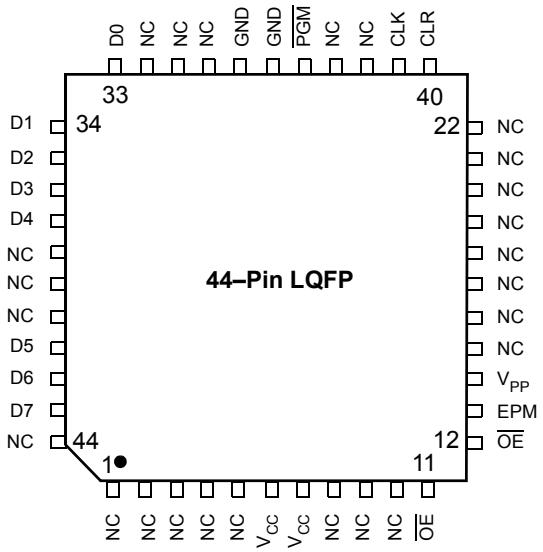


Figure 8. 44-Pin LQFP Pin Configuration EPROM Programming Mode

Table 7. 44-Pin LQFP Pin Identification EPROM Programming Mode

Pin No	Symbol	Function	Direction
1-5	NC	No Connection	
6-7	V_{CC}	Power Supply	
8-10	NC	No Connection	
11	CE	Chip Select	Input
12	OE	Output Enable	Input
13	EPM	EPROM Prog. Mode	Input
14	V_{PP}	Prog. Voltage	Input
15-22	NC	No Connection	
23	CLR	Clear	Input
24	CLK	Clock	Input
25-26	NC	No Connection	
27	/PGM	Prog. Mode	Input
28-29	GND	Ground	
30-32	NC	No Connection	

Table 7. 44-Pin LQFP Pin Identification EPROM Programming Mode (Continued)

Pin No	Symbol	Function	Direction
33-37	D0-D4	Data 0,1,2,3,4	Input/Output
38-40	NC	No Connection	
41-43	D5-D7	Data 5,6,7	Input/Output
44	NC	No Connection	

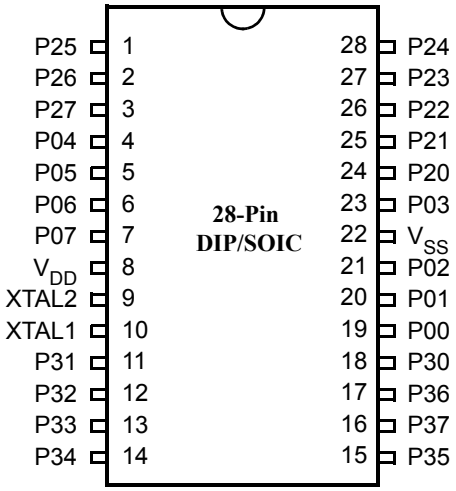


Figure 9. Standard Mode 28-Pin DIP/SOIC Pin Configuration

Table 8. 28-Pin DIP/SOIC/PLCC Pin Identification Standard Mode

Pin No	Symbol	Function	Direction
1-3	P25-P27	Port 2, Pins 5,6,	Input/Output
4-7	P04-P07	Port 0, Pins 4,5,6,7 In/Output	
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-P33	Port 3, Pins 1,2,3	Input
14-15	P34-P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19-21	P00-P02	Port 0, Pins 0,1,2	Input/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	Input/Output
24-28	P20-P24	Port 2, Pins 0,1,2,3,4	Input/Output

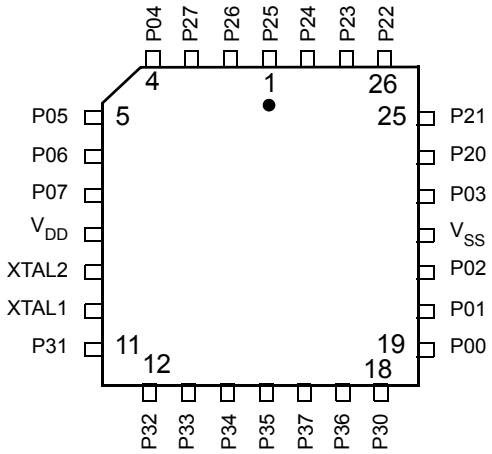


Figure 10. Standard Mode 28-Pin PLCC Pin Configuration

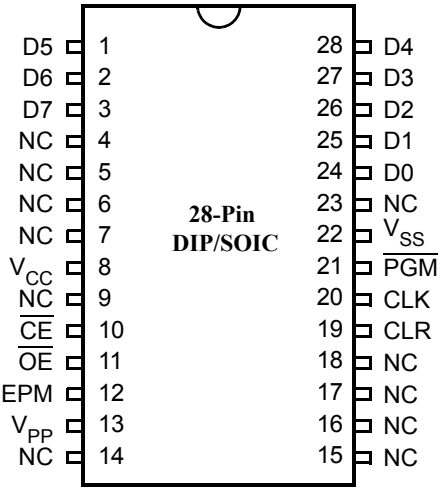


Figure 11. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration

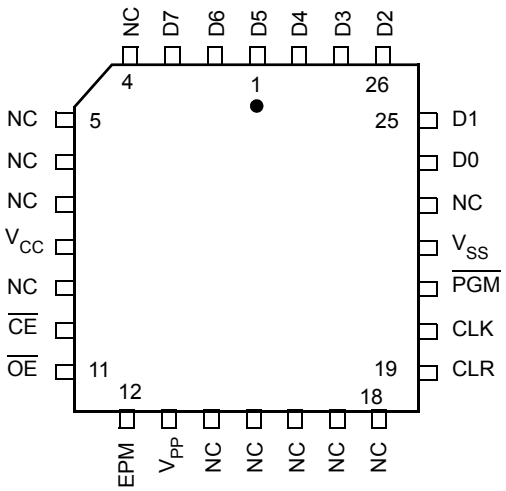


Figure 12. EPROM Programming Mode 28-Pin PLCC Pin Configuration

Table 9. 28-Pin EPROM Pin Identification EPROM Mode

Pin #	Symbol	Function	Direction
1-3	D5-D7	Data 5,6,7	Input/Output
4-7	NC	No Connection	
8	V_{CC}	Power Supply	
9	NC	No connection	
10	CE	Chip Select	Input
11	OE	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V_{PP}	Prog. Voltage	Input
14-18	NC	No Connection	
19	CLR	Clear	
20	CLK	Clock	
21	/PGM	Prog. Mode	Input
22	V_{SS}	Ground	
23	NC	No Connection	
24-28	D0-D4	Data 0,1,2,3,4	Input/Output

Electrical Characteristics

Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on XTAL1, P32, P33 and $\overline{\text{RESET}}$ Pins with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		1.21	W	
Maximum Allowable Current out of V_{SS}		220	mA	
Maximum Allowable Current into V_{DD}		180	mA	
Maximum Allowable Current into an Input Pin	–600	+600	µA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by $\overline{\text{RESET}}$ Pin		3	mA	

Notes
1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH}), + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$$

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load).

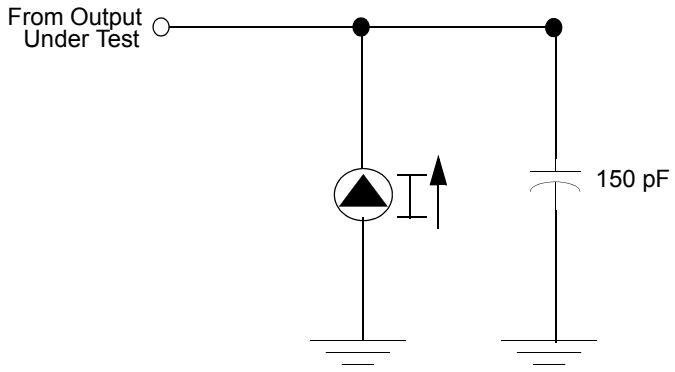


Figure 13. Test Load Diagram

Capacitance

T_A = 25 °C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC Electrical Characteristics

Table 11. DC Electrical Characteristics T_A = 0 °C to +70 °C

Symbol	Parameter	V_{CC}[1]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	0.7 V_{CC}	V_{CC} +0.3	1.8	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC} +0.3	2.5	V		
V_{CL}	Clock Input Low Voltage	3.5V	GND -0.3	0.2 V_{CC}	0.9	V	Driven by External Clock Generator	
		5.5V	GND -0.3	0.2 V_{CC}	1.5	V		
V_{IH}	Input High Voltage	3.5V	0.7 V_{CC}	V_{CC} +0.3	2.5	V		
		5.5V	0.7 V_{CC}	V_{CC} +0.3	2.5	V		
V_{IL}	Input Low Voltage	3.5V	GND -0.3	0.2 V_{CC}	1.5	V		
		5.5V	GND -0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage Low EMI Mode	3.5V	V_{CC} -0.4		3.3		I_{OH} = -0.5 mA	
		5.5V	V_{CC} -0.4		4.8			
V_{OH1}	Output High Voltage	3.5V	V_{CC} -0.4		3.3	V	I_{OH} = -2.0 mA	
		5.5V	V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	
V_{OL}	Output Low Voltage Low EMI Mode	3.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
		5.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	3.5V		0.4	0.1	V	I_{OL} = +4.0 mA	2
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	2
V_{OL2}	Output Low Voltage	3.5V		1.2	0.5	V	I_{OL} = +10 mA	2
		5.5V		1.2	0.5	V	I_{OL} = +10 mA	2
V_{RH}	Reset Input High Voltage	3.5V	.8 V_{CC}	V_{CC}	1.7	V		3
		5.5V	.8 V_{CC}	V_{CC}	2.1	V		3
V_{RL}	Reset Input Low Voltage	3.5V	GND -0.3	0.2 V_{CC}	1.3	V		3
		5.5V	GND -0.3	0.2 V_{CC}	1.7	V		3
V_{OLR}	Reset Output Low Voltage	3.5V		0.6	0.3	V	I_{OL} = 1.0 mA	3
		5.5V		0.6	0.2	V	I_{OL} = 1.0 mA	3

Table 11. DC Electrical Characteristics T_A = 0 °C to +70 °C (Continued)

Symbol	Parameter	V_{CC}[1]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{OFFSET}	Comparator Input Offset Voltage	3.5V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	3.5V	0	V_{CC} -1.0V		V		4
		5.5V	0	V_{CC} -1.0V		V		4
I_{IL}	Input Leakage	3.5V	-1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	-1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V	-20	-130	-65	µA		
		5.5V	-20	-180	-112	µA		
I_{CC}	Supply Current	3.5V		15	5	mA	@ 12 MHz	5,6
		5.5V		20	15	mA	@ 12 MHz	5,6
I_{CC1}	Standby Current HALT Mode	3.5V		4	2	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	5,6
		5.5V		6	4	mA		5,6
		3.5V		3	1.5	mA	Clock Divide by 16 @ 12 MHz	5,6
		5.5V		5	3	mA		5,6
I_{CC2}	Standby Current STOP Mode	3.5V		10	2	µA	V_{IN} = 0V, V_{CC}	7,8,9
		5.5V		10	3	µA	V_{IN} = 0V, V_{CC}	7,8,9
		3.5V		15	7	µA	V_{IN} = 0V, V_{CC}	7,8
		5.5V		30	10	µA	V_{IN} = 0V, V_{CC}	7,8
I_{ALL}	Auto Latch Low Current	3.0V	0.7	8	2.4	µA	0V < V_{IN} < V_{CC}	10
		5.5V	1.4	15	4.7	µA	0V < V_{IN} < V_{CC}	10
I_{ALH}	Auto Latch High Current	3.5V	-0.6	-5	-1.8	µA	0V < V_{IN} < V_{CC}	10
		5.5V	-1	-8	-3.8	µA	0V < V_{IN} < V_{CC}	10

Table 11. DC Electrical Characteristics T_A = 0 °C to +70 °C (Continued)

Symbol	Parameter	V_{CC}[1]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
T_{POR}	Power-On Reset	3.5V	2.0 ms	24	7	ms		
		5.5V	1.0 ms	13	4	ms		
V_{LV}	Auto Reset Voltage		2.3	3.0	2.8	V		11,12

Notes
1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V
2. STD Mode (not Low EMI Mode)
3. Z86E43/743/E44 only.
4. For analog comparator inputs when analog comparators are enabled
5. All outputs unloaded, I/O pins floating, inputs at rail.
6. CL1=CL2=22 pF.
7. Same as note 5 except inputs at V_{CC}
8. Clock must be forced Low, when XTAL1 is clock driven and XTAL2
9. WDT running
10. Auto Latch (mask option) selected.
11. Device does function down to the Auto Reset voltage
12. Max. temperature is 70 °C

Table 12. DC Electrical Characteristics T_A= -40 °C to +105 °C

Symbol	Parameter	V_{CC}[1]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	0.7 V_{CC}	V_{CC} +0.3	2.5	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC} +0.3	2.5	V		
V_{CL}	Clock Input Low Voltage	4.5V	GND -0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
		5.5V	GND -0.3	0.2 V_{CC}	1.5	V		
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC} +0.3	2.5	V		
		5.5V	0.7 V_{CC}	V_{CC} +0.3	2.5	V		
V_{IL}	Input Low Voltage	4.5V	GND -0.3	0.2 V_{CC}	1.5	V		
		5.5V	GND -0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage Low EMI Mode	4.5V	V_{CC} -0.4		4.8		I_{OH} = -0.5 mA	2
		5.5V	V_{CC} -0.4		4.8		I_{OH} = -0.5 mA	2

Table 12. DC Electrical Characteristics T_A= -40 °C to +105 °C (Continued)

Symbol	Parameter	V_{CC} [1]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{OH1}	Output High Voltage	4.5V	V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	2
		5.5V	V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	2
V_{OL}	Output Low Voltage Low EMI Mode	4.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
		5.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	2
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	2
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL} = +12 mA	2
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	2
V_{RH}	Reset Input High Voltage	4.5V	.8 V_{CC}	V_{CC}	1.7	V		3
		5.5V	.8 V_{CC}	V_{CC}	2.1	V		3
V_{OLR}	Reset Output Low Voltage	4.5V		0.6	0.3	V	I_{OL} = 1.0 mA	3
		5.5V		0.6	0.2	V	I_{OL} = 1.0 mA	3
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	4.5V	0	V_{CC} -1.5V		V		4
		5.5V	0	V_{CC} -1.5V		V		4
I_{IL}	Input Leakage	4.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	4.5V	-18	-180	-112	µA		3
		5.5V	-18	-180	-112	µA		3
I_{CC}	Supply Current	4.5V		20	15	mA	@ 12 MHz	5,6
		5.5V		20	15	mA	@ 12 MHz	5,6
I_{CC1}	Standby Current HALT Mode	4.5V		6	2	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	5,6
		5.5V		6	4	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	5,6

Table 12. DC Electrical Characteristics T_A= -40 °C to +105 °C (Continued)

Symbol	Parameter	V_{CC} [1]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC2}	Standby Current STOP Mode	4.5V		10	2	µA	V_{IN} = 0V, V_{CC}	7,8,9
		5.5V		10	3	µA	V_{IN} = 0V, V_{CC}	7,8,9
		4.5V		40	10	µA	V_{IN} = 0V, V_{CC}	7,8
		5.5V		40	10	µA	V_{IN} = 0V, V_{CC}	7,8
I_{ALL}	Auto Latch Low Current	4.5V	1.4	20	4.7	µA	0V < V_{IN} < V_{CC}	10
		5.5V	1.4	20	4.7	µA	0V < V_{IN} < V_{CC}	10
I_{ALH}	Auto Latch High Current	4.5V	-1.0	-10	-3.8	µA	0V < V_{IN} < V_{CC}	10
		5.5V	-1.0	-10	-3.8	µA	0V < V_{IN} < V_{CC}	10
T_{POR}	Power-On Reset	4.5V	1.0	14	4	ms		
		5.5V	1.0	14	4	ms		
V_{LV}	Auto Reset Voltage		2.0	3.3	2.8	V		11

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. STD Mode (not Low EMI Mode).
3. Z86E43/743/E44 only.
4. For analog comparator inputs when analog comparators are enabled.
5. All outputs unloaded, I/O pins floating, inputs at rail.
6. CL1=CL2=22 pF.
7. Same as note 5 except inputs at V_{CC}.
8. Clock must be forced Low, when XTAL1 is clock driven and XTAL2.
9. WDT is not running.
10. Auto Latch (mask option) selected.
11. Device does function down to the Auto Reset voltage.

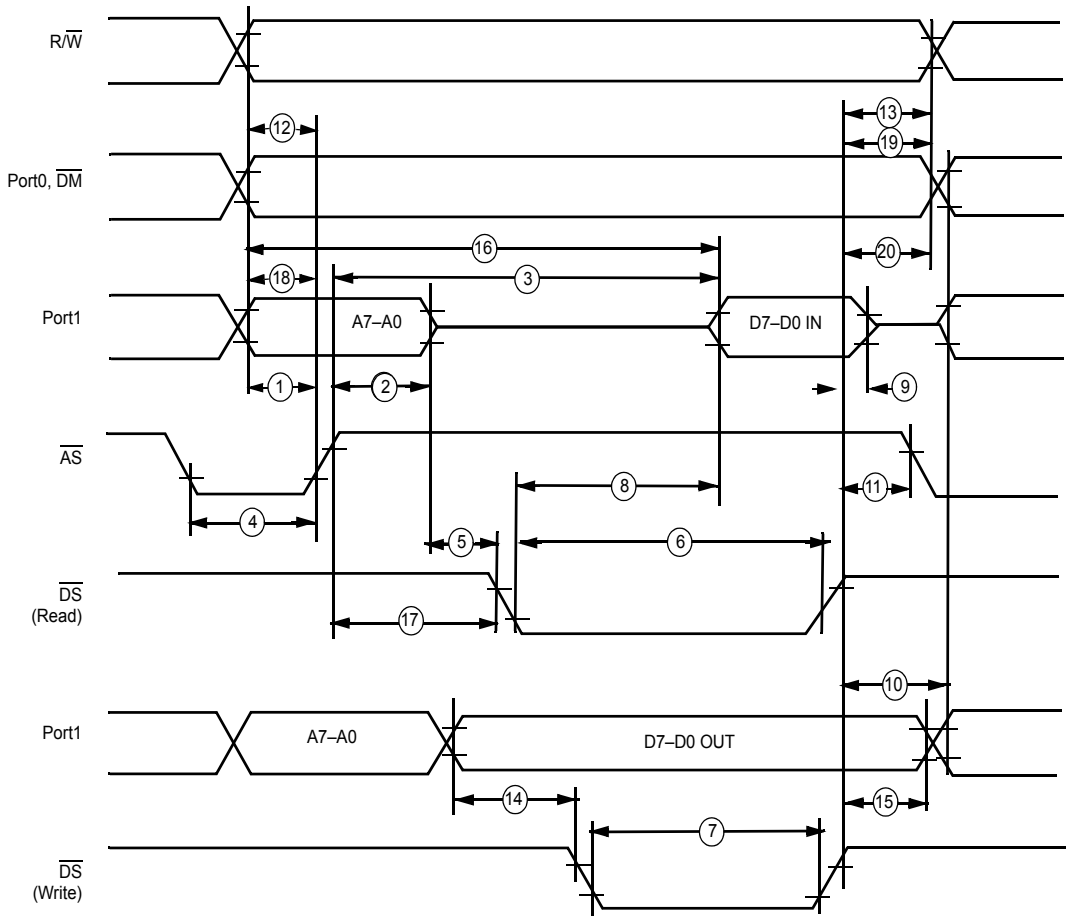


Figure 14. External I/O or Memory Read/Write Timing (Z86E43/743/E44 Only)

Table 13. DC Electrical Characteristics T_A = 0 °C to +70 °C, 12 MHz

No.	Symbol	Parameter	V_{CC} [1]	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	3.5V	35		ns	2
			5.5V	35		ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	3.5V	45		ns	2
			5.5V	45		ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	3.5V		250	ns	2,3
			5.5V		250	ns	2,3

Table 13. DC Electrical Characteristics T_A = 0 °C to +70 °C, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC} [1]	Min	Max	Units	Notes
4	TwAS	$\overline{AS}$ Low Width	3.5V	55		ns	2
			5.5V	55		ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	3.5V	0		ns	
			5.5V	0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	3.5V	200		ns	2,3
			5.5V	200		ns	2,3
7	TwDSW	$\overline{DS}$ (Write) Low Width	3.5V	110		ns	2,3
			5.5V	110		ns	2,3
8	TdDSR(DR)	$\overline{DS}$ Fail to Read Data Req'd Valid	3.5V		150	ns	2,3
			5.5V		150	ns	2,3
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	3.5V	0		ns	2
			5.5V	0		ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	3.5V	45		ns	2
			5.5V	55		ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	3.5V	30		ns	2
			5.5V	45		ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	3.5V	45		ns	2
			5.5V	45		ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	3.5V	45		ns	2
			5.5V	45		ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	3.5V	55		ns	2
			5.5V	55		ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	3.5V	45		ns	2
			5.5V	55		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.5V		310	ns	2,3
			5.5V		310	ns	2,3
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	3.5V	65		ns	2
			5.5V	65		ns	2

Table 13. DC Electrical Characteristics T_A = 0 °C to +70 °C, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC} [1]	Min	Max	Units	Notes
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Rise Delay	3.5V	35		ns	2
			5.5V	35		ns	2
19	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	3.5V	35		ns	2
			5.5V	35		ns	2

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing numbers given are for minimum TpC.
3. When using extended memory timing, add 2 TpC

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

Table 14. DC Electrical Characteristics T_A = -40 °C to +105 °C, 12 MHz

No.	Symbol	Parameter	V_{CC} [1]	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	4.5V	35		ns	2
			5.5V	35		ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	4.5V	45		ns	2
			5.5V	45		ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	4.5V		250	ns	2,3
			5.5V		250	ns	2,3
4	TwAS	$\overline{AS}$ Low Width	4.5V	55		ns	2
			5.5V	55		ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	4.5V	0		ns	
			5.5V	0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	4.5V	200		ns	2,3
			5.5V	200		ns	2,3
7	TwDSW	$\overline{DS}$ (Write) Low Width	4.5V	110		ns	2,3
			5.5V	110		ns	2,3
8	TdDSR(DR)	$\overline{DS}$ Fail to Read Data Req'd Valid	4.5V		150	ns	2,3
			5.5V		150	ns	2,3
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	4.5V	0		ns	2
			5.5V	0		ns	2

Table 14. DC Electrical Characteristics T_A = -40 °C to +105 °C, 12 MHz (Continued)

No.	Symbol	Parameter	V_{CC}[1]	Min	Max	Units	Notes
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	4.5V	45		ns	2
			5.5V	55		ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	4.5V	45		ns	2
			5.5V	45		ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	4.5V	45		ns	2
			5.5V	45		ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	4.5V	45		ns	2
			5.5V	45		ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	4.5V	55		ns	2
			5.5V	55		ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	4.5V	55		ns	2
			5.5V	55		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V		310	ns	2,3
			5.5V		310	ns	2,3
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	4.5V	65		ns	2
			5.5V	65		ns	2
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Rise Delay	4.5V	35		ns	2
			5.5V	35		ns	2
19	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	4.5V	35		ns	2
			5.5V	35		ns	2

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing numbers given are for minimum TpC.
3. When using extended memory timing, add 2 TpC.

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

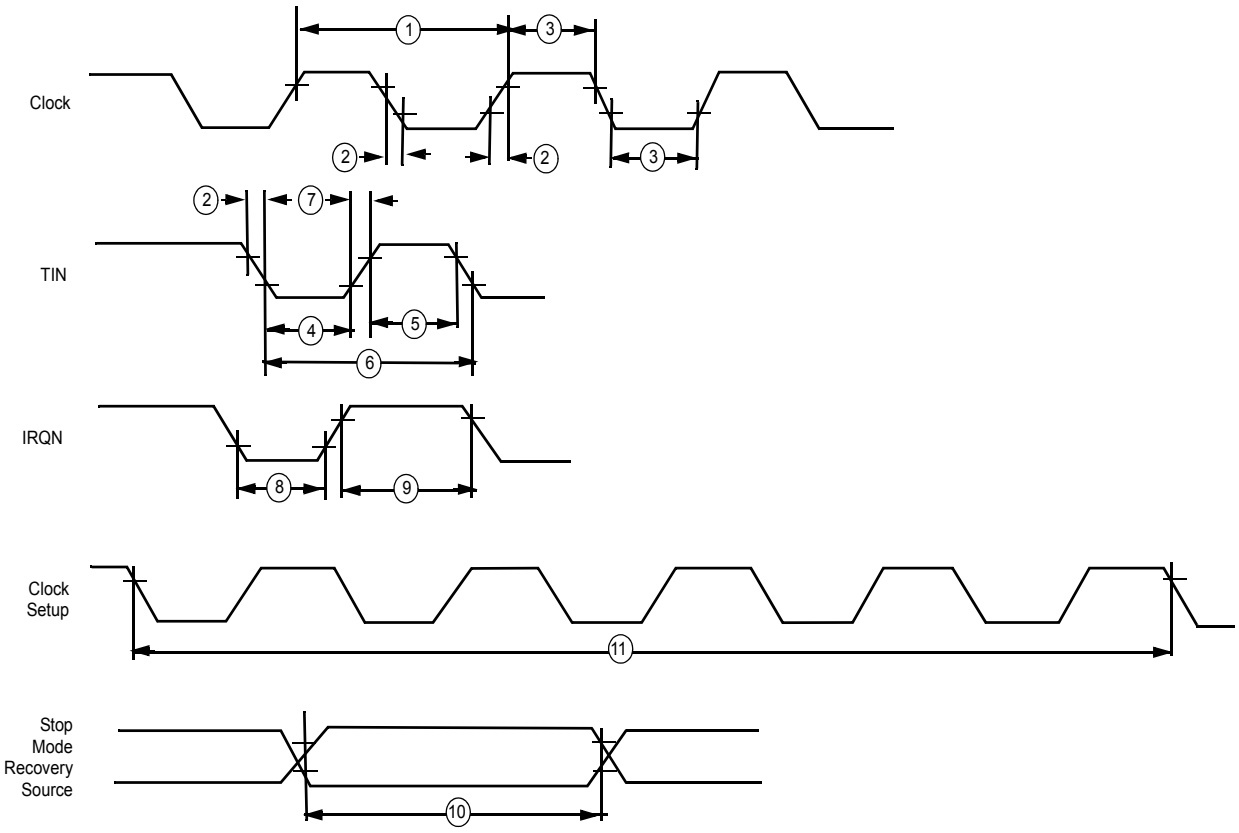


Figure 15. Additional Timing Diagram

Table 15. Additional Timing Table (Divide-By-One Mode) T_A = 0 °C to +70 °C

No	Symbol	Parameter	V_{CC} [1]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V	250	DC	166	DC	ns	2,3,4
			5.5V	250	DC	166	DC	ns	2,3,4
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		25		25	ns	2,3,4
			5.5V		25		25	ns	2,3,4
3	TwC	Input Clock Width	3.5V	100		100		ns	2,3,4
			5.5V	100		100		ns	2,3,4
4	TwTinL	Timer Input Low Width	3.5V	100		100		ns	2,3,4
			5.5V	70		70		ns	2,3,4

Table 15. Additional Timing Table (Divide-By-One Mode) T_A = 0 °C to +70 °C (Continued)

No	Symbol	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Notes
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC			2,3,4
			5.5V	5TpC		5TpC			2,3,4
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			2,3,4
			5.5V	8TpC		8TpC			2,3,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns	2,3,4
			5.5V		100		100	ns	2,3,4
8A	TwIL	Int. Request Low Time	3.5V	100		100		ns	2,3,4,5
			5.5V	70		70		ns	2,3,4,5
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC			2,3,4,6
			5.5V	5TpC		5TpC			2,3,4,6
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC			2,3,4,5
			5.5V	5TpC		5TpC			2,3,4,5
10	Twsm	Stop Mode Recovery Width Spec	3.5V	12		12		ns	4,7
			5.5V	12		12		ns	4,7
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC		4,7,8
			5.5V		5TpC		5TpC		4,7,8

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC}; for a logic 0.
3. SMR D1 = 0.
4. Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7 = 0.
5. Interrupt request via Port 3 (P31-P33).
6. Interrupt request via Port 3 (P30).
7. SMR-D5 = 1, POR STOP Mode Delay is on.
8. For RC and LC oscillator, and for oscillator driven by clock driver.

Table 16. Additional Timing Table (Divide-By-One Mode) T_A = -40 °C to +105 °C

No	Symbol	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	250	DC	166	DC	ns	2,3,4
			5.5V	250	DC	166	DC	ns	2,3,4

Table 16. Additional Timing Table (Divide-By-One Mode) T_A = -40 °C to +105 °C (Continued)

No	Symbol	Parameter	V_{CC} [1]	Min	Max	Min	Max	Units	Notes
2	TrC,TfC	Clock Input Rise & Fall Times	4.5V		25		25	ns	2,3,4
			5.5V		25		25	ns	2,3,4
3	TwC	Input Clock Width	4.5V	100		100		ns	2,3,4
			5.5V	100		100		ns	2,3,4
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	2,3,4
			5.5V	70		70		ns	2,3,4
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			2,3,4
			5.5V	5TpC		5TpC			2,3,4
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			2,3,4
			5.5V	8TpC		8TpC			2,3,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	4.5V		100		100	ns	2,3,4
			5.5V		100		100	ns	2,3,4
8A	TwIL	Int. Request Low Time	4.5V	100		100		ns	2,3,4,5
			5.5V	70		70		ns	2,3,4,5
8B	TwIL	Int. Request Low Time	4.5V	5TpC		5TpC			2,3,4,6
			5.5V	5TpC		5TpC			2,3,4,6
9	TwIH	Int. Request Input High Time	4.5V	5TpC		5TpC			2,3,4,5
			5.5V	5TpC		5TpC			2,3,4,5
10	Twsm	Stop Mode Recovery Width Spec	4.5V	12		12		ns	4,7
			5.5V	12		12		ns	4,7
11	Tost	Oscillator Startup Time	4.5V		5TpC		5TpC		4,7,8
			5.5V		5TpC		5TpC		4,7,8

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC}; for a logic 0.
3. SMR D1 = 0.
4. Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7=0.
5. Interrupt request via Port 3 (P31-P33).
6. Interrupt request via Port 3 (P30).
7. SMR-D5 = 1, POR STOP Mode Delay is on.
8. For RC and LC oscillator, and for oscillator driven by clock driver.

Handshake Timing Diagrams

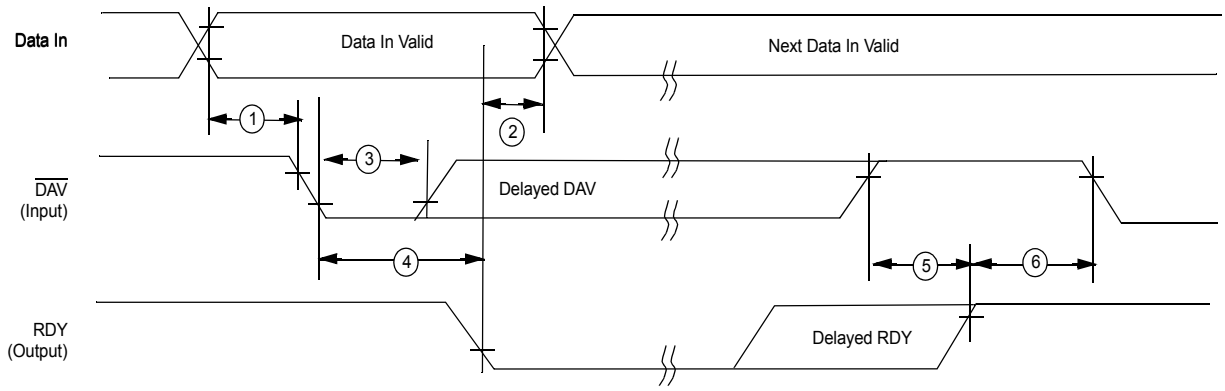


Figure 16. Input Handshake Timing

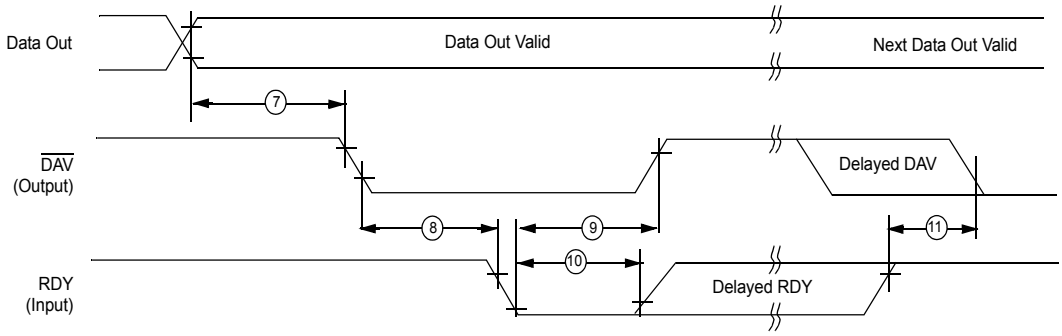


Figure 17. Output Handshake Timing

Table 17. Additional Timing Table (Divide by Two Mode) T_A = 0 °C to +70 °C

No	Symbol	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	250	DC	ns		2,6,4
			5.5V	62.5	DC	250	DC	ns		2,6,4
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15		25	ns		2,6,4
			5.5V		15		25	ns		2,6,4
3	TwC	Input Clock Width	3.5V	31		31		ns		2,6,4
			5.5V	31		31		ns		2,6,4

Table 17. Additional Timing Table (Divide by Two Mode) T_A = 0 °C to +70 °C (Continued)

No	Symbol	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Conditions	Notes
4	TwTinL	Timer Input Low Width	3.5V	70		70		ns		2,6,4
			5.5V	70		70		ns		2,6,4
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC				2,6,4
			5.5V	5TpC		5TpC				2,6,4
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC				2,6,4
			5.5V	8TpC		8TpC				2,6,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns		2,6,4
			5.5V		100		100	ns		2,6,4
8A	TwIL	Int. Request Low Time	3.5V	70		70		ns		2,6,4,5
			5.5V	70		70		ns		2,6,4,5
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
10	Twsm	Stop Mode Recovery Width Spec	3.5V	12		12		ns		6,7
			5.5V	12		12		ns		6,7
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC			6,7
			5.5V		5TpC		5TpC			6,7
12	Twdt	Watchdog Timer Delay Time Before Timeout	3.5V	7		10		ms	D0 =0	8,9
			5.5V	3.5		5		ms	D1 = 0	5,11
			3.5V	14		20		ms	D0 =1	5,11
			5.5V	7		10		ms	D1 = 0	5,11
			3.5V	28		40		ms	D1 = 0	5,11
			5.5V	14		20		ms	D1 = 1	5,11
			3.5V	112		160		ms	D0 = 1	5,11
			5.5V	56		80		ms	D1 = 1	5,11

Notes

1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 VC0 for a logic 1 and 0.2 VGC for a logic 0.
3. SMR D1 = 0.
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Interrupt request via Port 3 (P31-P33)
6. Interrupt request via Port 3 (P30).
7. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0
8. Reg. WDTMR.
9. Using internal RC.

Table 18. Additional Timing Table (Divide by Two Mode) T_A = -40 °C to +105 °C

No	Symbol	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	250	DC	ns		2,6,4
			5.5V	62.5	DC	250	DC	ns		2,6,4
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15		25	ns		2,6,4
			5.5V		15		25	ns		2,6,4
3	TwC	Input Clock Width	3.5V	31		31		ns		2,6,4
			5.5V	31		31		ns		2,6,4
4	TwTinL	Timer Input Low Width	3.5V	70		70		ns		2,6,4
			5.5V	70		70		ns		2,6,4
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC				2,6,4
			5.5V	5TpC		5TpC				2,6,4
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC				2,6,4
			5.5V	8TpC		8TpC				2,6,4
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns		2,6,4
			5.5V		100		100	ns		2,6,4
8A	TwIL	Int. Request Low Time	3.5V	70		70		ns		2,6,4,5
			5.5V	70		70		ns		2,6,4,5
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC				2,6,4,5
			5.5V	5TpC		5TpC				2,6,4,5
10	Twsm	Stop Mode Recovery Width Spec	3.5V	12		12		ns		6,7
			5.5V	12		12		ns		6,7
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC			6,7
			5.5V		5TpC		5TpC			6,7

Table 18. Additional Timing Table (Divide by Two Mode) T_A = -40 °C to +105 °C (Continued)

No	Symbol	Parameter	V_{CC} [1]	Min	Max	Min	Max	Units	Conditions	Notes
12	Twdt	Watchdog Timer Delay Time Before Timeout	3.5V	7		10		ms	D0 =0	8,9
			5.5V	3.5		5		ms	D1 = 0	5,11
			3.5V	14		20		ms	D0 =1	5,11
			5.5V	7		10		ms	D1 = 0	5,11
			3.5V	28		40		ms	D1 = 0	5,11
			5.5V	14		20		ms	D1 = 1	5,11
			3.5V	112		160		ms	D0 = 1	5,11
			5.5V	56		80		ms	D1 = 1	5,11

Notes
1. The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5 V and the V_{CC} voltage specification of 3.5 V guarantees only 3.5 V.
2. Timing Reference uses 0.7 VC0 for a logic 1 and 0.2 VGC for a logic 0.
3. SMR D1 = 0.
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Interrupt request via Port 3 (P31-P33)
6. Interrupt request via Port 3 (P30).
7. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0
8. Reg. WDTMR.
9. Using internal RC.

Pin Functions

EPROM Programming Mode

D7-D0 Data Bus. The data can be read from or written to external memory through the data bus.

V_{CC} Power Supply. This pin must supply 5 V during the EPROM read mode and 6 V during other modes.

$\overline{CE}$ Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

$\overline{OE}$ Output Enable (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Mode by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

PGM Program Mode (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

CLR Clear (active High). This pin resets the internal address counter at the High Level.

CLK Address Clock. This pin is a clock input. The internal address counter increases by one for each clock cycle.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if excessive noise surges above V_{CC} occur on pins P31 and $\overline{\text{RESET}}$.

In addition, processor operation of Z8 OTP devices may be affected by excessive noise surges on the V_{PP}, EPM, $\overline{\text{OE}}$ pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}
- Adding a capacitor to the affected pin
- Enable EPROM/Test Mode Disable OTP option bit.

Standard Mode

XTAL Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network, or external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator output.

R/$\overline{\text{W}}$ Read/Write (output, write Low). The R/$\overline{\text{W}}$ signal is Low when the CCP is writing to the external program or data memory (Z86E43/743/E44 only).

$\overline{\text{RESET}}$ Reset (input, active Low). Reset will initialize the MCU. Reset is accomplished either through Power-On, Watchdog Timer reset, Stop Mode Recovery, or external reset. During Power-On Reset and Watchdog Timer Reset, the internally generated reset drives the reset pin low for the POR time. Any devices driving the reset line must be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. After the POR time, $\overline{\text{RESET}}$ is a Schmitt-triggered input. ($\overline{\text{RESET}}$ is available on Z86E43/743/E44 only.)

To avoid asynchronous and noisy reset problems, the Z86E43/743/E44 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. During the reset cycle, $\overline{\text{DS}}$ is held active Low while $\overline{\text{AS}}$ cycles at a rate of TpC/2. Program execution begins at location 000CH, 5-10 TpC cycles after $\overline{\text{RESET}}$ is released. For Power-On Reset, the reset output time is 5 ms.

The Z86E43/743/E44 does not reset WDTMR, SMR, P2M, and P3M registers on a Stop-Mode Recovery operation.

$\overline{\text{ROMless}}$ (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the device functions nor

Note: *When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.*

$\overline{\text{DS}}$ (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{\text{DS}}$. For WRITE operations, the falling edge of $\overline{\text{DS}}$ indicates that output data is valid.

$\overline{\text{AS}}$ (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{\text{AS}}$. Under program control, $\overline{\text{AS}}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

Port 0 (P07-P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible I/0 port. These eight I/O lines can be configured under software control as a nibble I/0 port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or Al 5-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines Al 5-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include re-configuration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the High-Impedance Mode if selected as an address output state, along with Port 1 and the control signals $\overline{\text{AS}}$, $\overline{\text{DS}}$, and R/$\overline{\text{W}}$ (Figure 18).

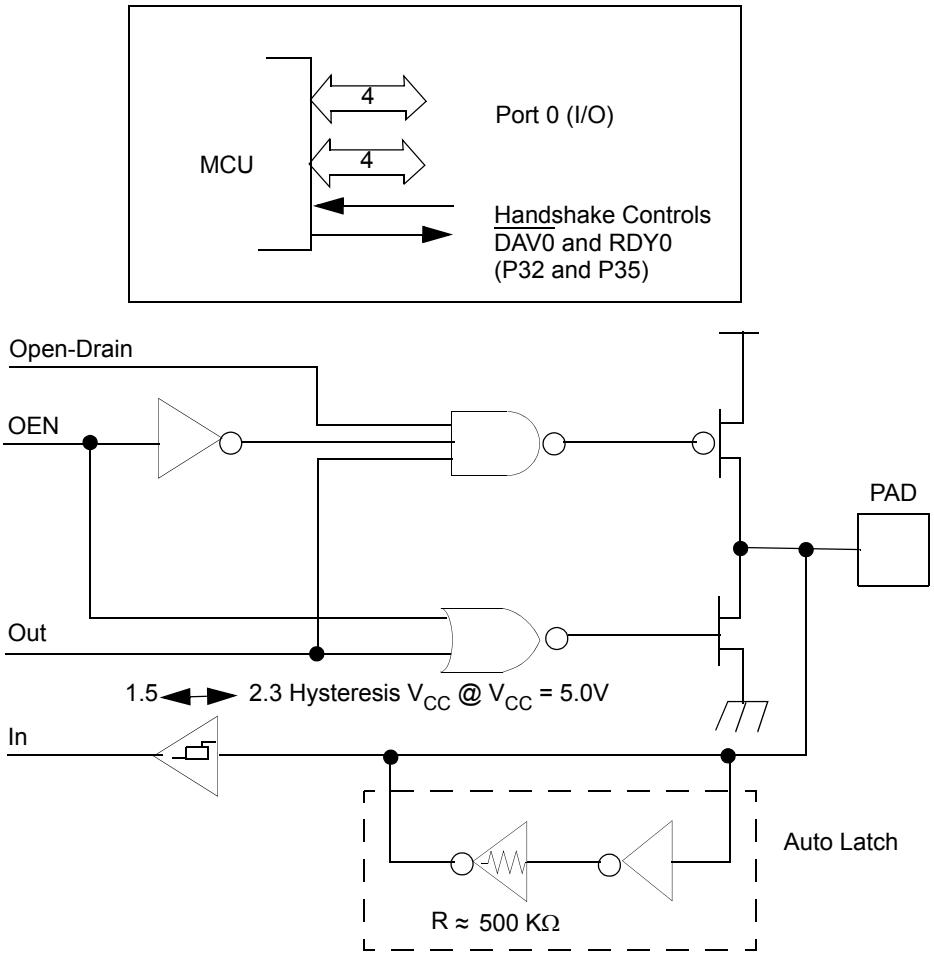


Figure 18. Port 0 Configuration

Port 1 (P17-P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and $\overline{\text{DAV1}}$ (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (see Figure 19).

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z86E43/743/E44 to share common resources in multiprocessor and DMA applications. In ROM mode, Port 1 is defined as input after reset.

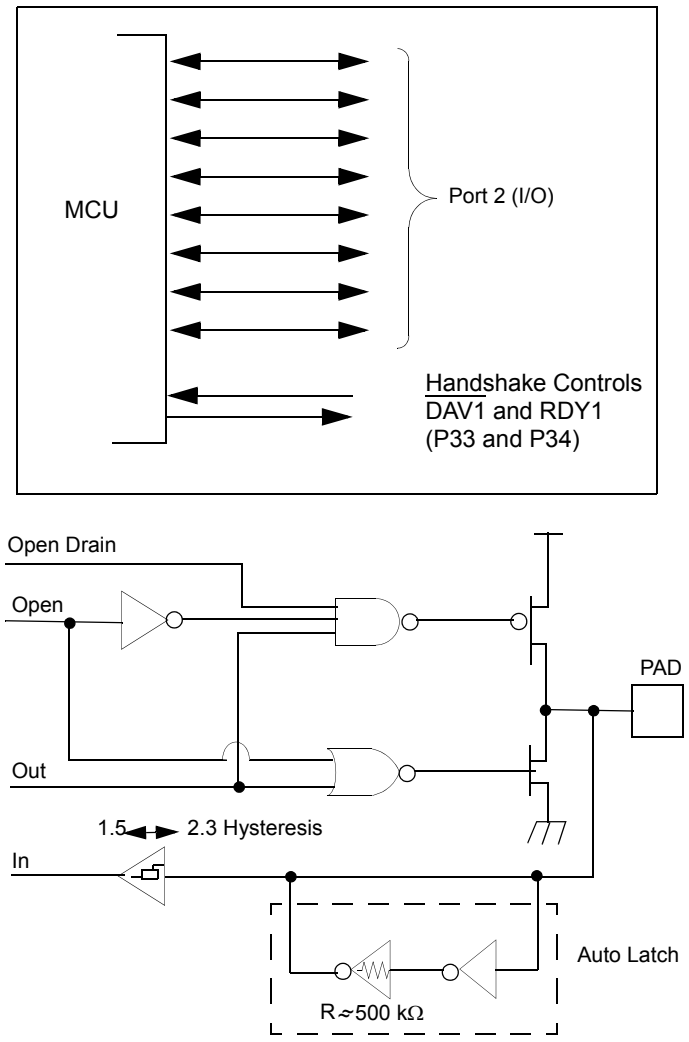


Figure 19. Port 1 Configuration (Z86E43/743/E44 Only)

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control. After reset, Port 2 is defined as an input.

In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (see Figure 20).

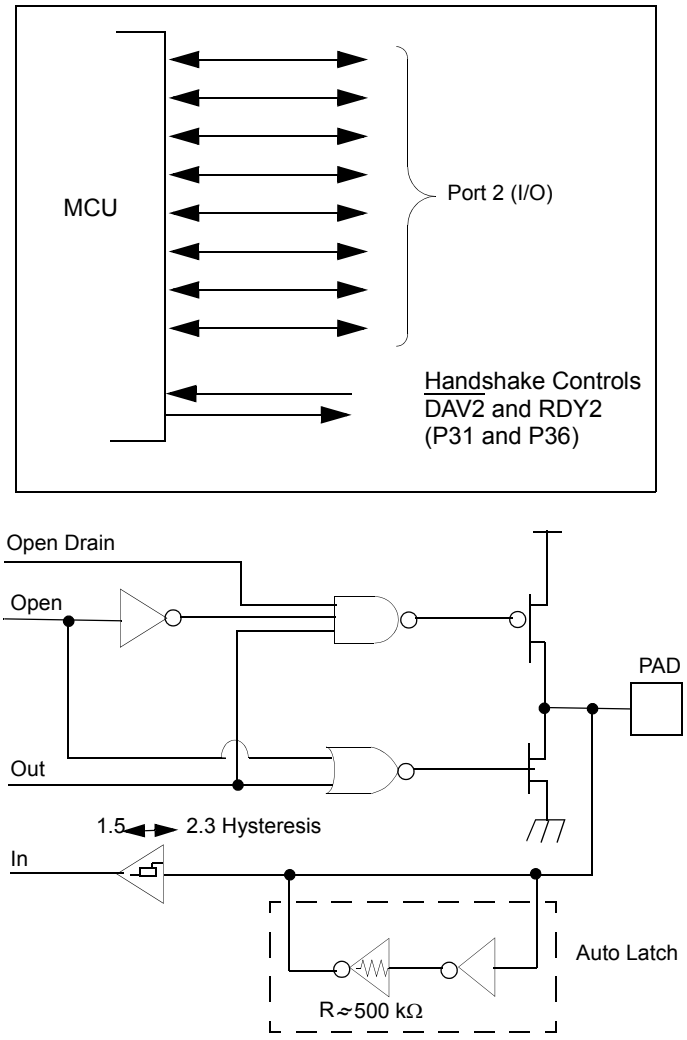


Figure 20. Port 2 Configuration

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS-compatible port with four fixed inputs (P33-P30) and four fixed outputs (P37-P34). These eight lines can be configured by software for interrupt and handshake control functions. Port 3, Pin 0 is Schmitt- triggered. P31, P32, and P33 are standard CMOS inputs with single trip point (no Auto Latches) and P34, P35, P36, and P37 are push-pull output lines. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31

and P32 with reference to the voltage on P33. The analog function is enabled by setting the D1 of Port 3 Mode Register (P3M). The comparator output can be outputted from P34 and P37, respectively, by setting PCON register Bit D0 to 1 state. For the interrupt function, P30 and P33 are falling edge triggered interrupt inputs. P31 and P32 can be programmed as falling, rising or both edges triggered interrupt inputs (see Figure 21). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake tines for Port 0, Port 1, and Port 2 are also available on Port 3 (see Table 19).

Note: *When enabling or disabling analog mode, the following is recommended:*

1. Allow two NOP decays before reading this comparator output.
2. Disable global interrupts, switch to analog mode, clear interrupts, and then re-enable interrupts.
3. IRQ register bits 3 to 0 must be cleared after enabling analog mode.

Note: *P33-P30 differs from the Z86C33/C43/233/243 in that there is no clamping diode to V_{CC} due to the EPROM high-voltage circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode.*

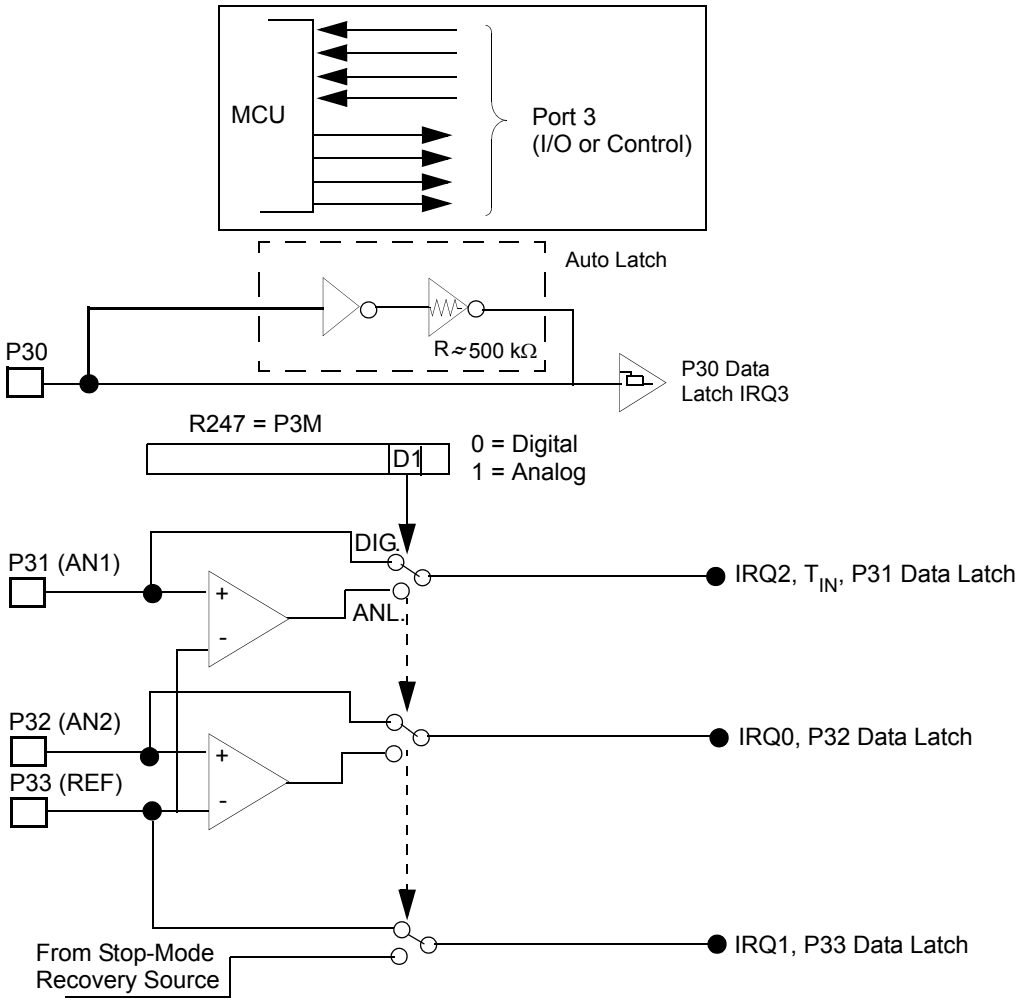


Figure 21. Port 3 Configuration

Table 19. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Interrupt	P0 HS	P1 HS	P2 HS	Ext
P30	IN			IRQ3				
P31	IN	T_{IN}	AN1	IRQ2		D/R		
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT		AN1-Out			R/D		DM
P35	OUT				R/D			
P36	OUT	T_{OUT}				R/D		
P37	OUT		An2-Out					

Comparator Inputs. Port 3, P31, and P32, each have a comparator front end. The comparator reference voltage P33 is common to both comparators. In analog mode, P31 and P32 are the positive input of the comparators and P33 is the reference voltage of the comparators.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33-P31) that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Auto Latches are available on Port 0, Port 1, Port 2, and P30. There are no Auto Latches on P31, P32, and P33.

Low EMI Emission. The Z86E43/743/E44 can be programmed to operate in a low EMI Emission Mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator.
- Internal SCLK/TCLK= XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time, when Low EMI Oscillator is selected.

Note: *For emulation only:*
Do not set the emulator to emulate Port 1 in low EMI mode. Port 1 must always be configured in Standard Mode.

Functional Description

The MCU incorporates the following special functions to enhance the standard Z8 architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of three ways:

1. Power-On Reset
2. Watchdog Timer
3. Stop Mode Recovery Source

Note: *Having the Auto Power-On Reset circuitry built-in, the MCU does not need to be connected to an external power-on reset circuit. The reset time is T_{POR}. The MCU does not re-initialize WDTMR, SMR, P2M, and P3M registers to their reset values on a Stop Mode Recovery operation.*

Note: *The device V_{CC} must rise up to the operating V_{CC} specification before the T_{POR} expires.*

Program Memory. The MCU can address up to 4/8/16 KB of Internal Program Memory (see Figure 22). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000Ch) to address 4095 (0FFFh)/8191 (1FFFh)/16384 (3FFFh), consists of programmable EPROM. After reset, the program counter points at the address 000Ch, which is the starting address of the user program.

In ROMless mode, the Z86E43/743/E44 can address up to 64 KB of External Program Memory. The ROM/ROMless option is only available on the 44-pin devices.

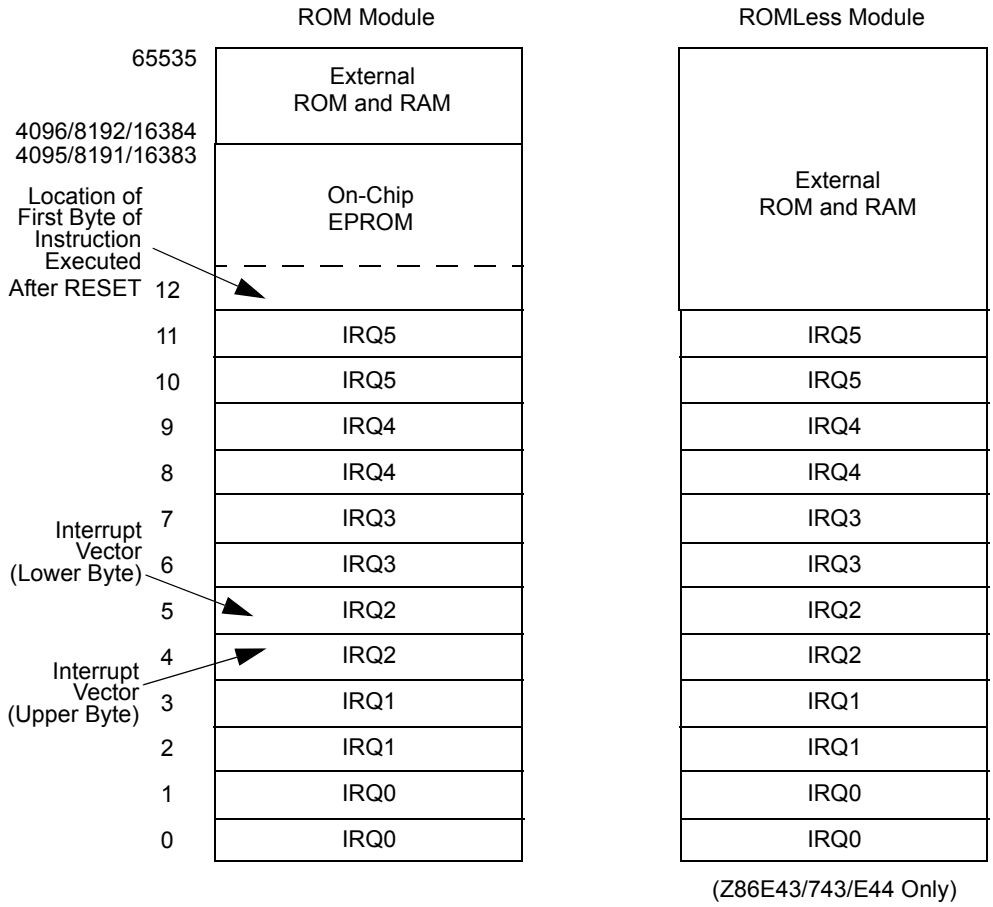


Figure 22. Program Memory Map

EPROM Protect. When in ROM Protect Mode, and executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory.

When in EPROM Protect Mode and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.

Data Memory ($\overline{DM}$). In ROM Mode, the Z86E43/743/E44 can address up to 60156/48 KB of external data memory beginning at location 4096/8192/16384. In ROMless mode, the Z86E43/743/E44 can address up to 64 KB of data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/0 function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 23). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory.

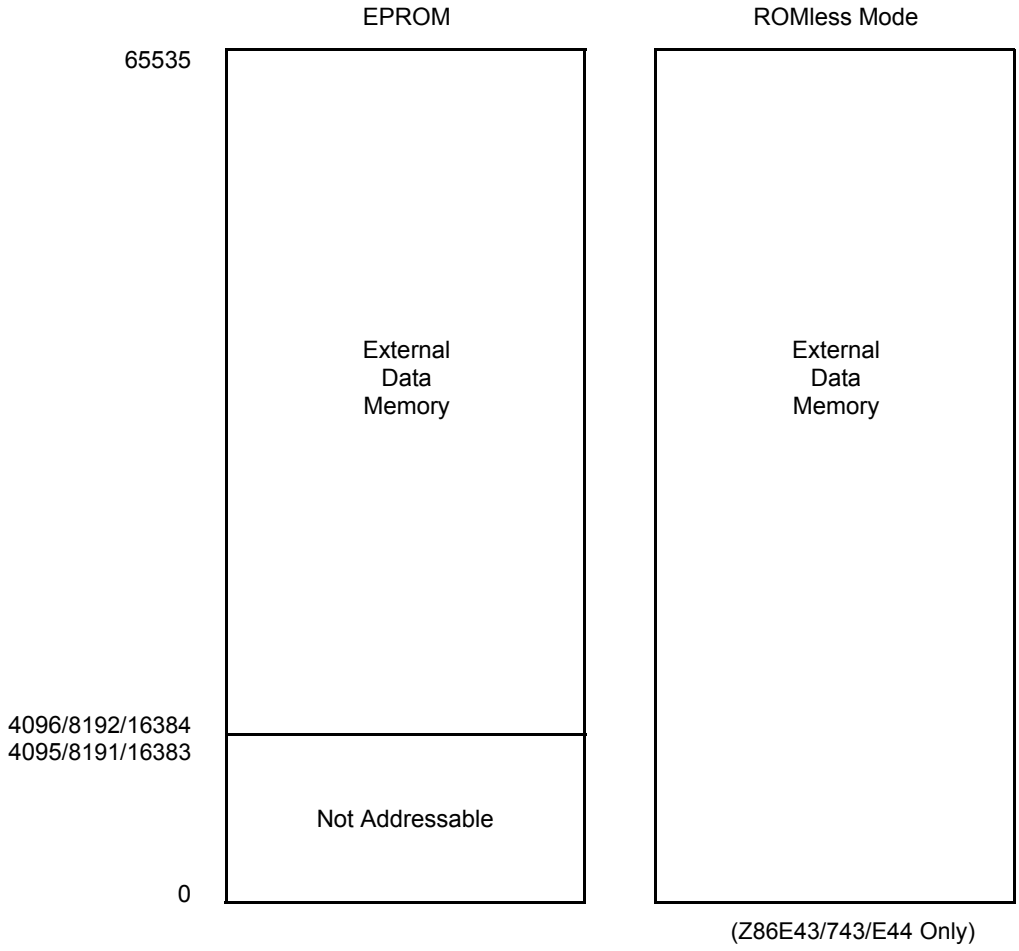


Figure 23. Data Memory Map

Register File. The register file consists of three I/O port registers, 236/125 general-purpose registers, 15 control and status registers, and three system configuration registers in the expanded register group. The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (see Figure 24). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: *Register Group E0-EF can only be accessed through working register and indirect addressing modes.*

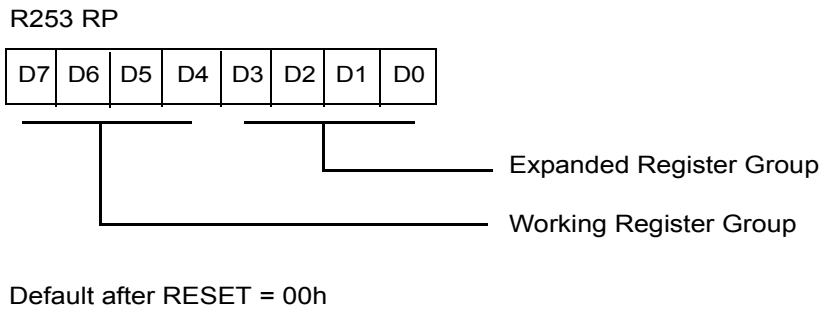


Figure 24. Register Pointer Register

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space RO through R15 is implemented as 16 groups of 16 registers per group (see Figure 26). These register banks are known as the Expanded Register File (ERF).

The low nibble (D3-D0) of the Register Pointer (RP) select the active ERF Bank, and the high nibble (D7-D4) of register RP select the working register group. Three system configuration registers reside in the Expanded Register File at bank FH: PCON, SMR, and WDTMR. The rest of the Expanded Register is not physically implemented and is reserved for future expansion.

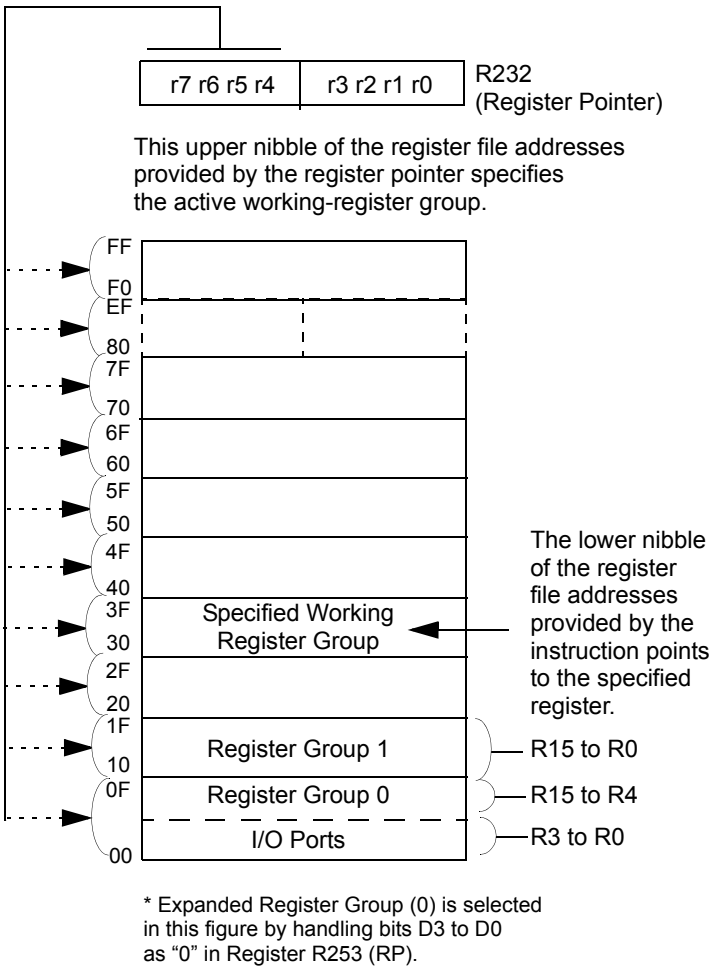


Figure 25. Register Pointer

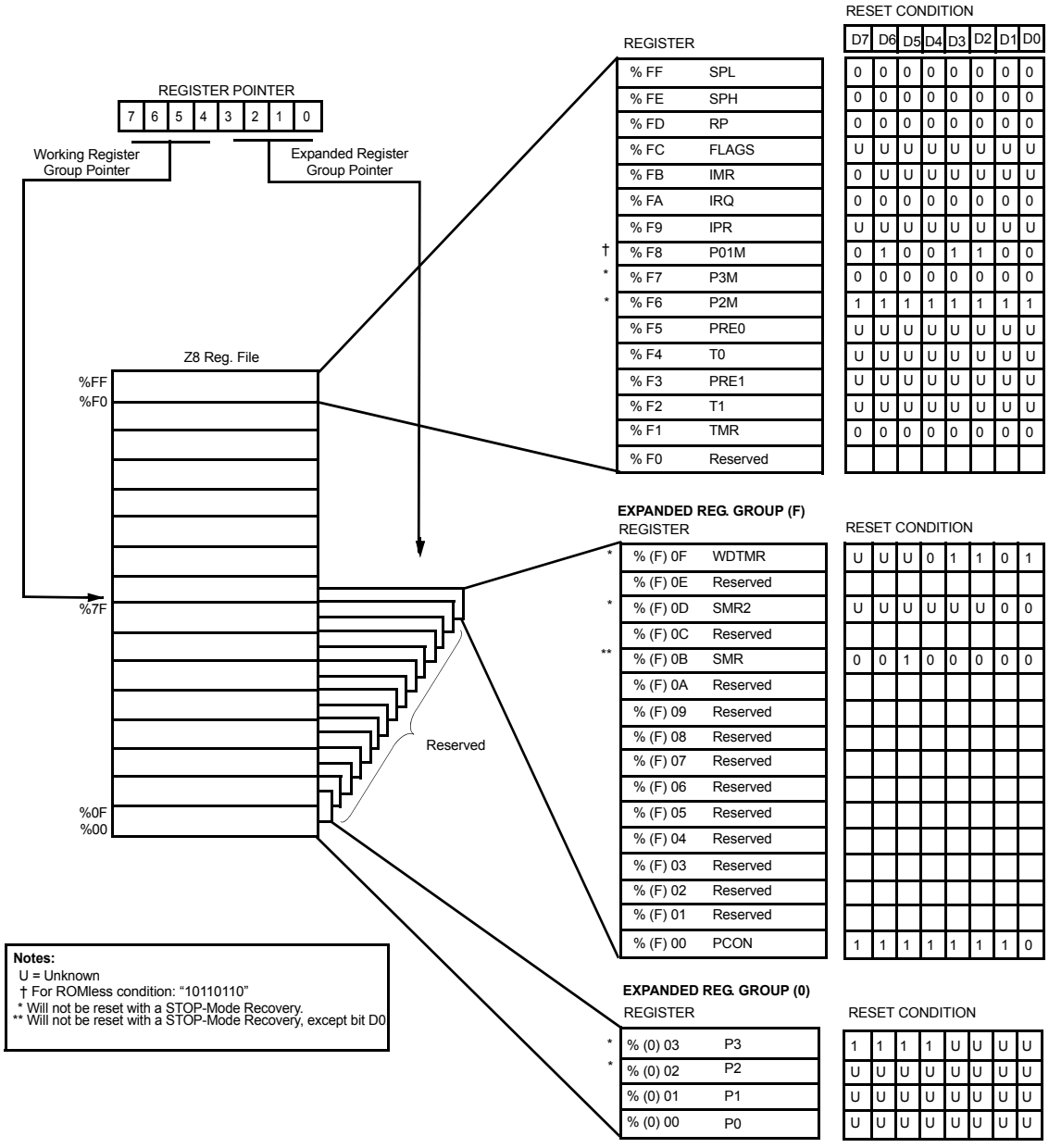


Figure 26. Expanded Register File Architecture

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. The register R254 is general-purpose on Z86E33/733/E34. R254 and R255 are set to 00h after any reset or Stop Mode Recovery.

RAM Protect. The upper portion of the RAM's address spaces 80h to EFh (excluding the control registers) can be protected from reading and writing. This option can be selected during the EPROM Programming Mode. After this option is selected, the user can activate this feature from the internal EPROM. D6 of the IMR control register (R251) is used to turn off/on the RAM protect by loading a 0 or 1, respectively. A "1" in D6 indicates RAM Protect enabled.

Stack. The Z86E43/743/E44 external data memory or the internal register file can be used for the stack. The 16-bit Stack Pointer (R254-R255) is used for the external stack, which can reside anywhere in the data memory for ROMless mode, but only from 4096/8192/16384 to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack on the Z8 that resides within the 236 general-purpose registers (R4-R239). SPH (R254) can be used as a general-purpose register when using internal stack only. R254 and R255 are set to 00H after any reset or Stop Mode Recovery.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The Ti prescaler is driven by internal or external clock sources; however, the TO prescaler is driven by the internal clock only (see Figure 27).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256), that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching one (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

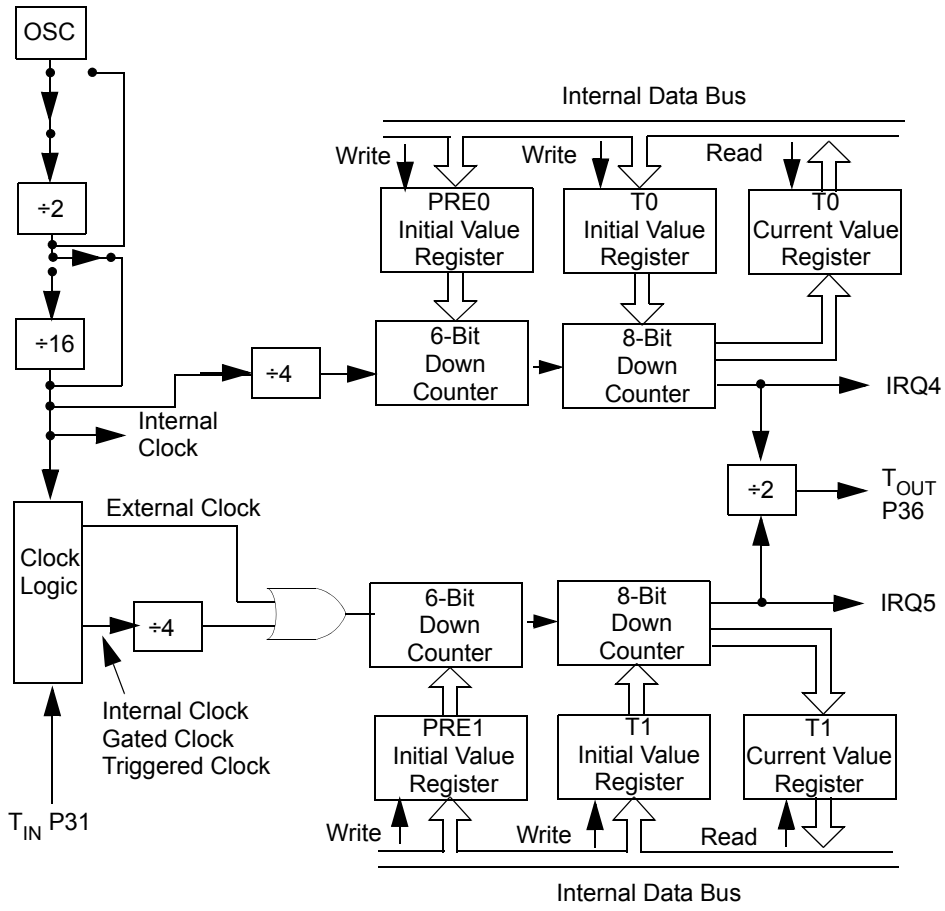


Figure 27. Counter/Timer Block Diagram

Interrupts. The MCU has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 28). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30) and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 20).

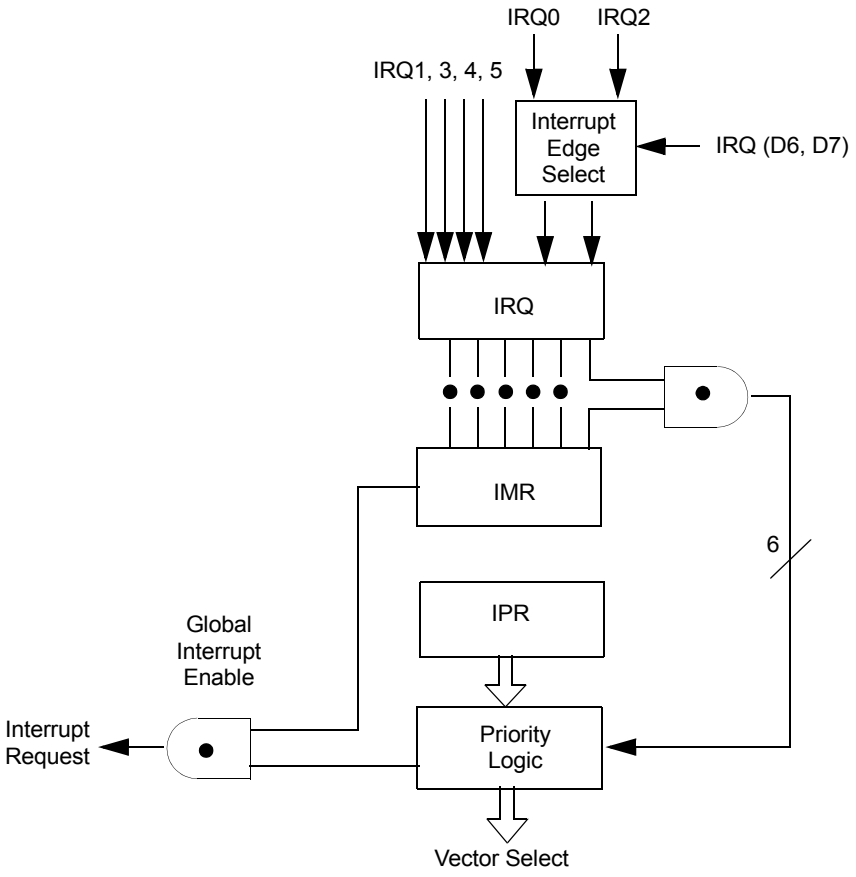


Figure 28. Interrupt Block Diagram

Table 20. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	$\overline{\text{DAV0}}$, IRQ0	0,1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2,3	External (P33), Falling Edge Triggered
IRQ2	$\overline{\text{DAV2}}$, IRQ2, T_{IN}	4,5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6,7	External (P30), Falling Edge Triggered
1RQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register (IPR). An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in Table 21.

Table 21. IRQ Register Configuration

IRO		Interrupt Edge	
D7	**D6**	**P31**	**P32**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes
1. F = Falling Edge
2. R = Rising Edge

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 16 MHz max, with a series resistance (RS) less than or equal to 100 Ω.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to device pin Ground. The RC oscillator option can be selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Table 29).

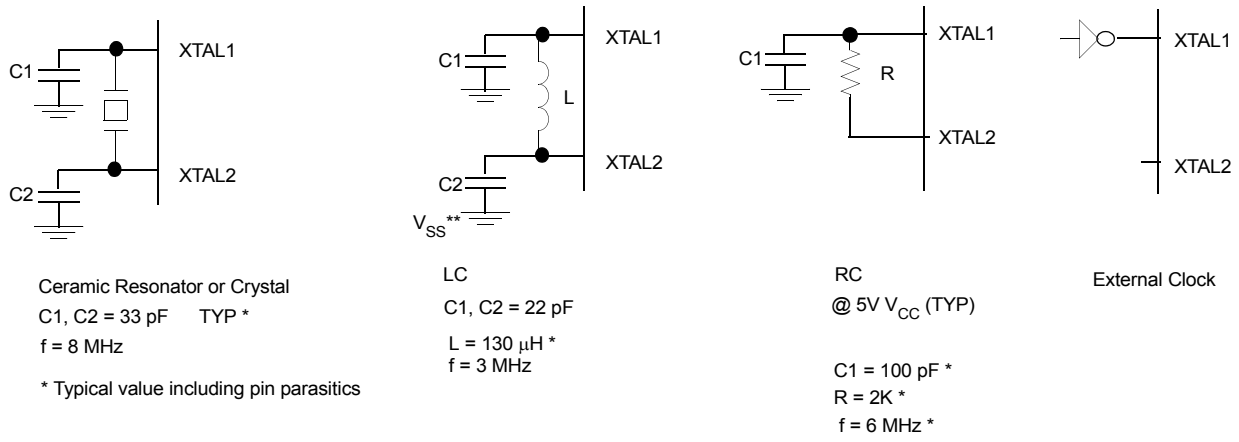


Figure 29. Oscillator Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status
2. Stop Mode Recovery (if D5 of SMR=0)
3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP mode Register (SMR) determines whether the POR timer is by-passed after Stop Mode Recovery (typical for an external clock and RC/LC oscillators with fast start up times).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT. In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, you must execute a NOP (Opcode = FFh) immediately before the appropriate sleep instruction, that is:

```
FF    NOP    ; clear the pipeline
6F    STOP   ; enter STOP mode
```

or

```
FF    NOP    ; clear the pipeline
7F    HALT   ; enter HALT mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. STOP Mode is terminated by one of the following resets: either by WDT time-out, POR, a Stop Mode Recovery Source, which is defined by the SMR register or external reset. This causes the processor to restart the application program at address 000Ch.

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2 and 3, and low EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00 (Figure 30).

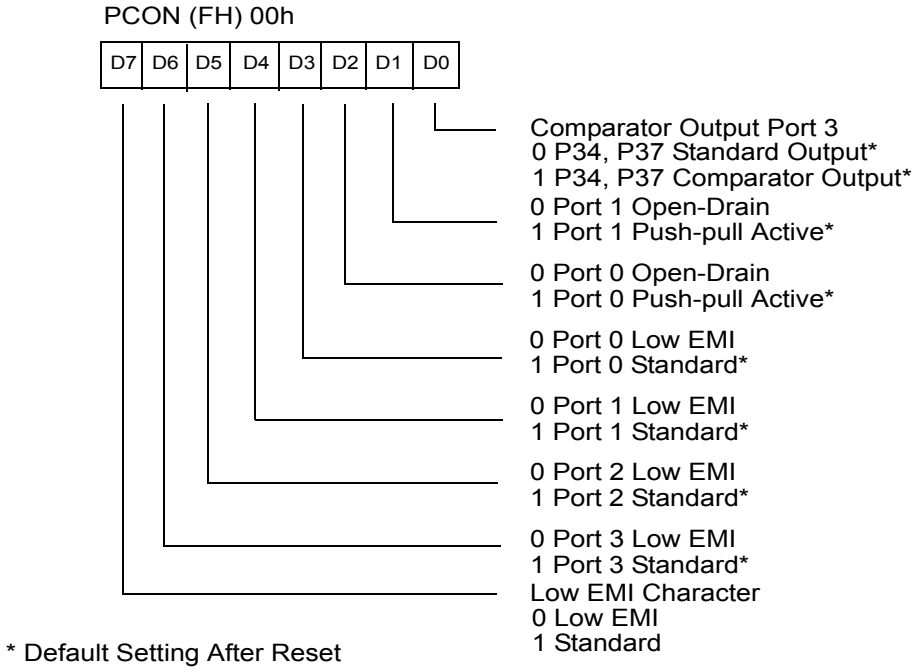


Figure 30. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0). Bit 0 controls the comparator output in Port 3. A "1" in this location brings the comparator outputs to P34 and P37, and a "0" releases the Port to its standard I/O configuration. The default value is 0.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

Low EMI Port 0 (D3). Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.

Low EMI Port 1 (D4). Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1.

Note: *The emulator does not support Port 1 low EMI mode and must be set D4 = 1.*

Low EMI Port 2 (D5). Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting this bit (D5=1). The default value is 1.

Low EMI Port 3 (D6). Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A "1" in this location configures the oscillator with standard drive. While a "0" configures the oscillator with low noise drive, however, it does not affect the relationship of SCLK and XTAL. The low EMI mode will reduce the drive of the oscillator (OSC). The default value is 1.

Note: *4 MHz is the maximum external clock frequency when running in the low EMI oscillator mode.*

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 31). All bits are Write Only except bit 7 which is a Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the Stop Mode Recovery Source. The SMR is located in Bank F of the Expanded Register File at address 0BH.

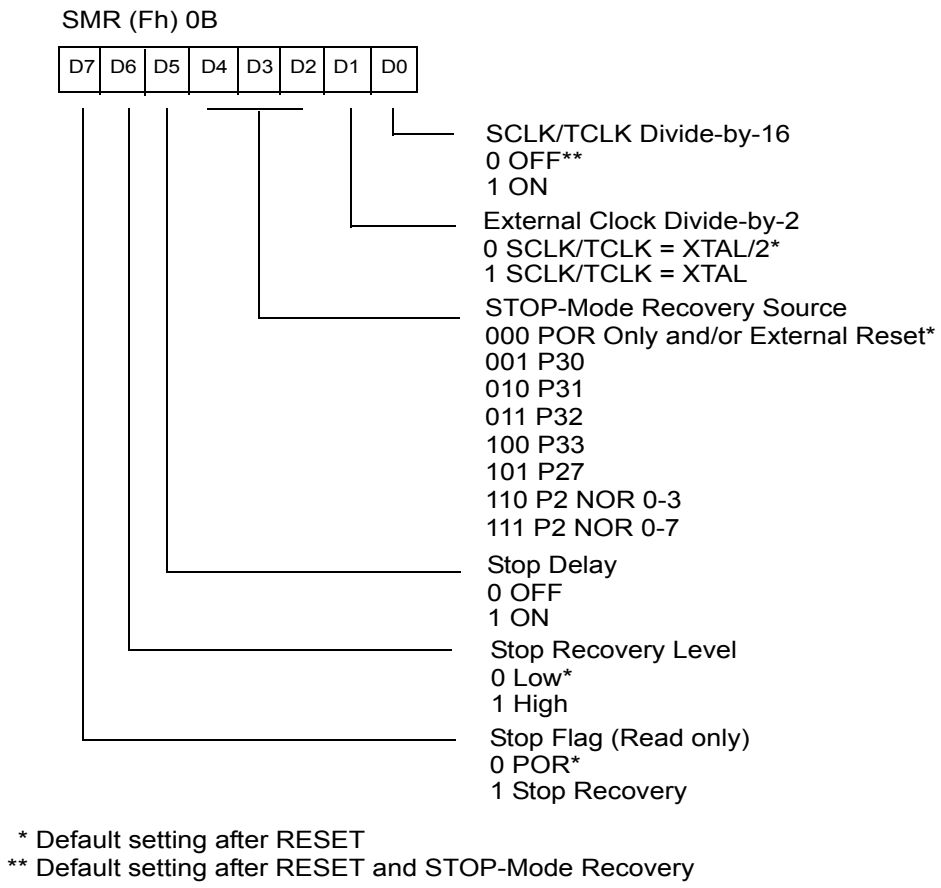


Figure 31. Stop Mode Recovery Register (Write-Only Except Bit D7, Which Is Read-Only)

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

Stop Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the Stop Mode Recovery (Figure 32). Table 22 shows the SMR source selected with the setting of D2 to D4. P33-P31 cannot be used to wake up

from STOP mode when programmed as analog inputs. When the Stop Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: *If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.*

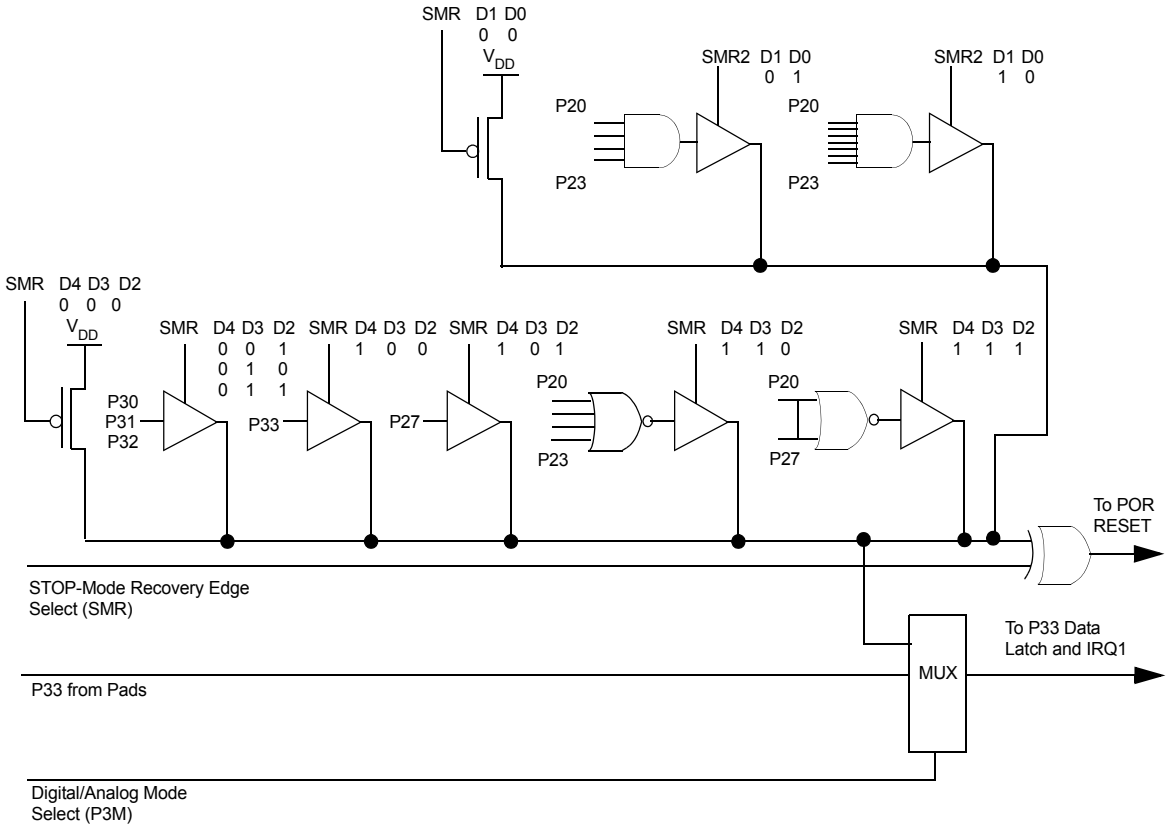


Figure 32. Stop Mode Recovery Source

Table 22. Stop Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0-3
1	1	1	Logical NOR of Port 2 bits 0-7

Stop Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop Mode Recovery is disabled by programming this bit to a zero. A "1" in this bit will cause a 5 ms RESET delay after Stop Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop Mode Recovery source needs to be kept active for at least 5TpC.

Stop Mode Recovery Level Select (D6). A "1" in this bit defines that a high level on any one of the recovery sources wakes the MCU from STOP Mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A "0" in this bit indicates that the device has been reset by POR (cold). A "1" in this bit indicates the device was awakened by a SMR source (warm).

Stop Mode Recovery Register 2 (SMR2). This register contains additional Stop Mode Recovery sources. When the Stop Mode Recovery sources are selected in this register then SMR Register Bits D2, D3, and D4 must be 0.

SMR:10		Operation
D1	DO	Description of Action
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watchdog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On

Reset and initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT is driven either by an on-board RC oscillator or an external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

Note: *Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.*

WDT Time-Out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained (Table 23). The default value of DO and Dl are 1 and 0, respectively.

Table 23. Time-out Period of WDT

D1	DO	Time-out of the Internal RC OSC	Time-out of the System Clock
0	0	5 ms	128 SCLK
0	1	10 ms[1]	256 SCLK[1]
1	0	20 ms	512 SCLK
1	1	80 ms	2048 SCLK

Note: The default setting is 10 ms.

WDT During HALT Mode (D2). This bit determines whether or not the WDT is active during HALT Mode. A “1” indicates that the WDT is active during HALT. A “0” disables the WDT in HALT Mode. The default value is “1 “. WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A “1” indicates active during STOP. A “0” disables the WDT during STOP Mode. This is applicable only when the WDT clock source is the internal RC oscillator.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1, and the WDT is stopped in STOP Mode. The default configuration of this bit is 0, which selects the RC oscillator.

Permanent WDT. When this feature is enabled, the WDT is enabled after reset and will operate in Run and HALT Mode. The control bits in the WDTMR do not affect the WDT operation. If the clock source of the WDT is the internal RC oscillator, then the WDT will run in STOP mode. If the clock source of the WDT is the XTAL1 pin, then the WDT will not run in STOP mode.

Note: *WDT time-out in STOP Mode will not reset SMR,SMR2,PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but will activate the T_{POR} delay.*

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 60 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watchdog reset or a Stop Mode Recovery (Figure 33 and Figure 34). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register File at address location 0Fh.

Clock Free WDT Reset. The WDT will enable the Z8 to reset the I/0 pins whenever the WDT times out, even without a clock source running on the XTAL1 and XTAL2 pins. WDTMR Bit D4 must be 0 for the clock Free WDT to work. The I/O pins will default to their default settings.

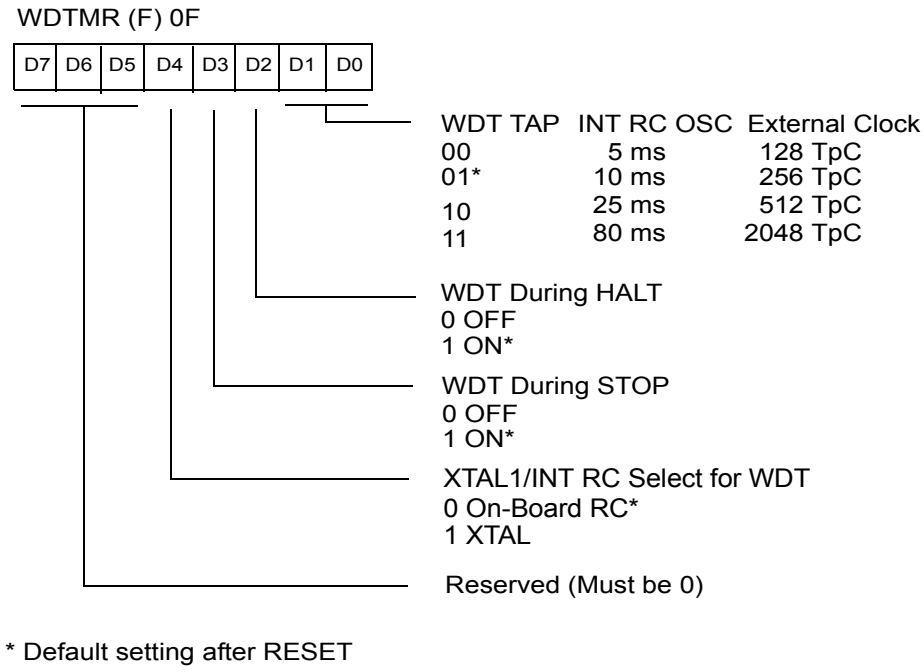


Figure 33. Watchdog Timer Mode Register Write Only

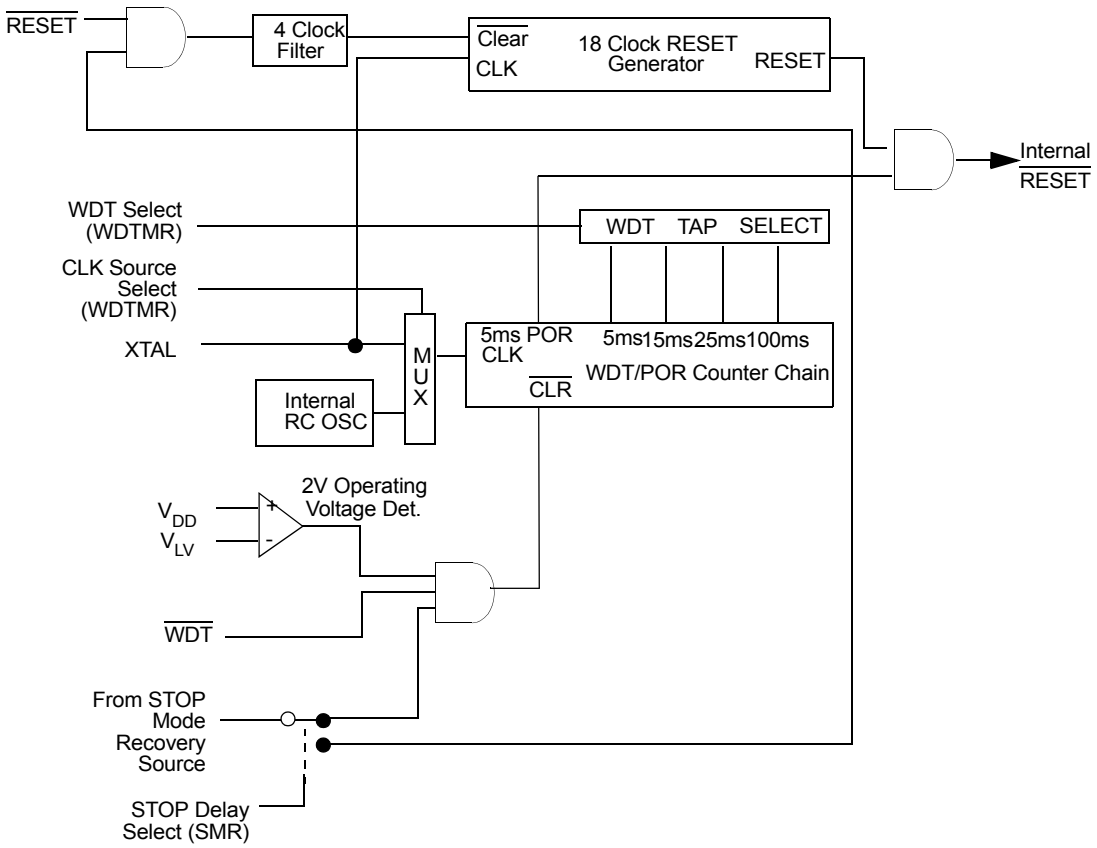


Figure 34. Resets and WDT

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below VLV (Figure 35).

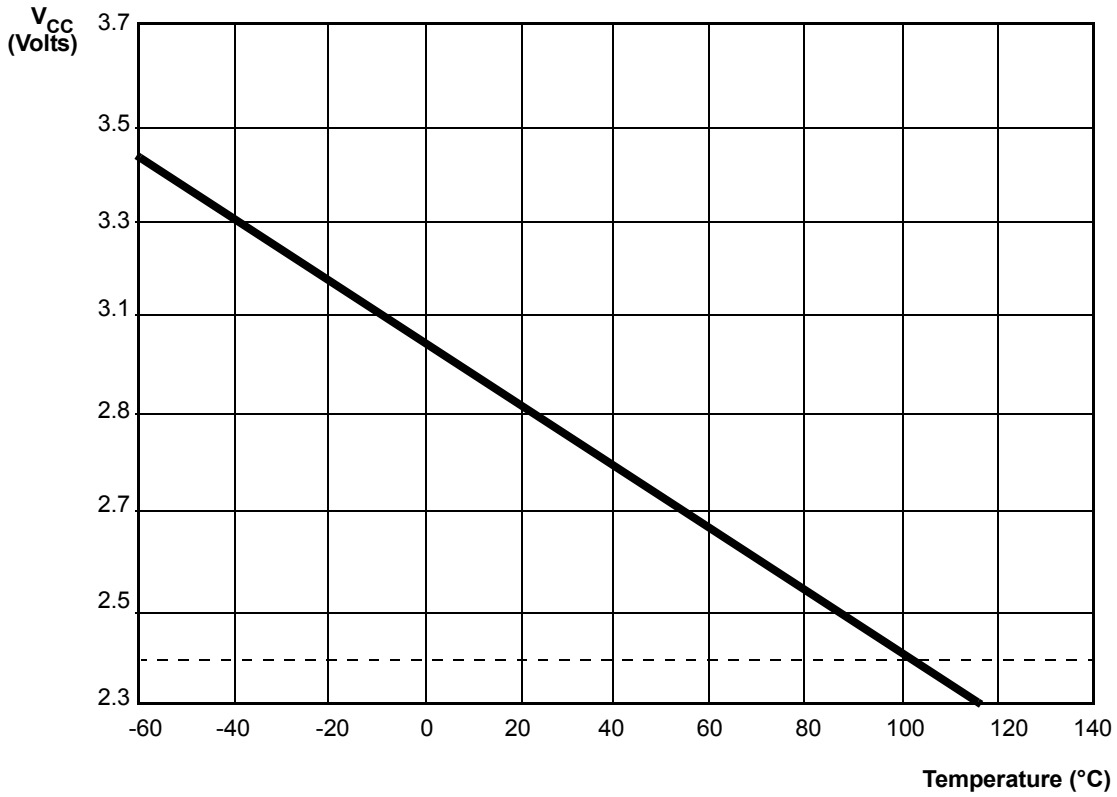


Figure 35. Typical V_{LV} Voltage vs. Temperature

Z8 Control Register Diagrams

Ordering Information

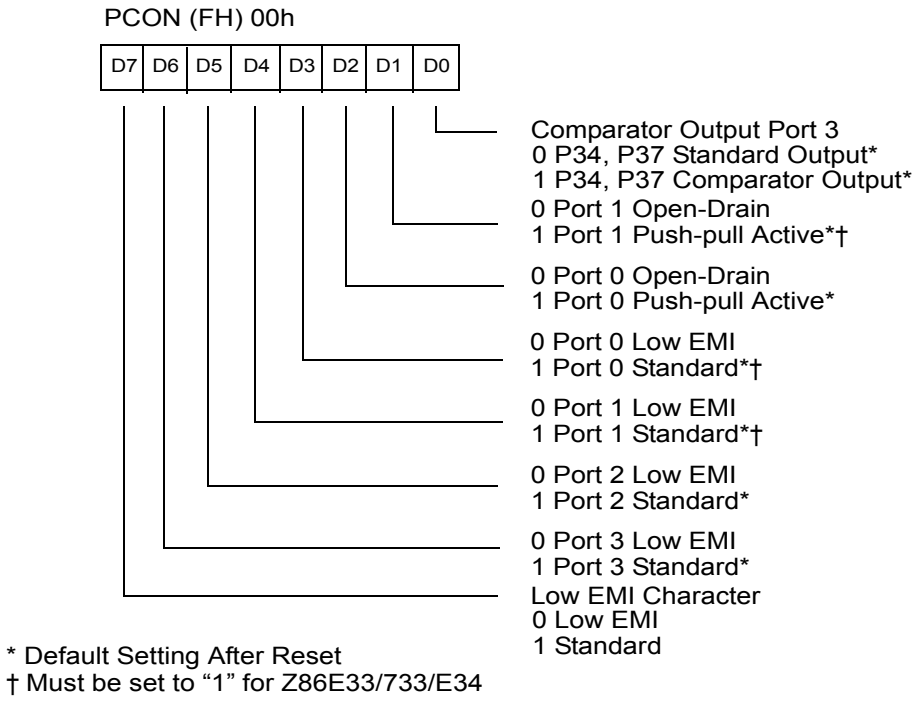
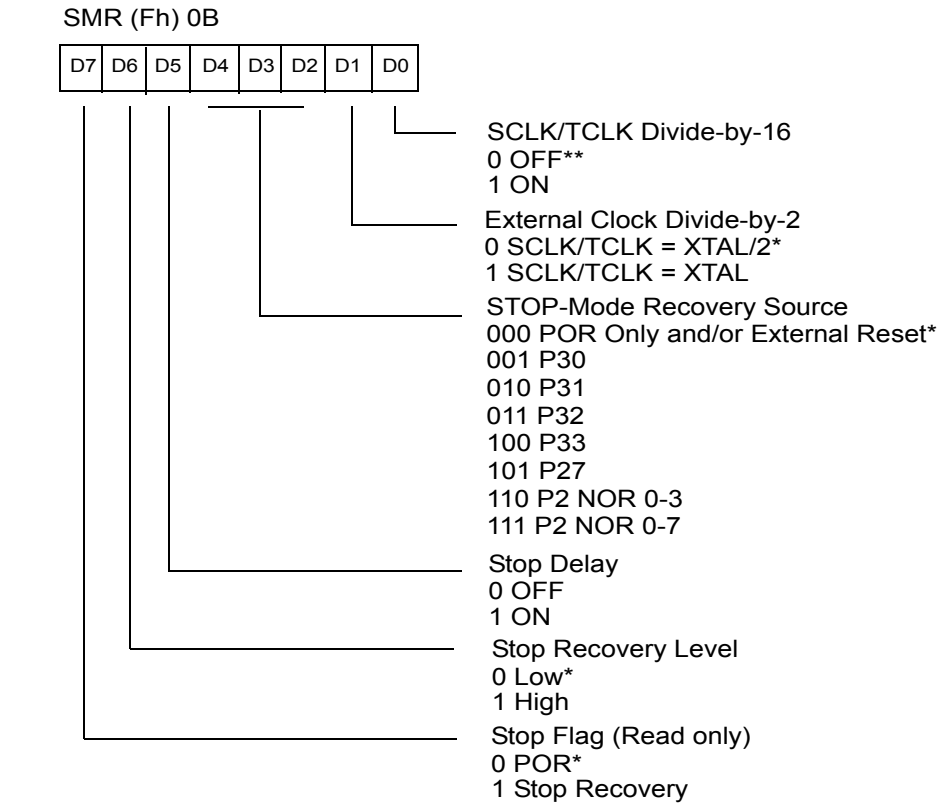
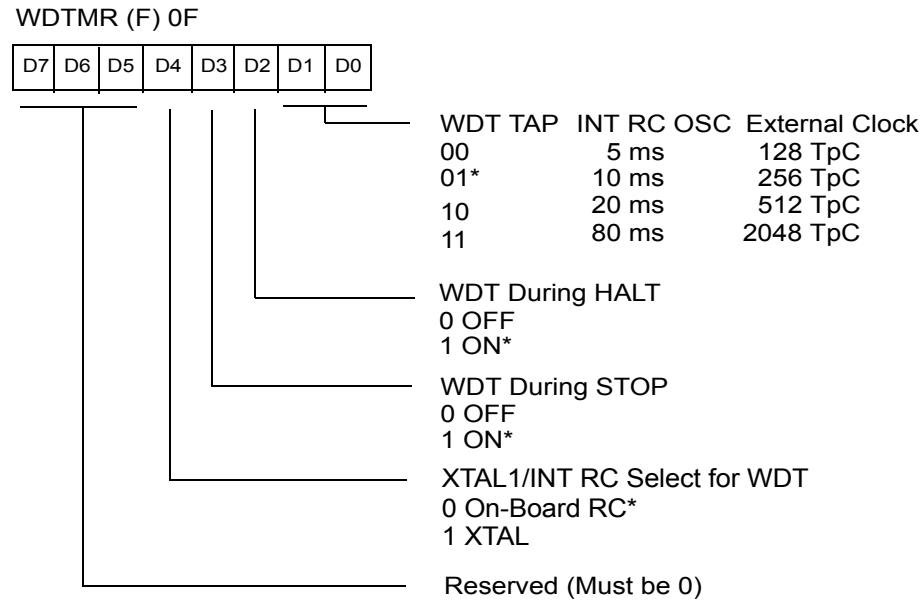


Figure 36. Port Configuration Register (PCON) (Write Only)



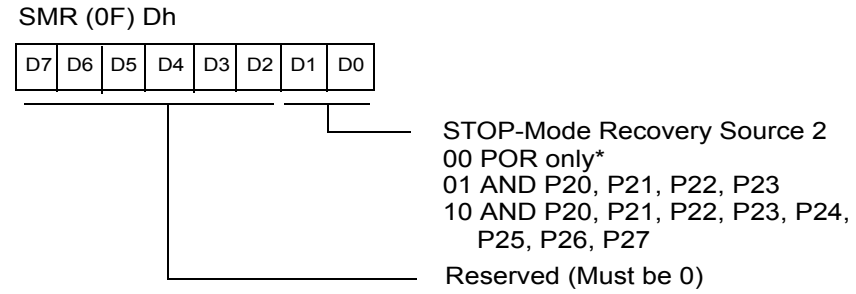
Note: Note used in conjunction with SMR2 Source
* Default setting after RESET
** Default setting after RESET and STOP-Mode Recovery

Figure 37. Stop Mode Recovery Register (Write Only Except Bit D7, Which is Read Only)



* Default setting after RESET

Figure 38. Watchdog Timer Mode Register (Write Only)



Note: Not used in conjunction with SMR Source

Figure 39. Stop Mode Recovery Register2 (Write Only)

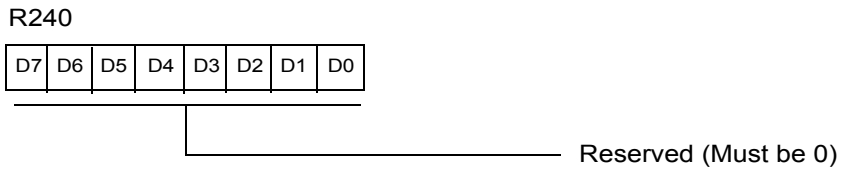


Figure 40. Reserved

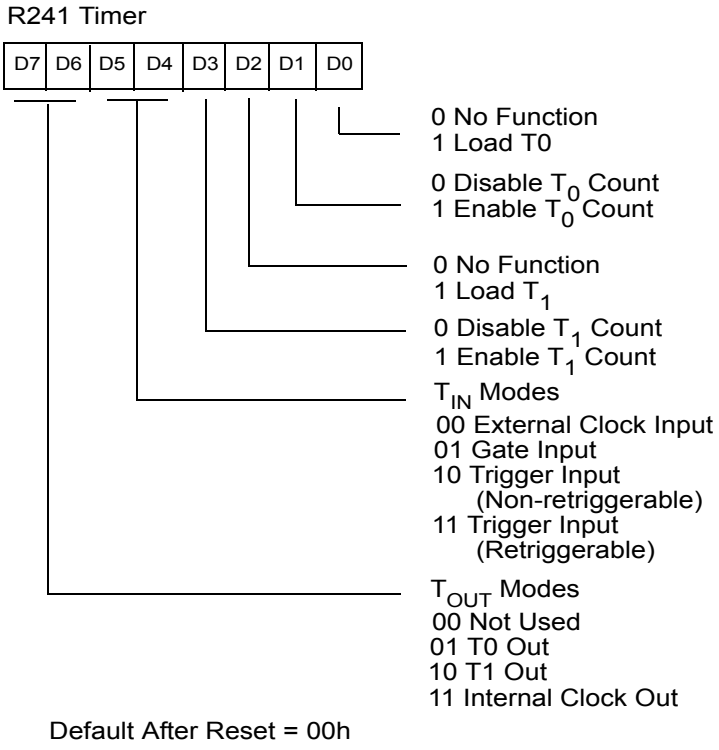


Figure 41. Timer Mode Register ($F1_h$: Read/Write)

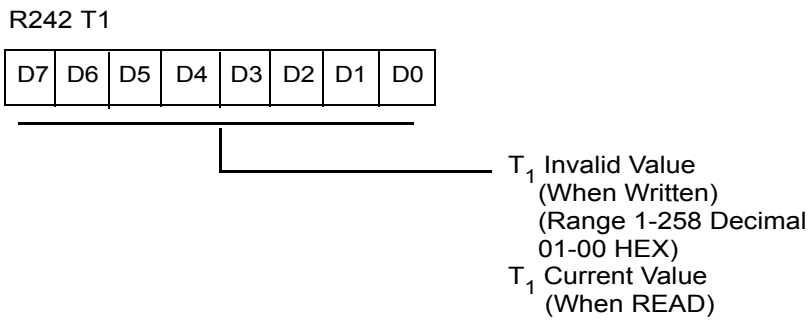


Figure 42. Counter/Timer 1 Register ($F2_h$: Read/Write)

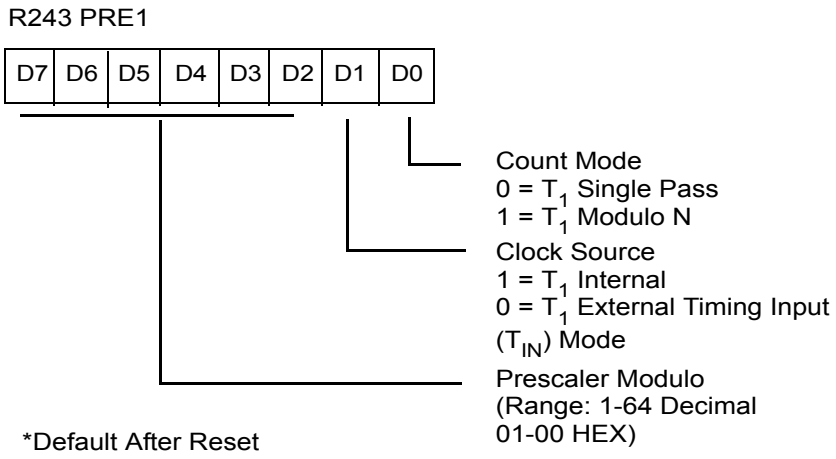


Figure 43. Prescaler 1 Register ($F3_h$: Write Only)

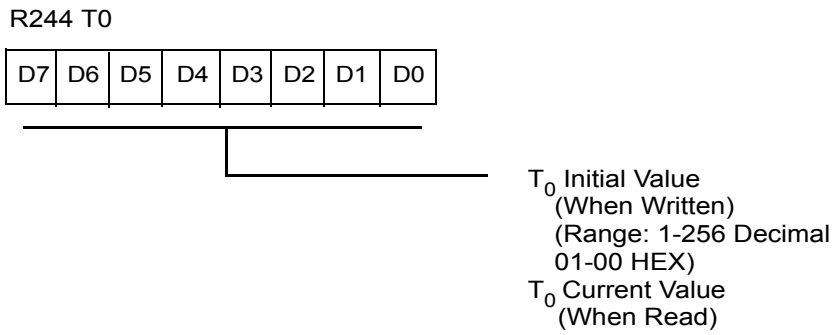


Figure 44. Counter/Timer 0 Register ($F4_h$: Read/Write)

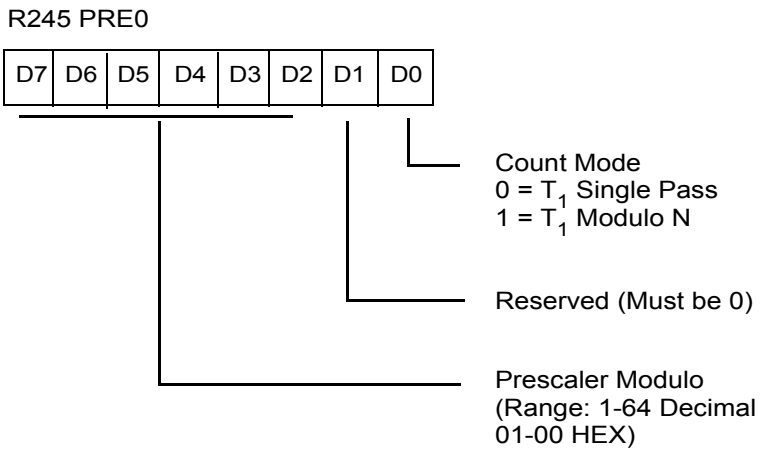


Figure 45. Prescaler 0 Register ($F5_h$: Write Only)

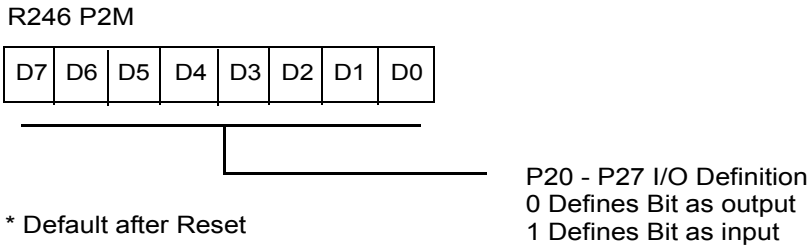


Figure 46. Port 2 Mode Register ($F6_h$: Write Only)

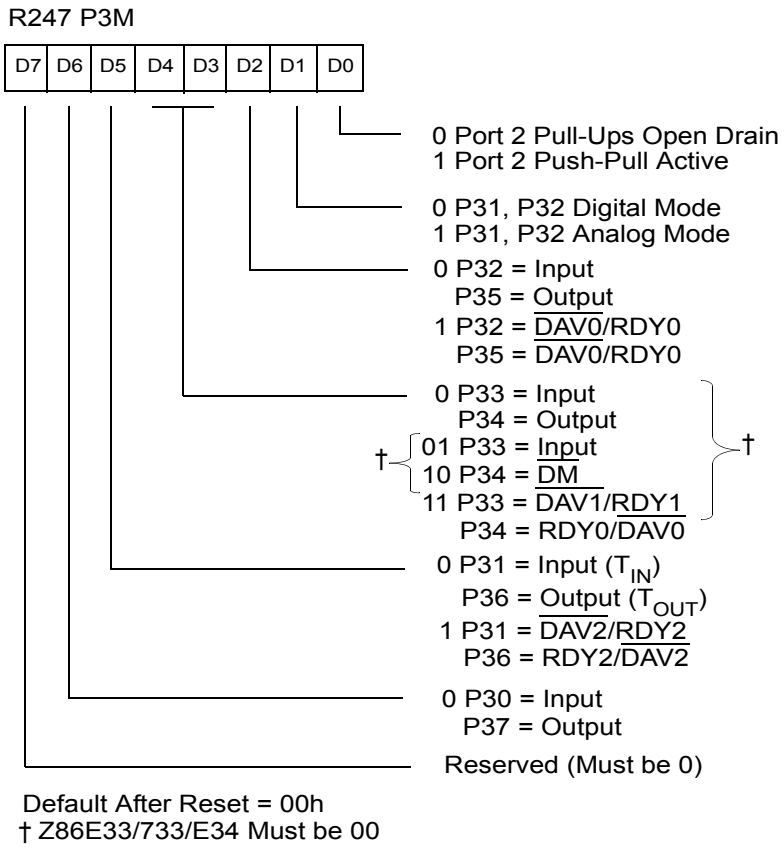
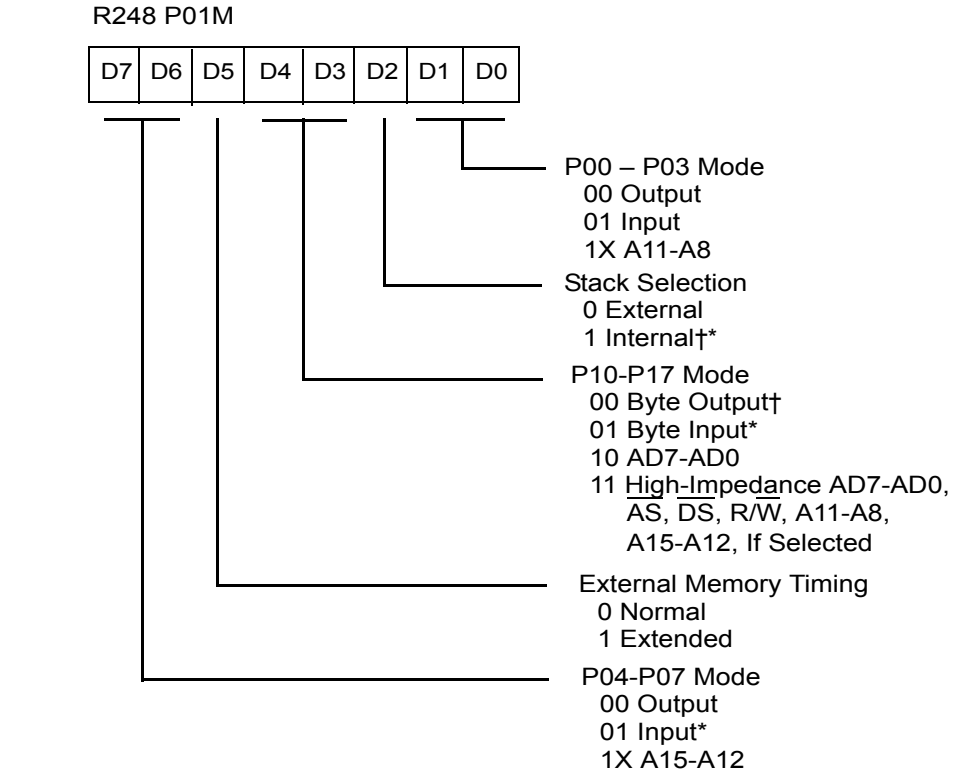


Figure 47. Port 3 Mode Register ($F7_h$: Write Only)



Reset Condition = 0100 1101B
For ROMless Condition = 1011 0110B
† Z86E33/733/E34 Must be 00
* Default after Reset

Figure 48. Port 0 and 1 Mode Register ($F8_h$: Write Only)

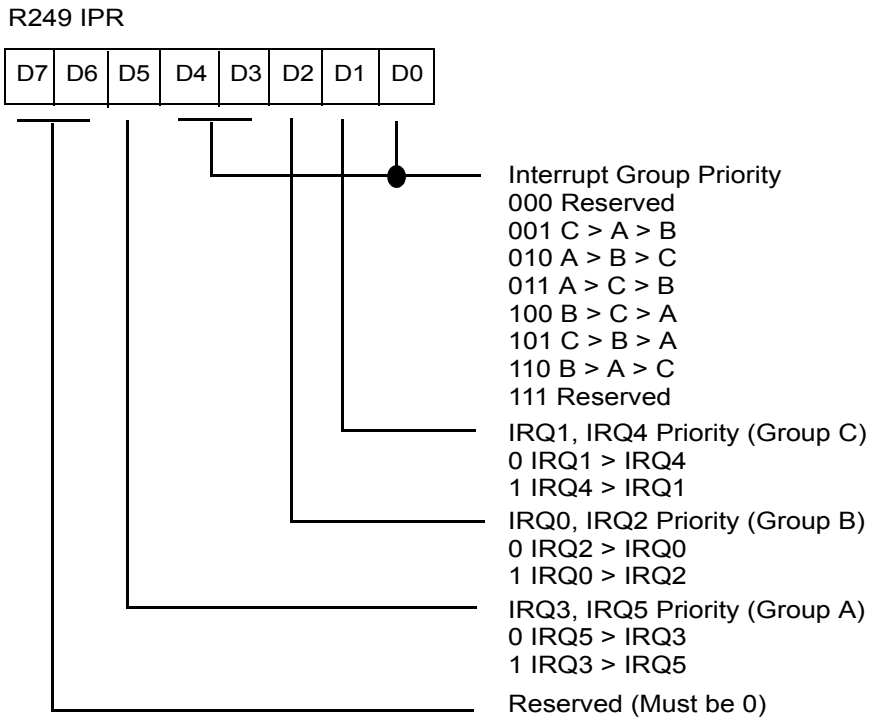


Figure 49. Interrupt Priority Register ($F9_h$: Write Only)

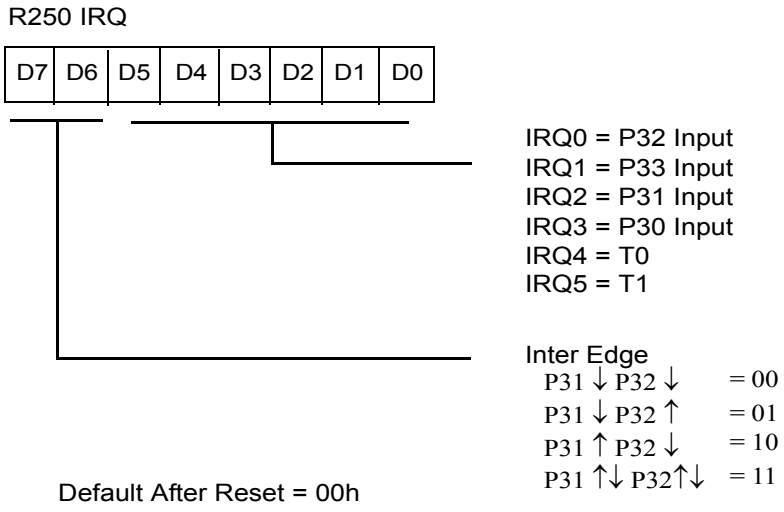


Figure 50. Interrupt Request Register (FA_h: Read/Write)

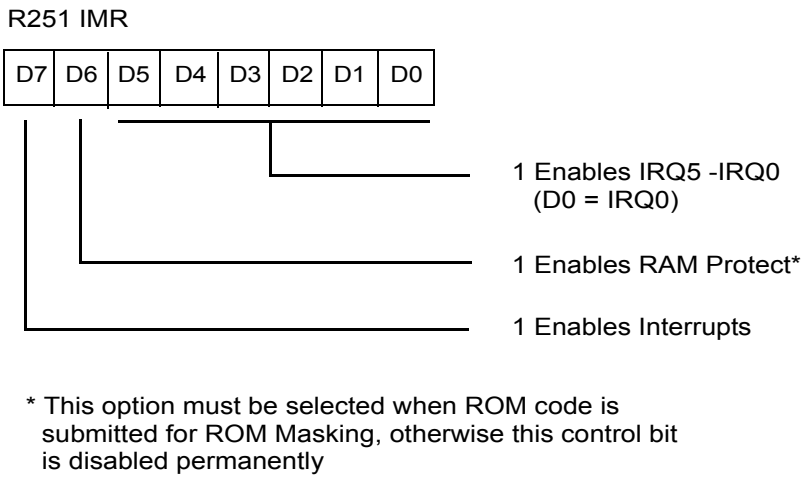


Figure 51. Interrupt Mask Register (FB_h: Read/Write)

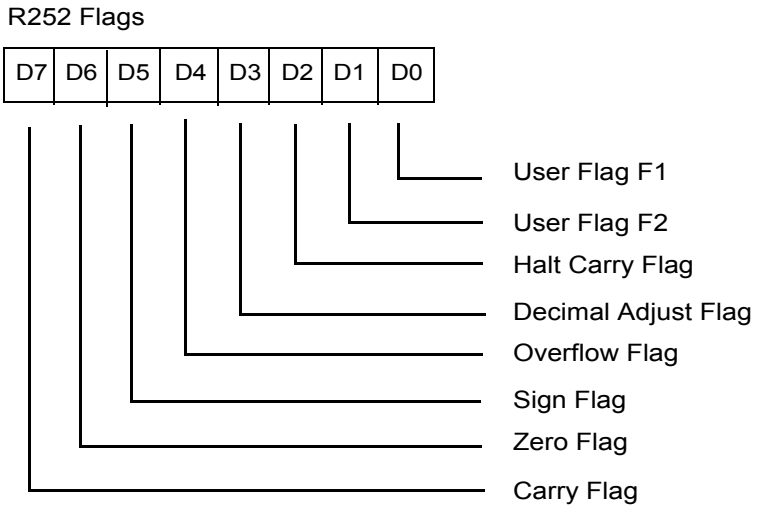


Figure 52. Flag Register (FC_h: Read/Write)

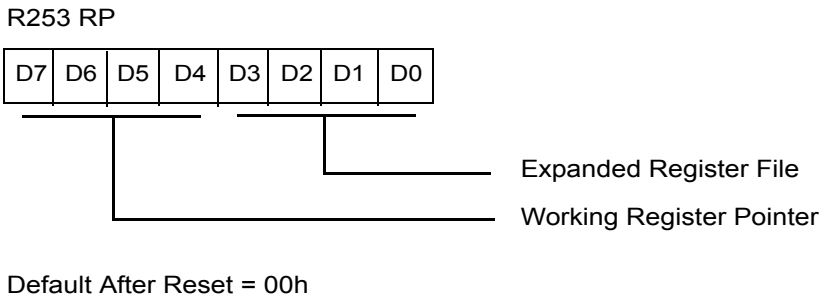


Figure 53. Register Pointer (FD_h: Read/Write)

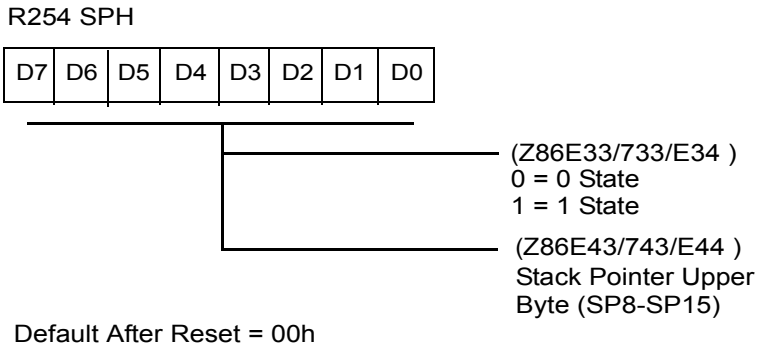


Figure 54. Stack Pointer High (FE_h: Read/Write)

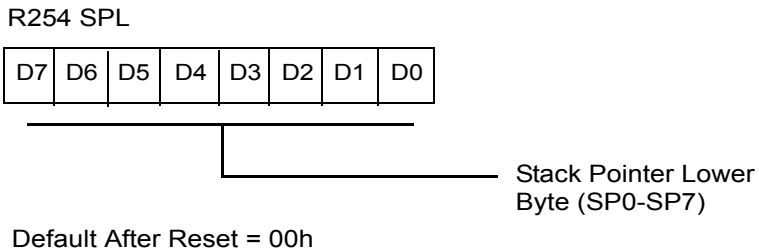
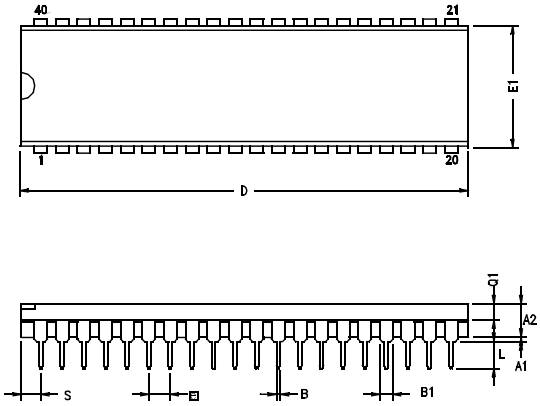


Figure 55. Stack Pointer Low (FF_h: Read/Write)

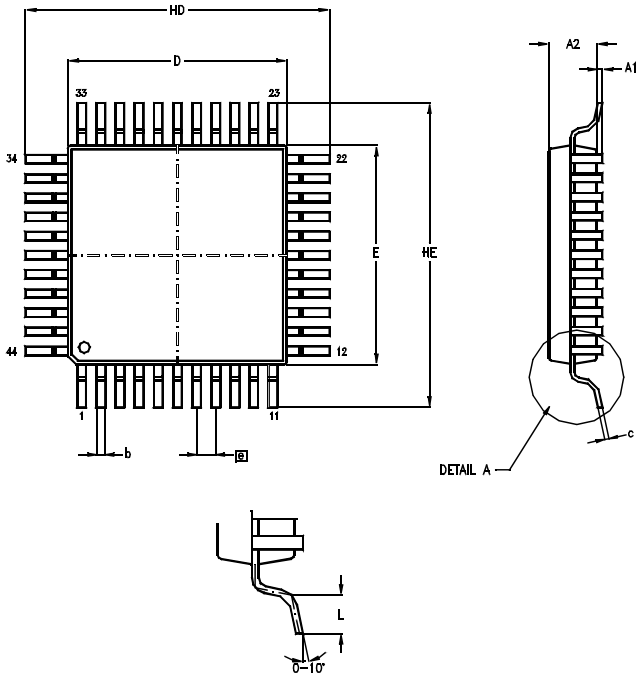
Package Information



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

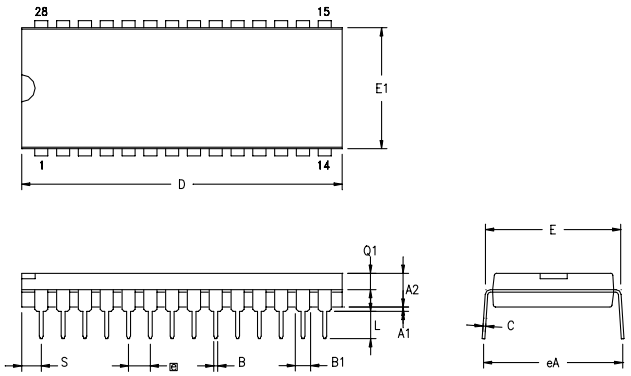
Figure 56. 40-PIN DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 BSC		.0315 BSC	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 .004"

Figure 57. 44-PIN LQFP Package Diagram

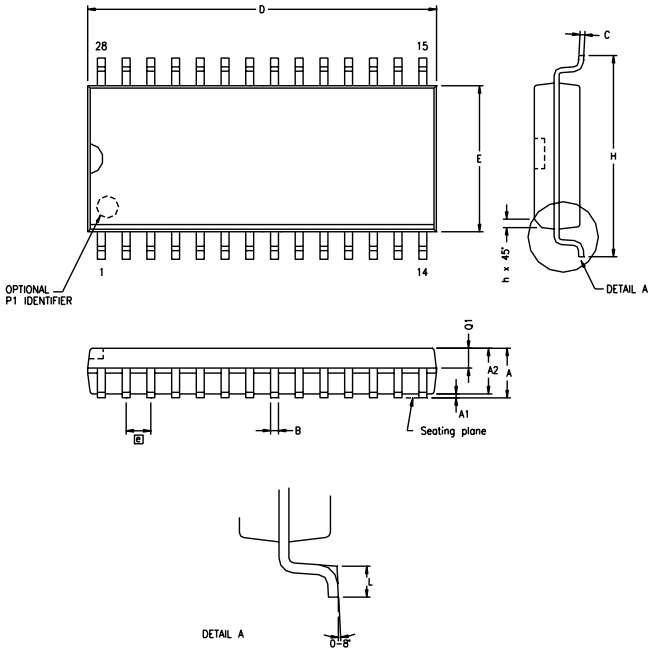


SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Figure 58. 28-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 59. 28-Pin SOIC Package Diagram

Ordering Information

Table 24.Ordering Information

Product	Speed (MHz)	Package Type	Pin Count
Z86E3312PSC	12	PDIP	28
Z86E3312SCC	12	SOIC	28
Z86E3312PSC	12	PLCC	28
Z86E3412PEC	12	PDIP	28
Z86E3412PSC	12	PDIP	28
Z86E3412SSC	12	SOIC	28
Z86E3412VSC	12	PLCC	28
Z86E4312FSC	12	LQFP	44
Z86E4312PSC	12	PDIP	40
Z86E4312VSC	12	PLCC	44
Z86E4412FSC	12	LQFP	44
Z86E4412PEC	12	PDIP	40
Z86E4412PSC	12	PDIP	40
Z86E4412VSC	12	PLCC	44
Z8673312PSC	12	PDIP	28
Z8673312SSC	12	SOIC	28
Z8673312VSC	12	PLCC	28
Z8674312FSC	12	LQFP	44
Z8674312PSC	12	PDIP	40
Z8674312VSC	12	PLCC	44

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.

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