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October 2013

FDB075N15A F085

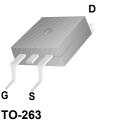
N-Channel Power Trench® MOSFET **150V**, **110A**, **7.5m** Ω

Features

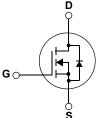
- Typ $r_{DS(on)}$ = 5.5m Ω at V_{GS} = 10V, I_D = 80A
- Typ $Q_{g(tot)}$ = 80nC at V_{GS} = 10V, I_D = 80A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Integrated Starter/alternator
- Primary Switch for 12V Systems



FDB SERIES





MOSFET Maximum Ratings $T_J = 25$ °C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage		150	V
V_{GS}	Gate to Source Voltage	±20	V	
	Drain Current - Continuous (V _{GS} =10) (Note 1) T _C = 25°C		110	А
ID	Pulsed Drain Current	T _C = 25°C	See Figure4	_ A
E _{AS}	Single Pulse Avalanche Energy	(Note 2)	502	mJ
D	Power Dissipation		333	W
P_{D}	Derate above 25°C		2.22	W/°C
T_J , T_{STG}	Operating and Storage Temperature		-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance Junction to Case		0.45	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient	(Note 3)	43	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB075N15A	FDB075N15A_F085	D2-PAK(TO-263)	330mm	24mm	800 units

- 1: Current is limited by bondwire configuration.
 2: Starting $T_J = 25^{\circ}C$, L = 0.24mH, $I_{AS} = 64$ A, $V_{DD} = 100$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche
 3: $R_{\theta,JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Units

Max

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

Parameter

Off Characteristics							
B _{VDSS}	Drain to Source Breakdown Voltage	I _D = 250μA, V	_{GS} = 0V	150	-	-	٧
	Desire to Course I calcage Current	V _{DS} =150V,	$T_{\rm J} = 25^{\rm o}{\rm C}$	-	-	1	μΑ
IDSS	Drain to Source Leakage Current	$V_{GS} = 0V$	$T_J = 175^{\circ}C(Note 4)$	-	-	1	mA
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V$		-	-	±100	nA

Test Conditions

Min

Тур

On Characteristics

Symbol

,	$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		2.0	3.0	4.0	V
Ī.	rps(on) Drain to Source On Resistance	I _D = 80A,	$T_J = 25^{\circ}C$	-	5.5	7.5	mΩ	
ď	DS(on)	Dialii to Source Off Resistance	V _{GS} = 10V	$T_J = 175^{\circ}C(Note 4)$	-	14.2	20	mΩ

Dynamic Characteristics

C _{iss}	Input Capacitance	7514.14		-	5595	-	pF
C _{oss}	Output Capacitance	$V_{DS} = 75V, V_{GS} = 6 = 1MHz$	$V_{DS} = 75V, V_{GS} = 0V,$ f = 1MHz		513	-	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1101112			16	-	pF
R_g	Gate Resistance	f = 1MHz	f = 1MHz		2.4	-	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	V _{GS} = 0 to 10V	V _{DD} = 75V	-	80	95	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2V	I _D = 80A	-	11	13	nC
Q_{gs}	Gate to Source Gate Charge			-	26.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	14	-	nC

Switching Characteristics

t _{on}	Turn-On Time		-	-	100	ns
t _{d(on)}	Turn-On Delay Time		-	33	-	ns
t _r	Rise Time	V _{DD} = 75V, I _D = 80A,	-	46	-	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10V, R_{GEN} = 6\Omega$	-	76	-	ns
t _f	Fall Time		-	25	-	ns
t _{off}	Turn-Off Time		-	-	138	ns

Drain-Source Diode Characteristics

Ved Source to Drain Diode Voltage	Source to Drain Diode Voltage	I _{SD} = 80A, V _{GS} = 0V		1.25	V	
	I _{SD} = 40A, V _{GS} = 0V	-	-	1.2	V	
T _{rr}	Reverse Recovery Time	$I_F = 80A$, $dI_{SD}/dt = 100A/\mu s$,	-	118	132	ns
Q _{rr}	Reverse Recovery Charge	V _{DD} =120V	-	341	494	nC

Notes

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

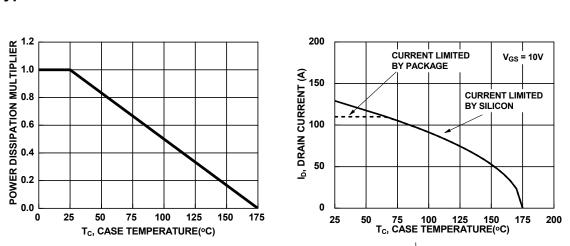


Figure 1. Normalized Power Dissipation vs Case Temperature

Typical Characteristics

Figure 2. Maximum Continuous Drain Current vs Case Temperature

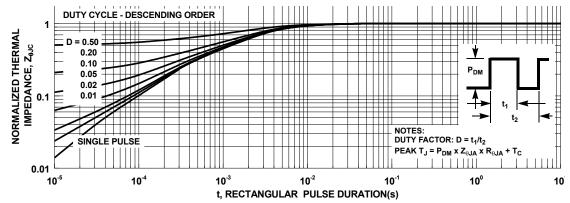


Figure 3. Normalized Maximum Transient Thermal Impedance

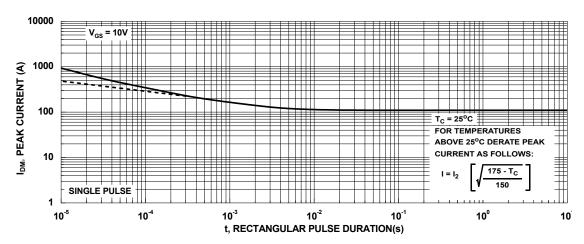


Figure 4. Peak Current Capability

Typical Characteristics

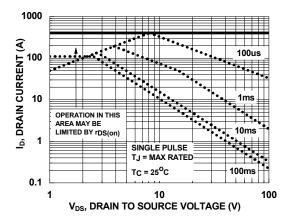
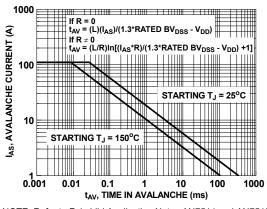


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching

Capability

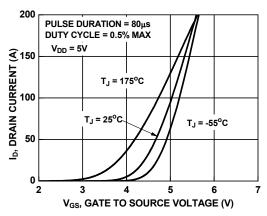


Figure 7. Transfer Characteristics

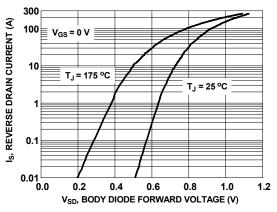


Figure 8. Forward Diode Characteristics

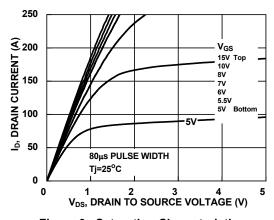


Figure 9. Saturation Characteristics

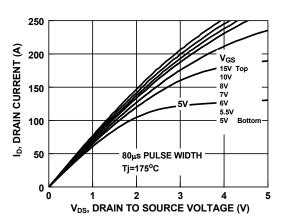


Figure 10. Saturation Characteristics

Typical Characteristics

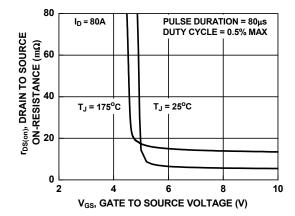


Figure 11. Rdson vs Gate Voltage

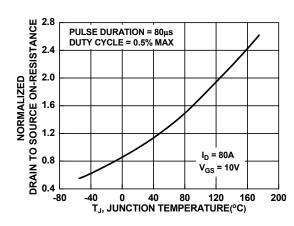


Figure 12. Normalized Rdson vs Junction Temperature

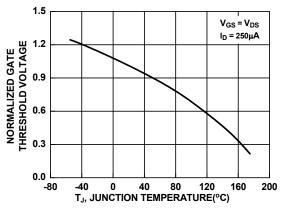


Figure 13. Normalized Gate Threshold Voltage vs
Temperature

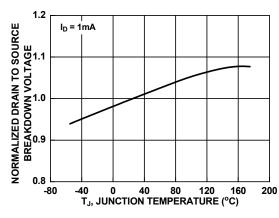


Figure 14. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

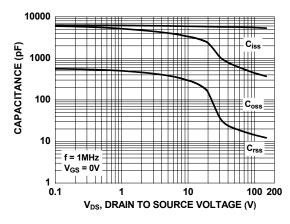


Figure 15. Capacitance vs Drain to Source Voltage

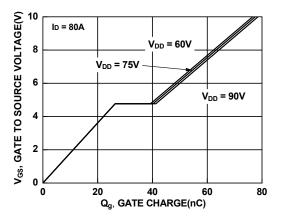


Figure 16. Gate Charge vs Gate to Source Voltage





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