

# BTS50080-1TMA

Smart High-Side Power Switch

PROFET®

One Channel

Automotive Power



Never stop thinking

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# Smart High-Side Power Switch PROFET® One Channel

**BTS50080-1TMA**



## 1 Overview

### Features

- Part of scalable product family
- Load current sense
- ReverSave®
- Very low standby current
- Current controlled input pin
- Improved electromagnetic compatibility (EMC)
- Fast demagnetization of inductive loads
- Stable behavior at under-voltage
- Green Product (RoHS compliant)
- AEC qualified



**PG-TO220-7-4**

|                                             |               |             |
|---------------------------------------------|---------------|-------------|
| Operating voltage                           | $V_{bb(on)}$  | 5.5 .. 38 V |
| Over-voltage protection                     | $V_{ON(CL)}$  | 39 V        |
| On-State resistance at 150°C                | $R_{DS(ON)}$  | 16 mΩ       |
| Nominal load current                        | $I_{L(nom)}$  | 9.5 A       |
| Load current (ISO)                          | $I_{L(ISO)}$  | 37.5 A      |
| Current limitation                          | $I_{L6(SC)}$  | 90 A        |
| Stand-by current for whole device with load | $I_{bb(OFF)}$ | 6 μA        |

The BTS50080-1TMA is a one channel high-side power switch in PG-TO220-7-4 package providing embedded protective functions.

The power transistor is built by a N-channel vertical power MOSFET with charge pump. The design is based on Smart SIPMOS chip on chip technology.

The BTS50080-1TMA has a current controlled input and offers a diagnostic feedback with load current sense and a defined fault signal in case of overload operation, overtemperature shutdown and/or short circuit shutdown.

| Type          | Package      | Marking |
|---------------|--------------|---------|
| BTS50080-1TMA | PG-TO220-7-4 | S50080A |

**Protective Functions**

- ReverSave<sup>®</sup>, channel switches on in case of reverse polarity
- Reverse battery protection without external components
- Short circuit protection with latch
- Over-load protection
- Multi-step current limitation
- Thermal shutdown with restart
- Over-voltage protection (including load dump)
- Loss of ground protection
- Loss of  $V_{bb}$  protection (with external diode for charged inductive loads)
- Electrostatic discharge protection (ESD)

**Diagnostic Functions**

- Proportional load current sense (with defined fault signal in case of overload operation, over temperature shutdown and/or short circuit shutdown)
- Open load detection in ON-state by load current sense

**Applications**

- $\mu$ C compatible high-side power switch with diagnostic feedback for 12 V grounded loads
- All types of resistive, inductive and capacitive loads
- Most suitable for loads with high inrush currents, so as lamps
- Replaces electromechanical relays, fuses and discrete circuits

## 2 Block Diagram and Terms

### 2.1 Block Diagram

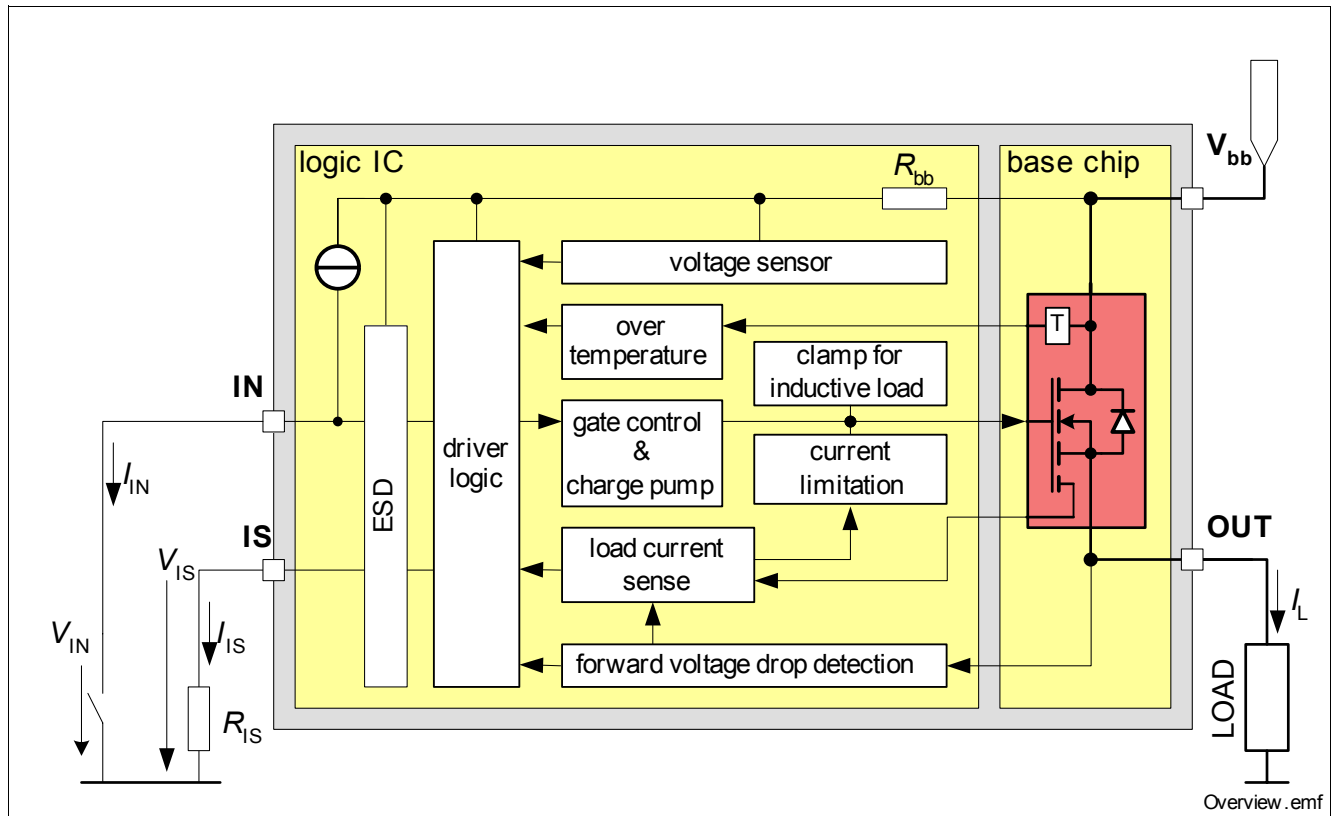


Figure 1 Block Diagram

### 2.2 Terms

Following figure shows all terms used in this data sheet.

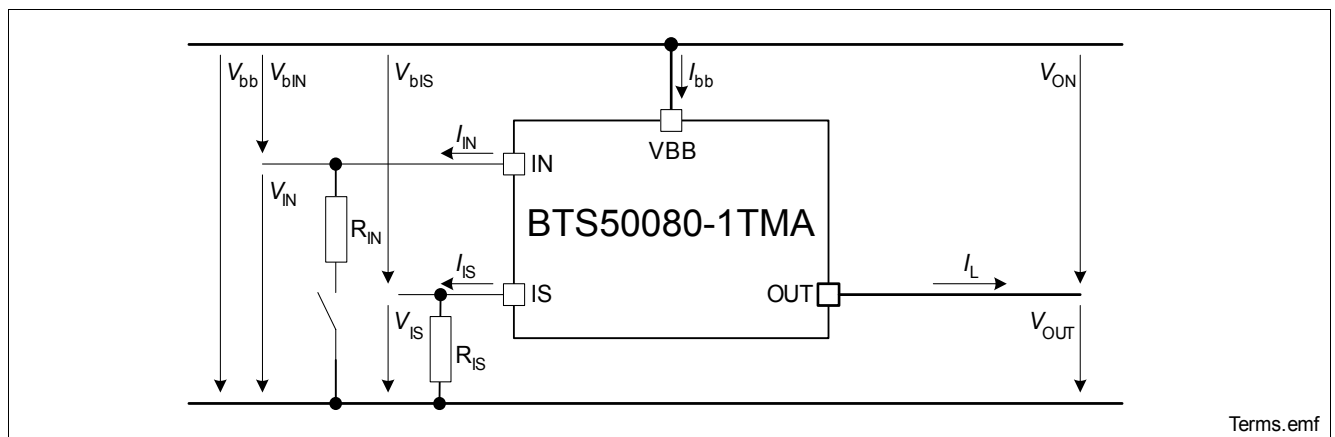
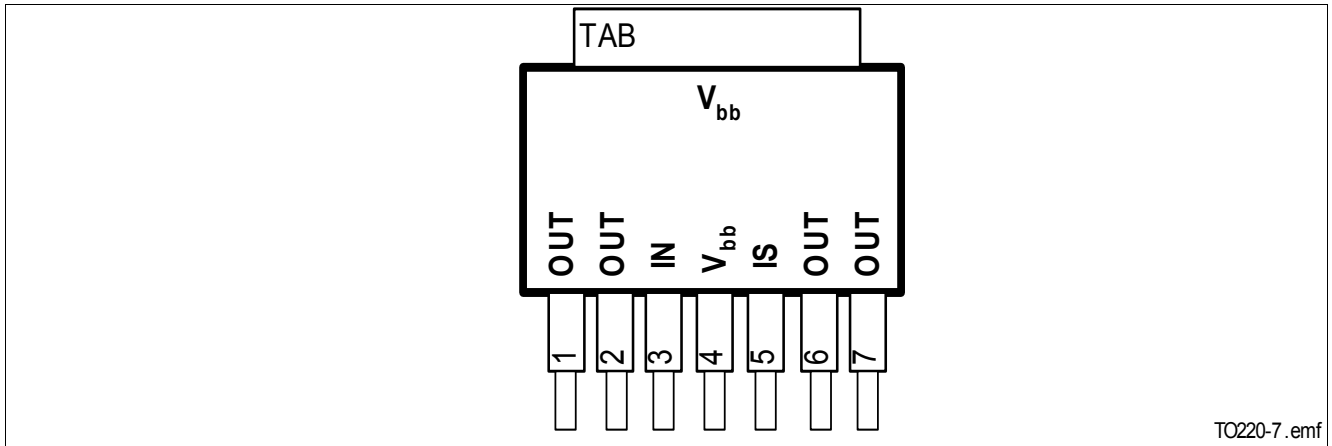


Figure 2 Terms

### 3 Pin Configuration

#### 3.1 Pin Assignment BTS50080-1TMA



TO220-7.emf

Figure 3 Pin Configuration

#### 3.2 Pin Definitions and Functions

| Pin  | Symbol   | Function                                                                                                                                                                                                                                                                   |
|------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 2 | OUT      | <b>Output;</b> output to the load; pin 1, 2, 6 and 7 must be externally shorted. <sup>1)</sup>                                                                                                                                                                             |
| 3    | IN       | <b>Input;</b> activates the power switch if shorted to ground.                                                                                                                                                                                                             |
| 4    | $V_{bb}$ | <b>Supply Voltage;</b> positive power supply voltage; tab and pin 4 are internally shorted.                                                                                                                                                                                |
| 5    | IS       | <b>Sense Output;</b> Diagnostic feedback; provides at normal operation a sense current proportional to the load current; in case of overload, over temperature and/or short circuit a defined current is provided (see <a href="#">Table 1 "Truth Table" on Page 21</a> ). |
| 6, 7 | OUT      | <b>Output;</b> output to the load; pin 1, 2, 6 and 7 must be externally shorted. <sup>1)</sup>                                                                                                                                                                             |
| TAB  | $V_{bb}$ | <b>Supply Voltage;</b> positive power supply voltage; tab and pin 4 are internally shorted.                                                                                                                                                                                |

1) Not shorting all outputs will considerably increase the on-state resistance, reduce the peak current capability, the clamping capability and decrease the current sense accuracy.

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings <sup>1)</sup>

$T_j = 25^\circ\text{C}$  (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values |      | Unit | Conditions |
|------|-----------|--------|--------------|------|------|------------|
|      |           |        | Min.         | Max. |      |            |

#### Supply Voltages

|       |                                                                               |              |     |    |   |                                          |
|-------|-------------------------------------------------------------------------------|--------------|-----|----|---|------------------------------------------|
| 4.1.1 | Supply voltage                                                                | $V_{bb}$     | -16 | 38 | V | –                                        |
| 4.1.2 | Supply voltage for full short circuit protection (single pulse) <sup>2)</sup> | $V_{bb(SC)}$ | 0   | 30 | V | –                                        |
| 4.1.3 | Supply Voltage for Load Dump protection <sup>3)</sup>                         | $V_{bb(LD)}$ | –   | 45 | V | $R_l = 2\ \Omega$ ,<br>$R_L = 1\ \Omega$ |

#### Logic Pins

|       |                                       |               |      |    |            |   |
|-------|---------------------------------------|---------------|------|----|------------|---|
| 4.1.4 | Voltage at input pin                  | $V_{bIN}$     | -16  | 63 | V          | – |
| 4.1.5 | Current through input pin             | $I_{IN}$      | -120 | 15 | mA         | – |
| 4.1.6 | Voltage at current sense pin          | $V_{bIS}$     | -16  | 63 | V          | – |
| 4.1.7 | Current through sense pin             | $I_{IS}$      | -120 | 15 | mA         | – |
| 4.1.8 | Input voltage slew rate <sup>4)</sup> | $dV_{bIN}/dt$ | -20  | 20 | V/ $\mu$ s | – |

#### Power Stages

|        |                                                       |          |   |             |   |                                                                                            |
|--------|-------------------------------------------------------|----------|---|-------------|---|--------------------------------------------------------------------------------------------|
| 4.1.9  | Load current <sup>5)</sup>                            | $I_L$    | - | $I_{L(SC)}$ | A | –                                                                                          |
| 4.1.10 | Maximum energy dissipation per channel (single pulse) | $E_{AS}$ | - | 0.4         | J | $V_{bb} = 12\ \text{V}$ ,<br>$I_{L(0)} = 20\ \text{A}$ ,<br>$T_{j(0)} = 150^\circ\text{C}$ |

#### Temperatures

|        |                      |           |     |     |                  |   |
|--------|----------------------|-----------|-----|-----|------------------|---|
| 4.1.11 | Junction temperature | $T_j$     | -40 | 150 | $^\circ\text{C}$ | – |
| 4.1.12 | Storage temperature  | $T_{stg}$ | -55 | 150 | $^\circ\text{C}$ | – |

#### ESD Susceptibility

|        |                        |           |    |   |    |                                       |
|--------|------------------------|-----------|----|---|----|---------------------------------------|
| 4.1.13 | ESD susceptibility HBM | $V_{ESD}$ | -3 | 3 | kV | according to<br>EIA/JESD 22-A<br>114B |
|--------|------------------------|-----------|----|---|----|---------------------------------------|

1) Not subject to production test, specified by design.

2) Short circuit is defined as a combination of remaining resistances and inductances. See [Figure 13](#).

3) Load Dump is specified in ISO 7637,  $R_l$  is the internal resistance of the Load Dump pulse generator.

4) Slew rate limitation can be achieved by means of using a series resistor for the small signal driver or in series in the input path. A series resistor  $R_{IN}$  in the input path is also required for reverse operation at  $V_{bb} \leq -16\text{V}$ . See also [Figure 14](#).

5) Current limitation is a protection feature. Operation in current limitation is considered as “outside” normal operating range. Protection features are not designed for continuous repetitive operation.

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Thermal Resistance

| Pos.  | Parameter                         | Symbol     | Limit Values |      |      | Unit | Conditions |
|-------|-----------------------------------|------------|--------------|------|------|------|------------|
|       |                                   |            | Min.         | Typ. | Max. |      |            |
| 4.2.1 | Junction to Case <sup>1)</sup>    | $R_{thjc}$ | —            | 0.7  | 0.8  | K/W  | —          |
| 4.2.2 | Junction to Ambient <sup>1)</sup> | $R_{thja}$ |              |      |      | K/W  | —          |
|       | free air                          |            | -            | 60   | -    |      |            |
|       | device on PCB <sup>2)</sup>       |            | -            | 33   | -    |      |            |

1) Not subject to production test, specified by design.

2) Device mounted on PCB (50 mm x 50 mm x 1.5mm epoxy, FR4) with 6 cm<sup>2</sup> copper heatsinking area (one layer, 70 µm thick) for  $V_{bb}$  connection. PCB is vertical without blown air.

## 5 Power Stages

The power stage is built by a N-channel vertical power MOSFET (DMOS) with charge pump.

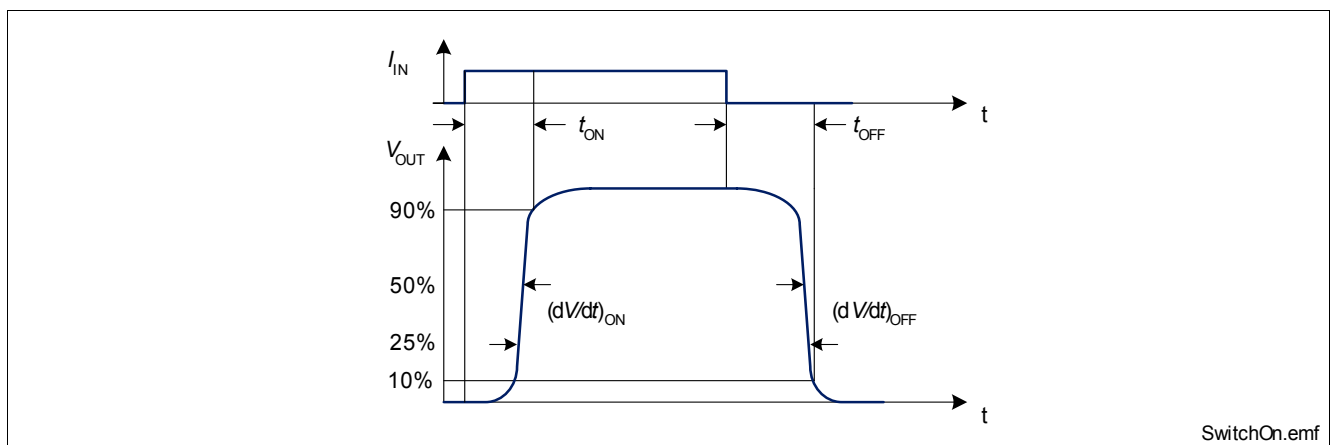
### 5.1 Input Circuit

**Figure 4** shows the input circuit of the BTS50080-1TMA. The current source to  $V_{bb}$  ensures that the device switches off in case of open input pin. The zener diode protects the input circuit against ESD pulses.



**Figure 4** Input Circuit

A high signal at the required external small signal transistor pulls the input pin to ground. A logic supply current  $I_{IN}$  is flowing and the power DMOS switches on with a dedicated slope, which is optimized in terms of EMC emission.



**Figure 5** Switching a Load (resistive)

### 5.2 Output On-State Resistance

The on-state resistance  $R_{DS(ON)}$  depends on the supply voltage as well as the junction temperature  $T_j$ . **Figure 6** shows these dependencies for the typical on-state resistance. The voltage drop in reverse polarity mode is described in [Section 6.3](#).

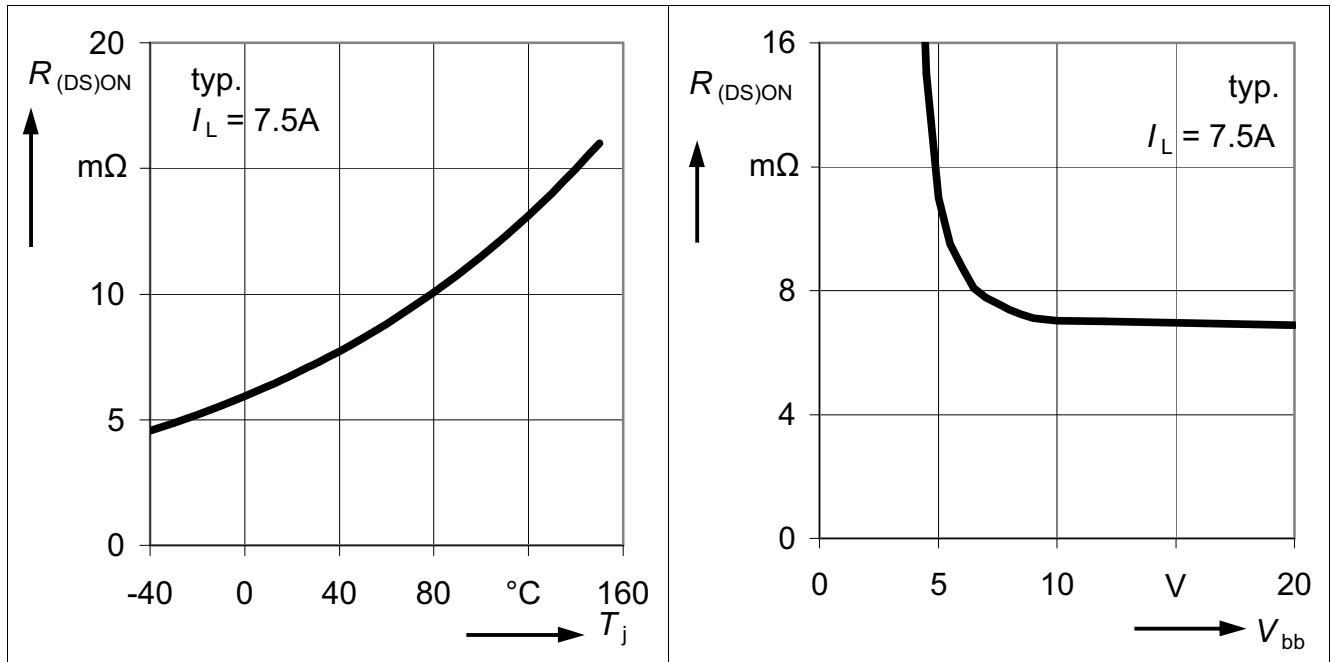


Figure 6 Typical On-State Resistance

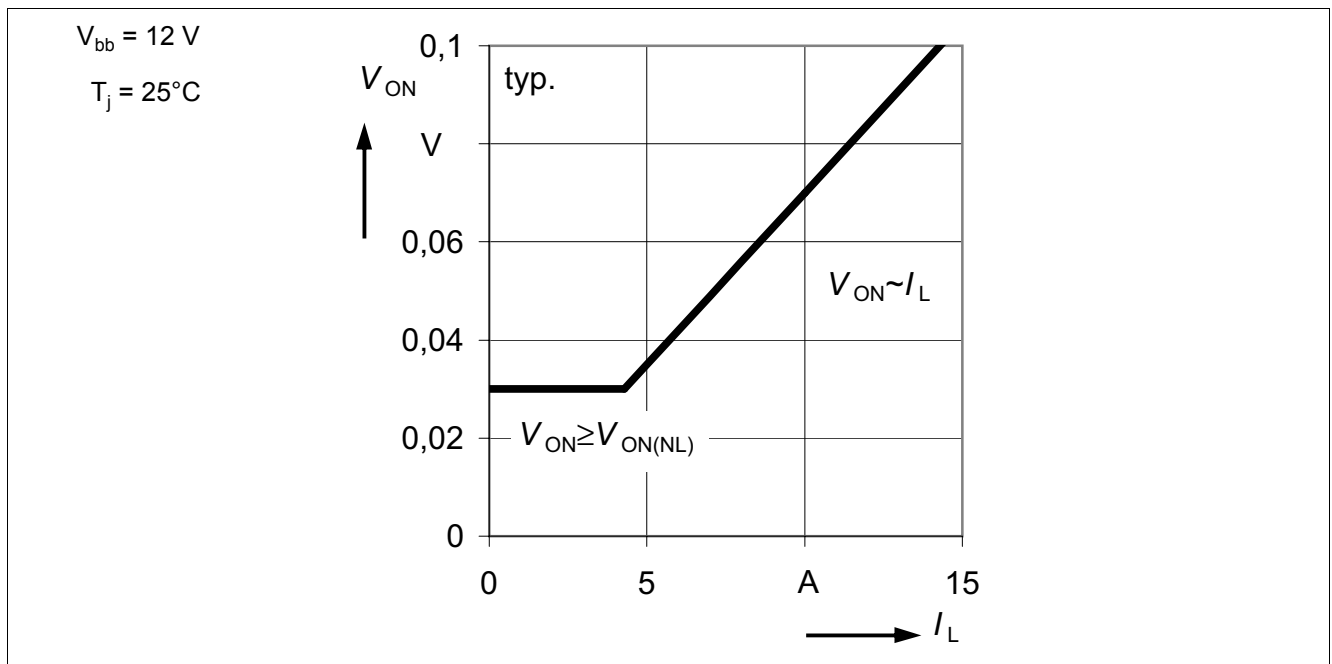


Figure 7 Typical Output Voltage Drop Limitation

### 5.3 Output Inductive Clamp

When switching off inductive loads, the output voltage  $V_{OUT}$  drops below ground potential due to the involved inductance ( $-di_L/dt = -v_L/L$ ;  $-V_{OUT} \cong -V_L$ ).



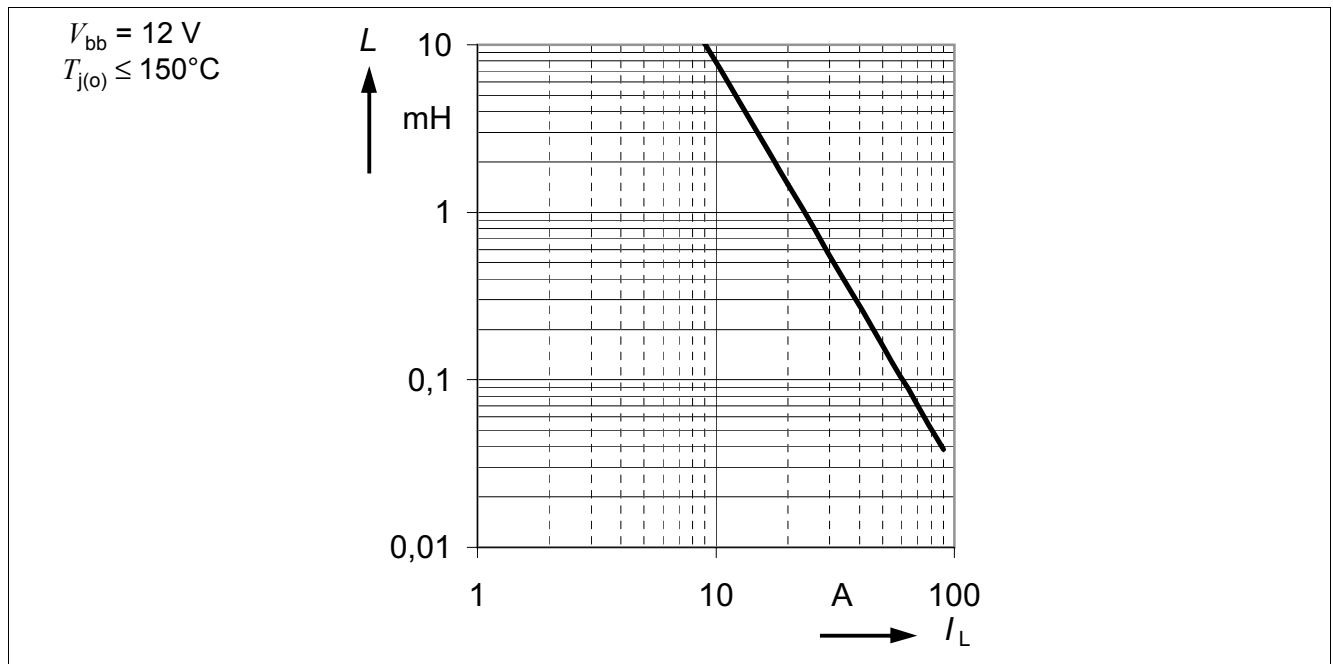


Figure 10 Maximum load inductance for single pulse,  $T_{j(0)} \leq 150^\circ\text{C}$ .

## 5.4 Electrical Characteristics

$V_{bb} = 12\text{ V}$ ,  $T_j = -40 \dots 150\text{ °C}$  (unless otherwise specified) Typical values are given at  $V_{bb} = 12\text{ V}$ ,  $T_j = 25\text{ °C}$

| Pos. | Parameter | Symbol | Limit Values |      |      | Unit | Conditions |
|------|-----------|--------|--------------|------|------|------|------------|
|      |           |        | Min.         | Typ. | Max. |      |            |

### General

|       |                                                                              |               |     |     |     |               |                       |
|-------|------------------------------------------------------------------------------|---------------|-----|-----|-----|---------------|-----------------------|
| 5.4.1 | Operating voltage <sup>1)</sup>                                              | $V_{bb(on)}$  | 5.5 | -   | 38  | V             | $V_{IN} = 0\text{ V}$ |
| 5.4.2 | Undervoltage shutdown <sup>2)</sup>                                          | $V_{bIN(u)}$  | -   | 2.5 | 3.5 | V             | $T_j = 25\text{ °C}$  |
| 5.4.3 | Undervoltage restart of charge pump                                          | $V_{bb(ucp)}$ | -   | 4   | 5.5 | V             | —                     |
| 5.4.4 | Operating current                                                            | $I_{IN}$      | -   | 1.4 | 2.2 | mA            | —                     |
| 5.4.5 | Stand-by current<br>$T_j = -40 \dots 120\text{ °C}$<br>$T_j = 150\text{ °C}$ | $I_{bb(OFF)}$ | -   | 3   | 6   | $\mu\text{A}$ | $I_{IN} = 0\text{ A}$ |
|       |                                                                              |               | -   | 6   | 14  |               |                       |
|       |                                                                              |               | -   | 6   | 14  |               |                       |

### Input characteristics

|       |                            |               |   |     |     |               |                                     |
|-------|----------------------------|---------------|---|-----|-----|---------------|-------------------------------------|
| 5.4.6 | Input current for turn-on  | $I_{IN(on)}$  | - | 1.4 | 2.2 | mA            | $V_{bIN} \geq V_{bb(ucp)} - V_{IN}$ |
| 5.4.7 | Input current for turn-off | $I_{IN(off)}$ | - | -   | 30  | $\mu\text{A}$ | —                                   |

### Output characteristics

|        |                                                                                                                                                                           |                |      |     |    |                  |                                                                                    |
|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|------|-----|----|------------------|------------------------------------------------------------------------------------|
| 5.4.8  | On-state resistance<br>$T_j = 25\text{ °C}$<br>$T_j = 150\text{ °C}$<br>$V_{bb} = 5.5\text{ V}$ , $T_j = 25\text{ °C}$<br>$V_{bb} = 5.5\text{ V}$ , $T_j = 150\text{ °C}$ | $R_{DS(ON)}$   | -    | 7   | -  | $\text{m}\Omega$ | $V_{IN} = 0\text{ V}$ , $I_L = 10\text{ A}$ ,<br>(Tab to pin 1, 2, 6 and 7)        |
|        |                                                                                                                                                                           |                | -    | 13  | 16 |                  |                                                                                    |
|        |                                                                                                                                                                           |                | -    | 9.5 | -  |                  |                                                                                    |
|        |                                                                                                                                                                           |                | -    | 17  | 22 |                  |                                                                                    |
|        |                                                                                                                                                                           |                | -    | 17  | 22 |                  |                                                                                    |
| 5.4.9  | Output voltage drop limitation at small load currents                                                                                                                     | $V_{ON(NL)}$   | -    | 30  | 60 | mV               | —                                                                                  |
| 5.4.10 | Nominal load current<br>(Tab to pin 1, 2, 6 and 7) <sup>3) 4)</sup>                                                                                                       | $I_{L(nom)}$   | 9.5  | 12  | -  | A                | $T_a = 85\text{ °C}$ ,<br>$V_{ON} \leq 0.5\text{ V}$ ,<br>$T_j \leq 150\text{ °C}$ |
|        | ISO load current<br>(Tab to pin 1, 2, 6 and 7) <sup>4)</sup>                                                                                                              | $I_{L(ISO)}$   | 37.5 | 48  | -  | A                | $T_c = 85\text{ °C}$ ,<br>$V_{ON} \leq 0.5\text{ V}$ ,<br>$T_j \leq 150\text{ °C}$ |
| 5.4.11 | Output clamp                                                                                                                                                              | $V_{ON(CL)}$   | 39   | 42  | -  | V                | $I_L = 40\text{ mA}$ ,<br>$T_j = 25\text{ °C}$                                     |
| 5.4.12 | Inverse current output voltage drop <sup>2) 5)</sup><br>(Tab to pin 1, 2, 6 and 7)<br>$T_j = 25\text{ °C}$<br>$T_j = 150\text{ °C}$                                       | $-V_{ON(inv)}$ | -    | 700 | -  | mV               | $I_L = -10\text{ A}$ ,<br>$R_{IS} = 1\text{ k}\Omega$                              |
|        |                                                                                                                                                                           |                | -    | 300 | -  |                  |                                                                                    |
|        |                                                                                                                                                                           |                | -    | 300 | -  |                  |                                                                                    |

### Timings

|        |                                |           |   |     |     |               |                           |
|--------|--------------------------------|-----------|---|-----|-----|---------------|---------------------------|
| 5.4.13 | Turn-on time to 90% $V_{OUT}$  | $t_{ON}$  | - | 300 | 550 | $\mu\text{s}$ | $R_L = 2.2\text{ }\Omega$ |
| 5.4.14 | Turn-off time to 10% $V_{OUT}$ | $t_{OFF}$ | - | 300 | 600 | $\mu\text{s}$ | $R_L = 2.2\text{ }\Omega$ |

$V_{bb} = 12\text{ V}$ ,  $T_j = -40 \dots 150\text{ °C}$  (unless otherwise specified) Typical values are given at  $V_{bb} = 12\text{ V}$ ,  $T_j = 25\text{ °C}$

| Pos.   | Parameter                                           | Symbol           | Limit Values |      |      | Unit       | Conditions                                                       |
|--------|-----------------------------------------------------|------------------|--------------|------|------|------------|------------------------------------------------------------------|
|        |                                                     |                  | Min.         | Typ. | Max. |            |                                                                  |
| 5.4.15 | Turn-on delay after inverse operation <sup>2)</sup> | $t_{d(inv)}$     | -            | 1    | -    | ms         | $V_{bb} > V_{OUT}$ ,<br>$V_{IN(inv)} = V_{IN(fwd)} = 0\text{ V}$ |
| 5.4.16 | Slew rate On<br>25% to 50% $V_{OUT}$                | $(dV/dt)_{ON}$   | -            | 0.2  | 0.35 | V/ $\mu$ s | $R_L = 2.2\text{ }\Omega$                                        |
| 5.4.17 | Slew rate Off<br>50% to 25% $V_{OUT}$               | $-(dV/dt)_{OFF}$ | -            | 0.2  | 0.45 | V/ $\mu$ s | $R_L = 2.2\text{ }\Omega$                                        |

- 1) Please mind the limitations of the embedded protection functions. See [Chapter 4.1](#) and [Chapter 6](#) for details.
- 2) Not subject to production test, specified by design
- 3) Device mounted on PCB (50 mm x 50 mm x 1.5mm epoxy, FR4) with 6 cm<sup>2</sup> copper heatsinking area (one layer, 70  $\mu$ m thick) for  $V_{bb}$  connection. PCB is vertical without blown air.
- 4) Not subject to production test, parameters are calculated from  $R_{DS(ON)}$  and  $R_{th}$
- 5) During inverse operation ( $I_L < 0\text{ A}$ ,  $V_{bIN} > 0\text{ V}$ ), a current through the intrinsic body diode causing a voltage drop of  $V_{ON(inv)}$  results in a delayed switch on with a time delay  $t_{d(inv)}$  after the transition from inverse to forward operation. A sense current  $I_{IS(fault)}$  can be provided by the pin IS until standard forward operation is reached.

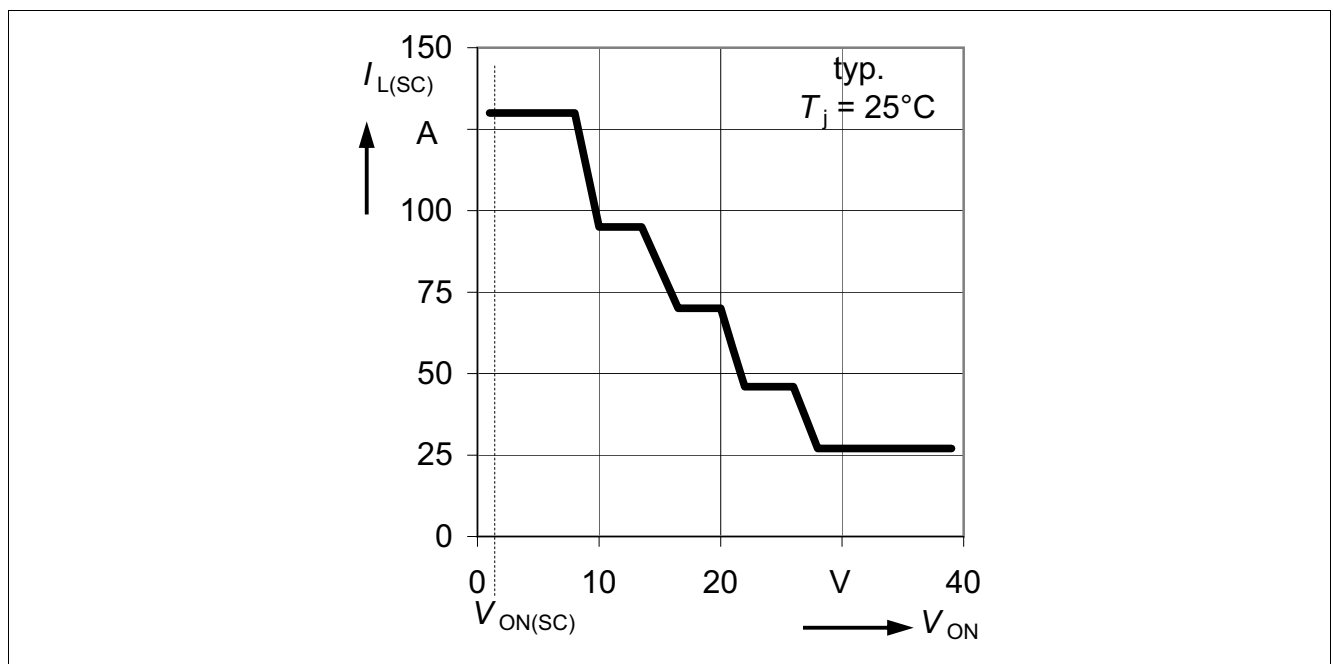
*Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature.  
Typical values show the typical parameters expected from manufacturing.*

## 6 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are neither designed for continuous nor repetitive operation.

### 6.1 Over-Load Protection

The load current  $I_L$  is limited by the device itself in case of over-load or short circuit to ground. There are multiple steps of current limitation  $I_{L(SC)}$  which are selected automatically depending on the voltage drop  $V_{ON}$  across the power DMOS. Please note that the voltage at the OUT pin is  $V_{bb} - V_{ON}$ . **Figure 11** shows the dependency for a typical device.



**Figure 11 Typical Current Limitation**

Depending on the severity of the short condition as well as on the battery voltage the resulting voltage drop across the device varies.

Whenever the resulting voltage drop  $V_{ON}$  exceeds the short circuit detection threshold  $V_{ON(SC)}$ , the device will switch off immediately and latch until being reset via the input. The  $V_{ON(SC)}$  detection functionality is activated, when  $V_{bIN} > 10$  V typ. and the blanking time  $t_{d(SC1)}$  expired after switch on.

In the event that either the short circuit detection via  $V_{ON(SC)}$  is not activated or that the on chip temperature sensor senses over-temperature before the blanking time  $t_{d(SC1)}$  expired, the device switches off resulting from over-temperature detection. After cooling down with thermal hysteresis, the device switches on again. The device will react as during normal switch on triggered by the input signal. Please refer to **Figure 12** and **Figure 19** for details.

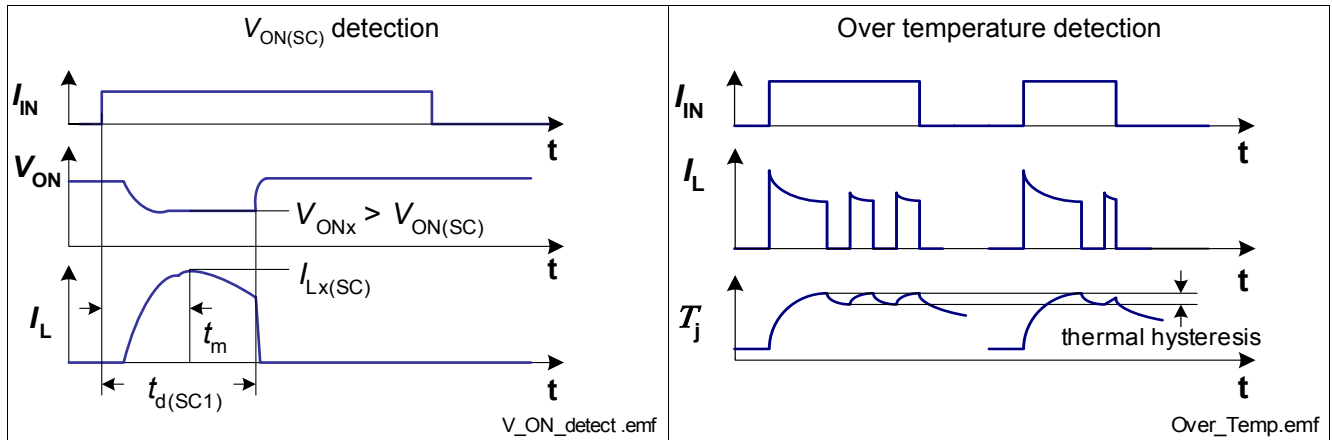


Figure 12 Overload Behavior

## 6.2 Short circuit impedance

The capability to handle single short circuit events depends on the battery voltage as well as on the primary and secondary short impedance. **Figure 13** outlines allowable combinations for a single short circuit event of maximum, secondary inductance for given secondary resistance.

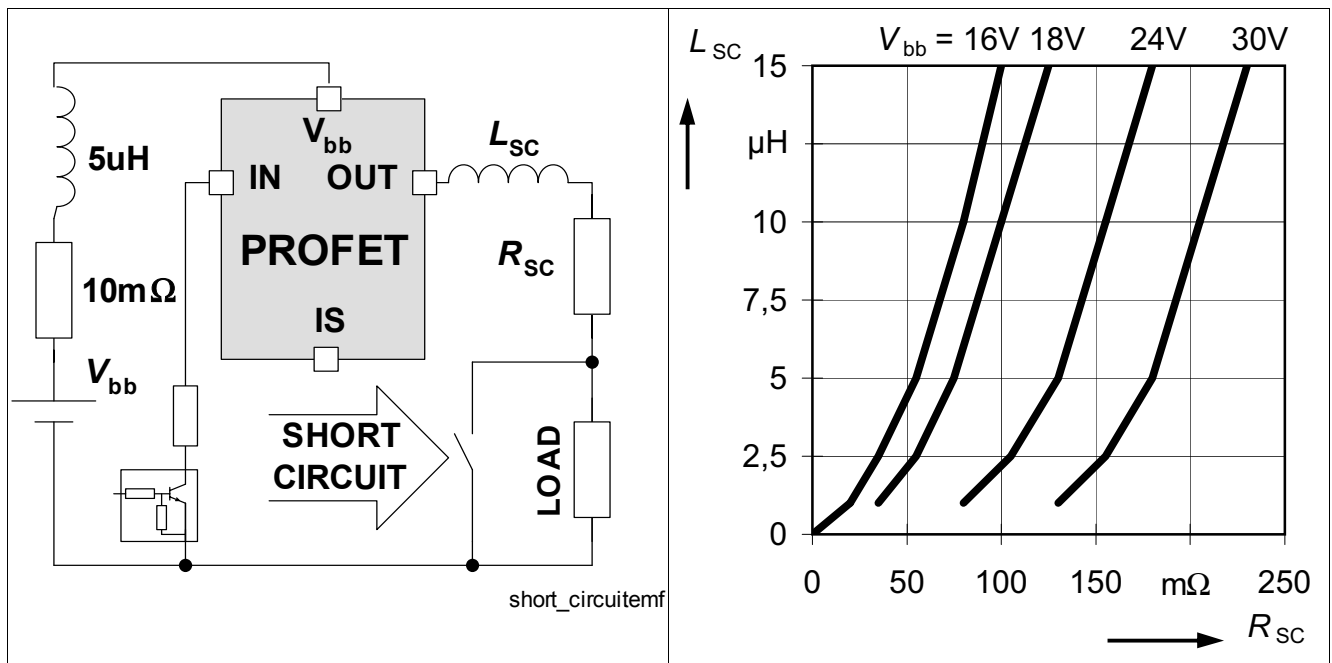
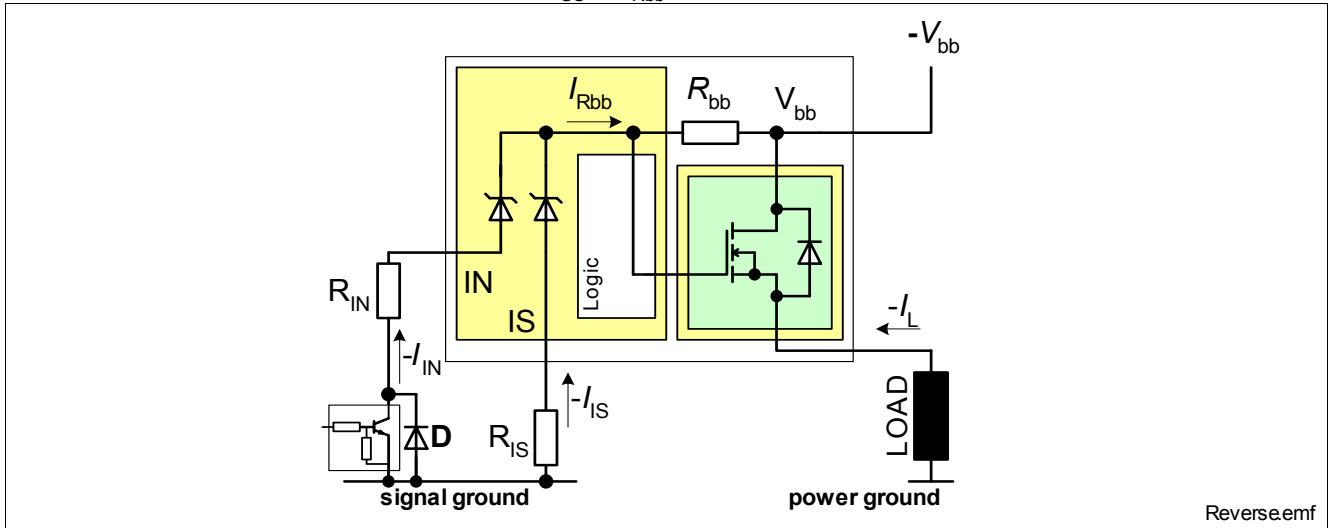


Figure 13 Short circuit

### 6.3 Reverse Polarity Protection - Reversafe®

The device can not block a current flow in reverse polarity condition. In order to minimize power dissipation, the device offers Reversafe® functionality. In reverse polarity condition the channel will be switched on provided a sufficient gate to source voltage is generated  $V_{GS} \approx V_{Rbb}$ . Please refer to [Figure 14](#) for details.



**Figure 14** Reverse battery protection

Additional power is dissipated by the integrated  $R_{bb}$  resistor. Use following formula for estimation of overall power dissipation  $P_{diss(rev)}$  in reverse polarity mode.

$$P_{diss(rev)} \approx R_{ON(rev)} \cdot I_L^2 + R_{bb} \cdot I_{Rbb}^2$$

For reverse battery voltages up to  $V_{bb} < 16\text{ V}$  the pin IN or the pin IS should be low ohmic connected to signal ground. This can be achieved e.g. by using a small signal diode D in parallel to the input switch or by using a small signal MOSFET driver. For reverse battery voltages higher then  $V_{bb} = 16\text{ V}$  an additional resistor  $R_{IN}$  is recommended. The overall current through  $R_{bb}$  should not be above 80 mA.

$$\frac{1}{R_{IN}} + \frac{1}{R_{IS}} = \frac{0.08\text{ A}}{|V_{bb}| - 12\text{ V}}$$

*Note: No protection mechanism is active during reverse polarity. The IC logic is not functional.*

## 6.4 Over-Voltage Protection

Beside the output clamp for the power stage as described in [Section 5.3](#) there is a clamp mechanism implemented for all logic pins. See [Figure 15](#) for details.

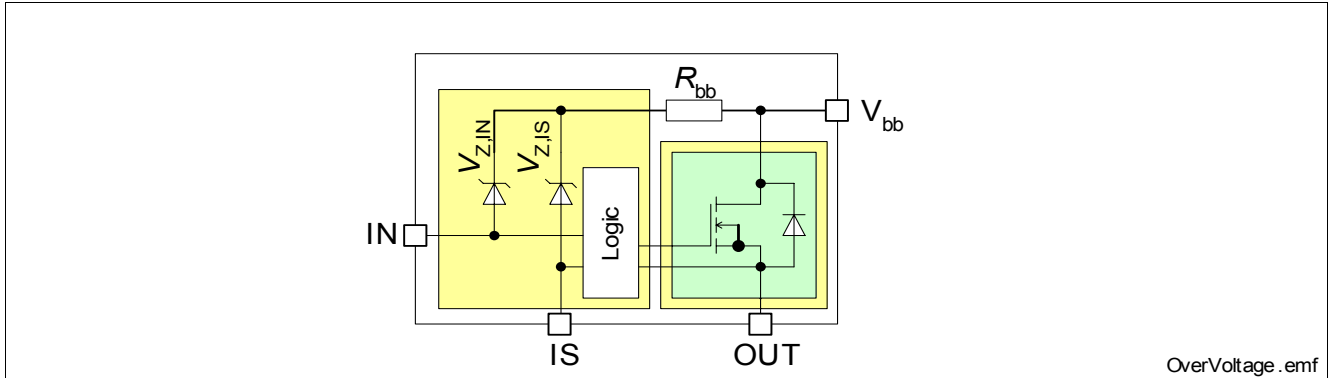


Figure 15 Over-Voltage Protection

## 6.5 Loss of Ground Protection

In case of complete loss of the device ground connections the BTS50080-1TMA securely changes to or remains in off state.

## 6.6 Loss of $V_{bb}$ Protection

In case of complete loss of  $V_{bb}$  the BTS50080-1TMA remains in off state.

In case of loss of  $V_{bb}$  connection with charged inductive loads a current path with load current capability has to be provided, to demagnetize the charged inductances. It is recommended to use a diode, a Z-diode, or a varistor ( $V_{ZL} + V_D < 30 \text{ V}$  or  $V_{Zb} + V_D < 16 \text{ V}$  if  $R_{IN} = 0$ ). For higher clamp voltages currents through IN and IS have to be limited to  $\sim 120 \text{ mA}$ . Please refer to [Figure 16](#) for details.

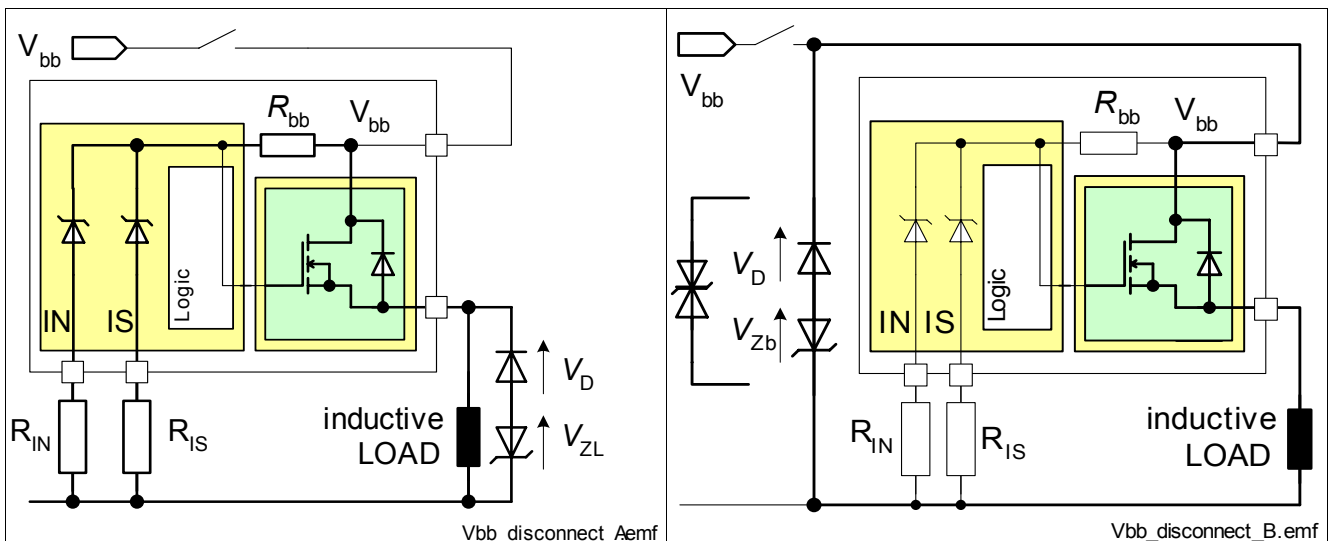


Figure 16 Loss of  $V_{bb}$

## 6.7 Electrical Characteristics

$V_{bb} = 12\text{ V}$ ,  $T_j = -40 \dots 150\text{ °C}$  (unless otherwise specified) Typical values are given at  $V_{bb} = 12\text{ V}$ ,  $T_j = 25\text{ °C}$

| Pos. | Parameter | Symbol | Limit Values |      |      | Unit | Conditions |
|------|-----------|--------|--------------|------|------|------|------------|
|      |           |        | Min.         | Typ. | Max. |      |            |

### Over-Load Protection

|       |                                                                                                                      |               |              |                   |               |                    |                                                                                            |
|-------|----------------------------------------------------------------------------------------------------------------------|---------------|--------------|-------------------|---------------|--------------------|--------------------------------------------------------------------------------------------|
| 6.7.1 | Load current limitation <sup>1) 2)</sup><br>$T_j = -40\text{ °C}$<br>$T_j = +25\text{ °C}$<br>$T_j = +150\text{ °C}$ | $I_{L6(SC)}$  | -<br>-<br>90 | 140<br>130<br>120 | 170<br>-<br>- | A                  | $V_{ON} = 6\text{ V}$ ,<br>(Tab to pin 1, 2, 6 and 7)                                      |
| 6.7.2 | Load current limitation <sup>2)</sup><br>$T_j = -40\text{ °C}$<br>$T_j = +25\text{ °C}$<br>$T_j = +150\text{ °C}$    | $I_{L12(SC)}$ | -<br>-<br>55 | 105<br>95<br>85   | 130<br>-<br>- | A                  | $V_{ON} = 12\text{ V}$ ,<br>$t_m = 170\text{ }\mu\text{s}$ ,<br>(Tab to pin 1, 2, 6 and 7) |
| 6.7.3 | Load current limitation <sup>1) 2)</sup><br>$T_j = -40\text{ °C}$<br>$T_j = +25\text{ °C}$<br>$T_j = +150\text{ °C}$ | $I_{L18(SC)}$ | -<br>-<br>45 | 75<br>70<br>65    | 100<br>-<br>- | A                  | $V_{ON} = 18\text{ V}$ ,<br>(Tab to pin 1, 2, 6 and 7)                                     |
| 6.7.4 | Load current limitation <sup>2)</sup><br>$T_j = -40\text{ °C}$<br>$T_j = +25\text{ °C}$<br>$T_j = +150\text{ °C}$    | $I_{L24(SC)}$ | -<br>-<br>28 | 47<br>46<br>45    | 70<br>-<br>-  | A                  | $V_{ON} = 24\text{ V}$ ,<br>$t_m = 170\text{ }\mu\text{s}$ ,<br>(Tab to pin 1, 2, 6 and 7) |
| 6.7.5 | Load current limitation <sup>1) 2)</sup><br>$T_j = -40\text{ °C}$<br>$T_j = +25\text{ °C}$<br>$T_j = +150\text{ °C}$ | $I_{L36(SC)}$ | -<br>-<br>15 | 27<br>27<br>27    | 40<br>-<br>-  | A                  | $V_{ON} = 36\text{ V}$ ,<br>(Tab to pin 1, 2, 6 and 7)                                     |
| 6.7.6 | Short circuit shutdown detection voltage <sup>1)</sup>                                                               | $V_{ON(SC)}$  | 2.5          | 3.5               | 4.5           | V                  | $V_{BIN} > 10\text{ V typ.}$ ,<br>$T_j = 25\text{ °C}$                                     |
| 6.7.7 | Short circuit shutdown delay after input current pos. slope <sup>3)</sup>                                            | $t_{d(SC1)}$  | 350          | 650               | 1200          | $\mu\text{s}$      | $V_{ON} > V_{ON(SC)}$                                                                      |
| 6.7.8 | Thermal shut down temperature                                                                                        | $T_{j(SC)}$   | 150          | 175 <sub>1)</sub> | -             | $^{\circ}\text{C}$ | -                                                                                          |
| 6.7.9 | Thermal hysteresis <sup>1)</sup>                                                                                     | $\Delta T_j$  | -            | 10                | -             | K                  | -                                                                                          |

### Reverse Polarity

|        |                                                                                                                                                                                                                                                                                     |               |                  |                      |                    |            |                                                                                                                  |
|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|------------------|----------------------|--------------------|------------|------------------------------------------------------------------------------------------------------------------|
| 6.7.10 | On-State resistance in case of reverse polarity<br>$V_{bb} = -8\text{ V}$ , $T_j = 25\text{ °C}$ <sup>1)</sup><br>$V_{bb} = -8\text{ V}$ , $T_j = 150\text{ °C}$ <sup>1)</sup><br>$V_{bb} = -12\text{ V}$ , $T_j = 25\text{ °C}$<br>$V_{bb} = -12\text{ V}$ , $T_j = 150\text{ °C}$ | $R_{ON(rev)}$ | -<br>-<br>-<br>- | 8.5<br>13<br>8<br>13 | -<br>18<br>-<br>19 | m $\Omega$ | $V_{IN} = 0\text{ V}$ ,<br>$I_L = -10\text{ A}$ ,<br>$R_{IS} = 1\text{ k}\Omega$ ,<br>(pin 1, 2, 6 and 7 to TAB) |
| 6.7.11 | Integrated resistor in $V_{bb}$ line                                                                                                                                                                                                                                                | $R_{bb}$      | -                | 100                  | 150                | $\Omega$   | $T_j = 25\text{ °C}$                                                                                             |

### Over-Voltage

|        |                         |            |    |    |   |   |                         |
|--------|-------------------------|------------|----|----|---|---|-------------------------|
| 6.7.12 | Over-voltage protection | $V_Z$      |    |    |   | V | $I_{bb} = 15\text{ mA}$ |
|        | Input pin               | $V_{Z,IN}$ | 63 | 67 | - | V |                         |
|        | Sense pin               | $V_{Z,IS}$ | 63 | 67 | - | V |                         |

1) Not subject to production test, specified by design

- 2) Short circuit current limit for max. duration of  $t_{d(SC1)}$ , prior to shutdown, see also [Figure 12](#).
- 3) min. value valid only if input "off-signal" time exceeds 30  $\mu$ s

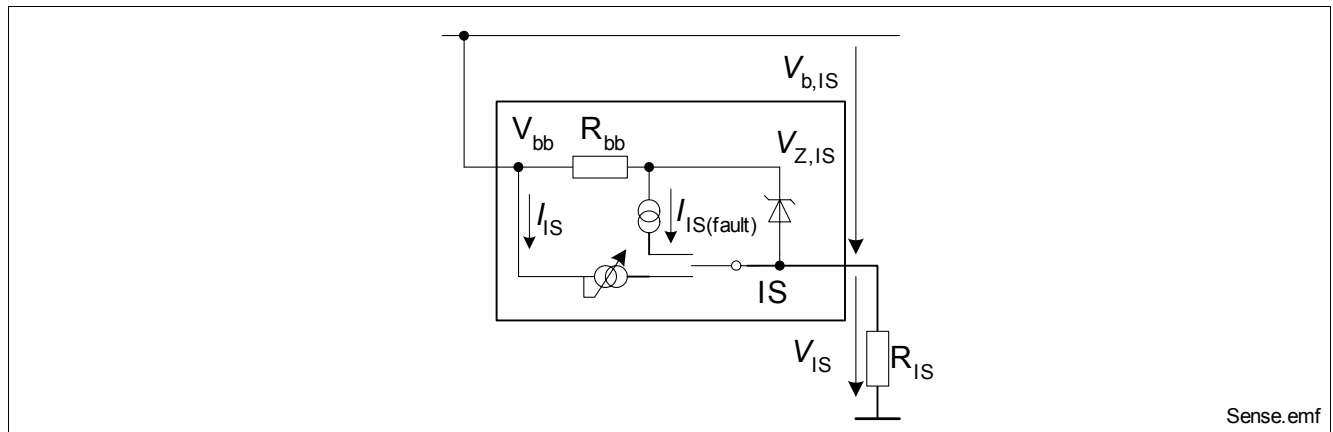
## 7 Diagnosis

For diagnosis purpose, the BTS50080-1TMA provides an IntelliSense signal at the pin IS.

The pin IS provides during normal operation a sense current, which is proportional to the load current as long as  $V_{bIS} > 5\text{ V}$ . The ratio of the output current is defined as  $k_{ILIS} = I_L / I_{IS}$ . During switch-on no current is provided, until the forward voltage drops below  $V_{ON} < 1\text{ V typ.}$  The output sense current is limited to  $I_{IS(lim)}$ .

The pin IS provides in case of any fault conditions a defined fault current  $I_{IS(fault)}$  as long as  $V_{bIS} > 8\text{ V}$ . Fault conditions are over-current ( $V_{ON} > 1\text{ V typ.}$ ), current limit or over-temperature switch off.

The pin IS provides no current during open load in ON and de-energisation of inductive loads.



**Figure 17 Block Diagram: Diagnosis**

**Table 1 Truth Table**

| Parameter                 | Input Current Level                | Output Level         | Current Sense $I_{IS}$                                       |
|---------------------------|------------------------------------|----------------------|--------------------------------------------------------------|
| Normal operation          | L <sup>1)</sup><br>H <sup>1)</sup> | L<br>H               | $\approx 0$ ( $I_{IS(LL)}$ )<br>nominal                      |
| Overload                  | L<br>H                             | L<br>H               | $\approx 0$ ( $I_{IS(LL)}$ )<br>$I_{IS(fault)}$              |
| Short circuit to GND      | L<br>H                             | L<br>L               | $\approx 0$ ( $I_{IS(LL)}$ )<br>$I_{IS(fault)}$              |
| Overtemperature           | L<br>H                             | L<br>L               | $\approx 0$ ( $I_{IS(LL)}$ )<br>$I_{IS(fault)}$              |
| Short circuit to $V_{bb}$ | L<br>H                             | H<br>H               | $\approx 0$ ( $I_{IS(LL)}$ )<br>< nominal <sup>2)</sup>      |
| Open load                 | L<br>H                             | Z <sup>1)</sup><br>H | $\approx 0$ ( $I_{IS(LL)}$ )<br>$\approx 0$ ( $I_{IS(LH)}$ ) |

1) H = "High" Level, L = "Low" Level, Z = high impedance, potential depends on external circuit

2) Low ohmic short to  $V_{bb}$  may reduce the output current  $I_L$  and therefore also the sense current  $I_{IS}$ .

The accuracy of the provided current sense ratio ( $k_{ILIS} = I_L / I_{IS}$ ) depends on the load current. Please refer to [Figure 18](#) for details. A typical resistor  $R_{IS}$  of 1 kΩ is recommended.

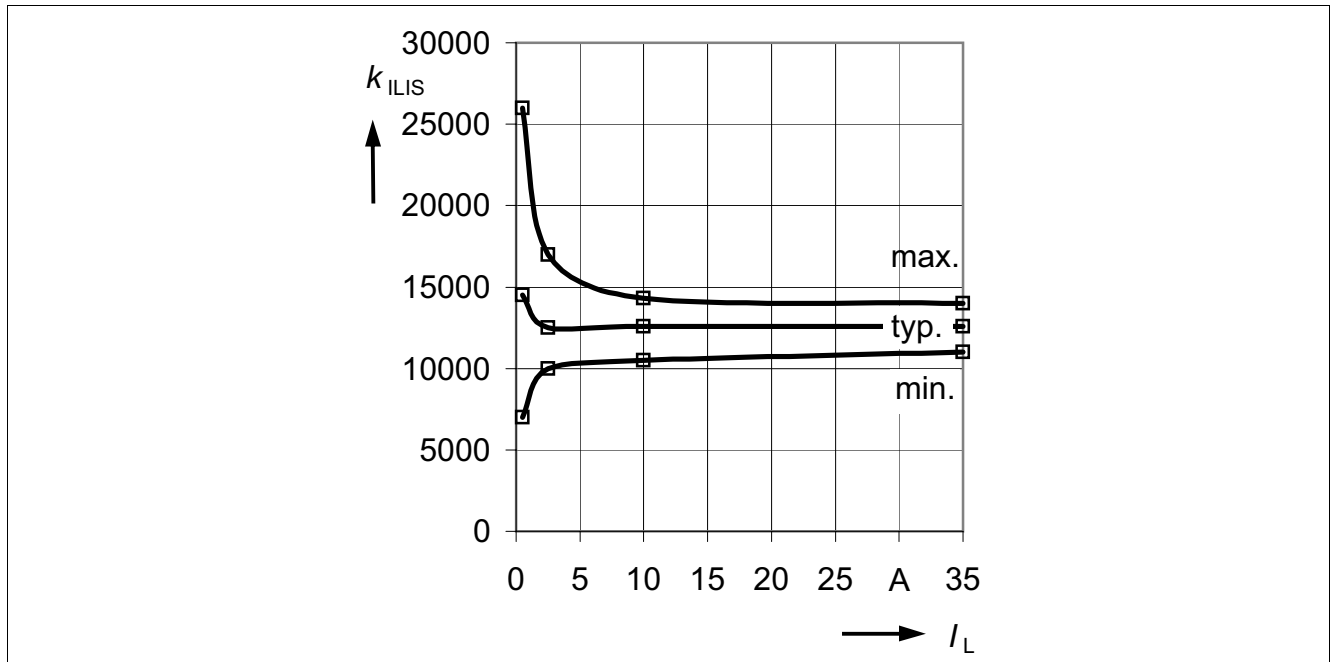


Figure 18 Current sense ratio  $k_{ILIS}$ <sup>1)</sup>

Details about timings between the diagnosis signal  $I_{IS}$ , the forward voltage drop  $V_{ON}$  and the load current  $I_L$  in ON-state can be found in [Figure 19](#).

*Note: During operation at low load current and at activated forward voltage drop limitation the “two level control” of  $V_{ON(NL)}$  can cause a sense current ripple synchronous to the “two level control” of  $V_{ON(NL)}$ . The ripple frequency increases at reduced load currents.*

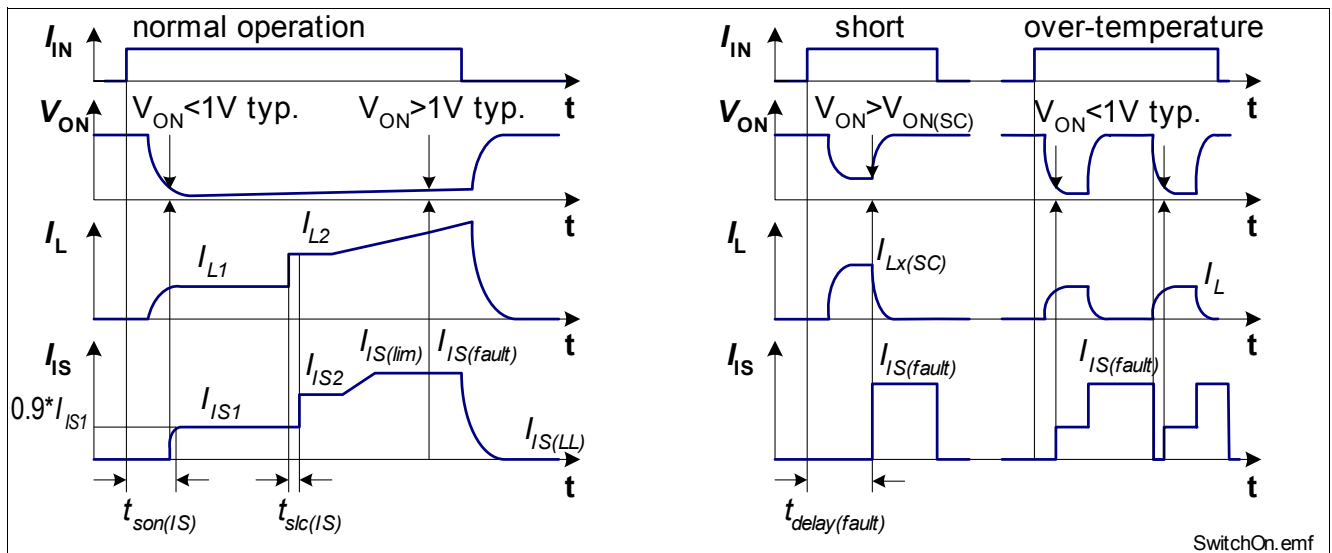


Figure 19 Timing of Diagnosis Signal in ON-state

1) The curves show the behavior based on characterization data. The marked points are guaranteed in this Datasheet in [Section 7.1](#) (Position 7.1.1).

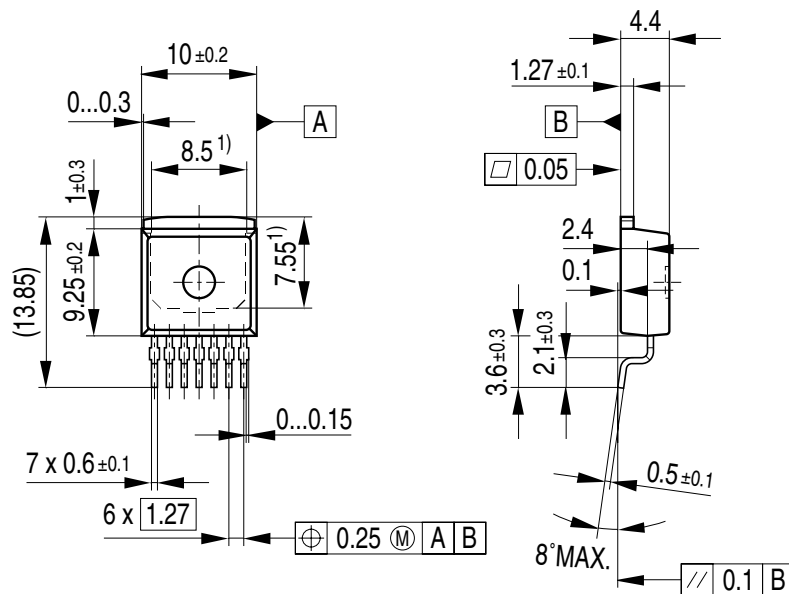
## 7.1 Electrical Characteristics

$V_{bb} = 12\text{ V}$ ,  $T_j = -40 \dots 150\text{ °C}$  (unless otherwise specified) Typical values are given at  $V_{bb} = 12\text{ V}$ ,  $T_j = 25\text{ °C}$

| Pos.               | Parameter                                                                                                                                                                                                                   | Symbol             | Limit Values |      |      | Unit | Conditions                                        |
|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|--------------|------|------|------|---------------------------------------------------|
|                    |                                                                                                                                                                                                                             |                    | Min.         | Typ. | Max. |      |                                                   |
| Load Current Sense |                                                                                                                                                                                                                             |                    |              |      |      |      |                                                   |
| 7.1.1              | Current sense ratio, static on-condition<br><br>$I_L = 35\text{ A}$<br>$I_L = 10\text{ A}$<br>$I_L = 2.5\text{ A}$<br>$I_L = 0.5\text{ A}$<br><br>$I_{IN} = 0$ (e.g. during de energizing of inductive loads) <sup>1)</sup> | $k_{ILIS}$         | -            | 12.5 | -    | k    | $V_{IN} = 0\text{ V}$ ,<br>$I_{IS} < I_{IS(lim)}$ |
|                    |                                                                                                                                                                                                                             |                    | 11           | 12.6 | 14   |      |                                                   |
|                    |                                                                                                                                                                                                                             |                    | 10.5         | 12.6 | 14.3 |      |                                                   |
|                    |                                                                                                                                                                                                                             |                    | 10           | 12.5 | 17   |      |                                                   |
|                    |                                                                                                                                                                                                                             |                    | 7            | 14.5 | 26   |      |                                                   |
|                    |                                                                                                                                                                                                                             |                    | disabled     |      |      | -    | -                                                 |
| 7.1.2              | Sense saturation current <sup>1)</sup>                                                                                                                                                                                      | $I_{IS(lim)}$      | 4.0          | 6    | 7.5  | mA   | $V_{ON} < 1\text{ V}$ , typ.                      |
| 7.1.3              | Sense current under fault conditions                                                                                                                                                                                        | $I_{IS(fault)}$    | 4.0          | 5.2  | 7.5  | mA   | $V_{ON} > 1\text{ V}$ , typ.                      |
| 7.1.4              | Current sense leakage current                                                                                                                                                                                               | $I_{IS(LL)}$       | —            | 0.1  | 0.5  | μA   | $I_{IN} = 0$                                      |
| 7.1.5              | Current sense offset current                                                                                                                                                                                                | $I_{IS(LH)}$       | —            | 0.1  | 1    | μA   | $V_{IN} = 0$ , $I_L \leq 0$                       |
| 7.1.6              | Current sense settling time to 90%<br>$I_{IS\_stat.}$ <sup>1)</sup>                                                                                                                                                         | $t_{son(IS)}$      | —            | 250  | 500  | μs   | $I_L = 0 \rightarrow 20\text{ A}$                 |
| 7.1.7              | Current sense settling time to 90%<br>$I_{IS\_stat.}$ <sup>1)</sup>                                                                                                                                                         | $t_{slc(IS)}$      | —            | 50   | 100  | μs   | $I_L = 10 \rightarrow 20\text{ A}$                |
| 7.1.8              | Fault-Sense signal delay after input current positive slope                                                                                                                                                                 | $t_{delay(fault)}$ | 350          | 650  | 1200 | μs   | $V_{ON} > 1\text{ V}$ , typ.                      |

1) Not subject to production test, specified by design

## 8 Package Outlines



<sup>1)</sup> Typical  
Metal surface min. X = 7.25, Y = 6.9  
All metal surfaces tin plated, except area of cut.

Figure 20 PG-T0220-7-4

### Green Product

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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Dimensions in mm

## 9 Revision History

| Version               | Date       | Changes                      |
|-----------------------|------------|------------------------------|
| Datasheet<br>Rev. 1.0 | 2008-01-21 | Initial version of datasheet |

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