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January 2015

# J111 / J112 / J113 / MMBFJ111 / MMBFJ112 / MMBFJ113
# N-Channel Switch

## Features

- This device is designed for low level analog switching, sample and hold circuits and chopper stabilized amplifiers.
- Sourced from process 51
- Source & Drain are interchangeable.

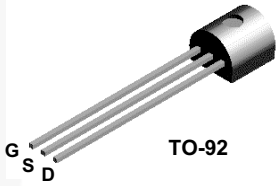



**Figure 1. J111 / J112 / J113 Device Package**

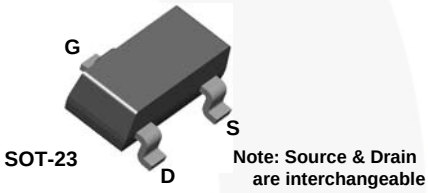



**Figure 2. MMBFJ111 / MMBFJ112 / MMBFJ113 Device Package**

## Ordering Information

| Part Number | Top Mark | Package | Packing Method |
|---|---|---|---|
| J111 | J111 | TO-92 3L | Bulk |
| J111_D26Z | J111 | TO-92 3L | Tape and Reel |
| J111_D74Z | J111 | TO-92 3L | Ammo |
| J112 | J112 | TO-92 3L | Bulk |
| J112_D26Z | J112 | TO-92 3L | Tape and Reel |
| J112_D27Z | J112 | TO-92 3L | Tape and Reel |
| J112_D74Z | J112 | TO-92 3L | Ammo |
| J113 | J113 | TO-92 3L | Bulk |
| J113_D74Z | J113 | TO-92 3L | Ammo |
| J113_D75Z | J113 | TO-92 3L | Ammo |
| MMBFJ111 | 6P | SOT-23 3L | Tape and Reel |
| MMBFJ112 | 6R | SOT-23 3L | Tape and Reel |
| MMBFJ113 | 6S | SOT-23 3L | Tape and Reel |

## Absolute Maximum Ratings[1], [2]

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A$ = 25°C unless otherwise noted.

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DG}$ | Drain-Gate Voltage | 35 | V |
| $V_{GS}$ | Gate-Source Voltage | -35 | V |
| $I_{GF}$ | Forward Gate Current | 50 | mA |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | -55 to 150 | °C |

**Notes:**

1. These ratings are based on a maximum junction temperature of 150°C.
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

## Thermal Characteristics

Values are at $T_A$ = 25°C unless otherwise noted.

| Symbol | Parameter | Max. | | Unit |
|---|---|---|---|---|
| | | J111 / J112 / J113[3] | MMBFJ111 / MMBFJ112 / MMBFJ113[4] | |
| $P_D$ | Total Device Dissipation | 625 | 350 | mW |
| | Derate Above 25°C | 5.0 | 2.8 | mW/°C |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 125 | | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | 200 | 357 | °C/W |

**Notes:**

3. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.
4. Device mounted on FR-4 PCB 36mm × 18mm × 1.5mm; mounting pad for the collector lead minimum 6cm$^2$.

## Electrical Characteristics

Values are at $T_A$ = 25°C unless otherwise noted.

| Symbol | Parameter | Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $V_{(BR)GSS}$ | Gate-Source Breakdown Voltage | $I_G$ = -1.0 µA, $V_{DS}$ = 0 | | -35 | | V |
| $I_{GSS}$ | Gate Reverse Current | $V_{GS}$ = -15 V, $V_{DS}$ = 0 | | | -1.0 | nA |
| $V_{GS}$(off) | Gate-Source Cut-Off Voltage | $V_{DS}$ = 15 V, $I_D$ = 1.0 µA | **111** | -3.0 | -10.0 | V |
| | | | **112** | -1.0 | -5.0 | |
| | | | **113** | -0.5 | -3.0 | |
| $I_D$(off) | Drain Cutoff Leakage Current | $V_{DS}$ = 5.0 V, $V_{GS}$ = -10 V | | | 1.0 | nA |
| **On Characteristics** | | | | | | |
| $I_{DSS}$ | Zero-Gate Voltage Drain Current[5] | $V_{DS}$ = 15 V, $V_{GS}$ = 0 | **111** | 20 | | mA |
| | | | **112** | 5.0 | | |
| | | | **113** | 2.0 | | |
| $r_{DS}$(on) | Drain-Source On Resistance | $V_{DS}$ ≤ 0.1 V, $V_{GS}$ = 0 | **111** | | 30 | Ω |
| | | | **112** | | 50 | |
| | | | **113** | | 100 | |
| **Small Signal Characteristics** | | | | | | |
| $C_{dg}$(on)<br>$C_{sg}$(on) | Drain-Gate &Source-Gate On Capacitance | $V_{DS}$ = 0, $V_{GS}$ = 0, f = 1.0 MHz | | | 28 | pF |
| $C_{dg}$(off) | Drain-Gate Off Capacitance | $V_{DS}$ = 0, $V_{GS}$ = -10 V, f = 1.0 MHz | | | 5.0 | pF |
| $C_{sg}$(off) | Source-Gate Off Capacitance | $V_{DS}$ = 0, $V_{GS}$ = -10 V, f = 1.0 MHz | | | 5.0 | pF |

**Note:**

5. Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2%.

## Typical Performance Characteristics

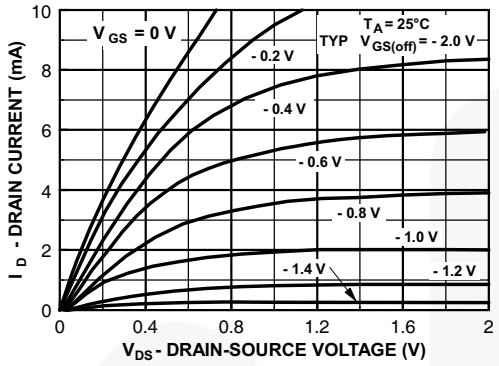



**Figure 3. Common Drain-Source**

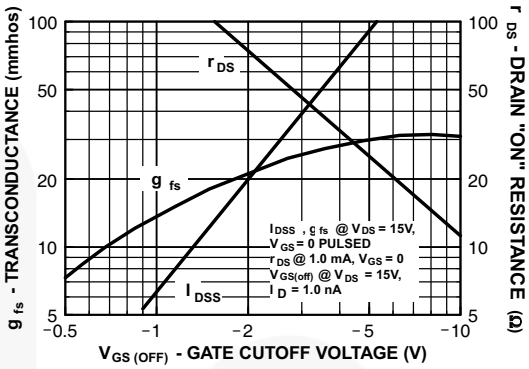



**Figure 4. Parameter Interactions**

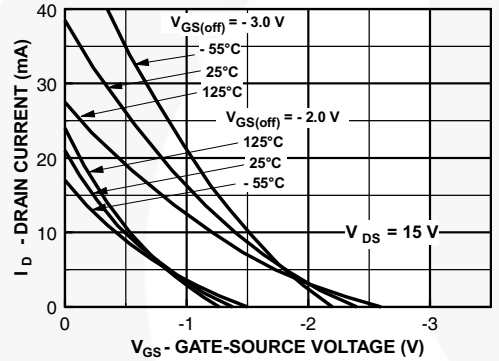



**Figure 5. Transfer Characteristics**

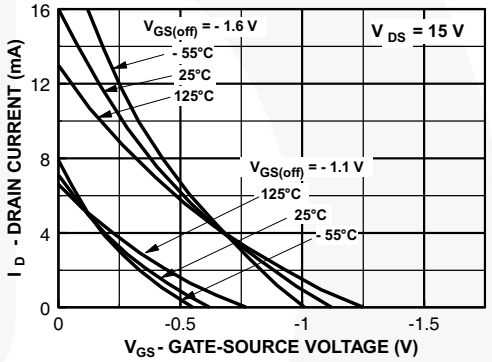



**Figure 6. Transfer Characteristics**

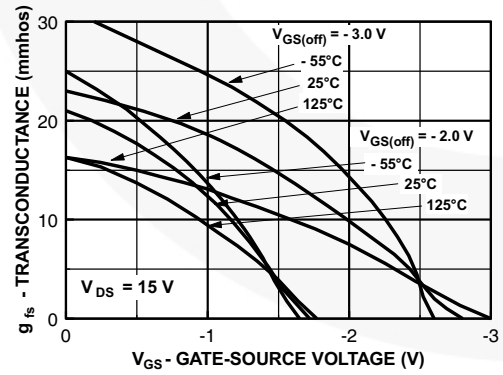



**Figure 7. Transfer Characteristics**

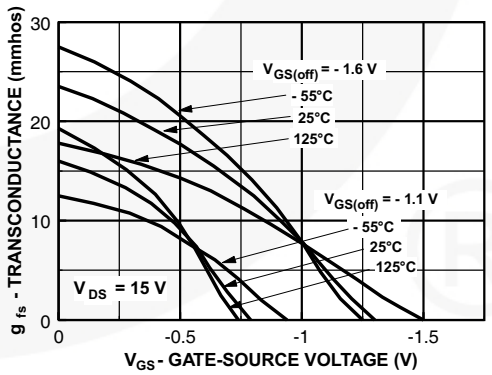



**Figure 8. Transfer Characteristics**

## Typical Performance Characteristics (Continued)

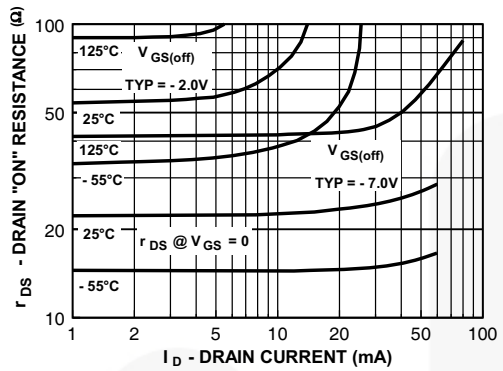



**Figure 9. On Resistance vs. Drain Current**

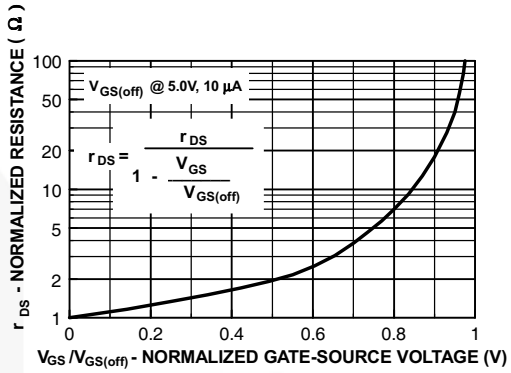



**Figure 10. Normalized Drain Resistance vs. Bias Voltage**

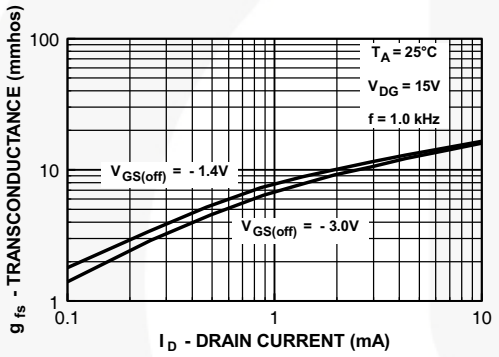



**Figure 11. Transconductance vs. Drain Current**

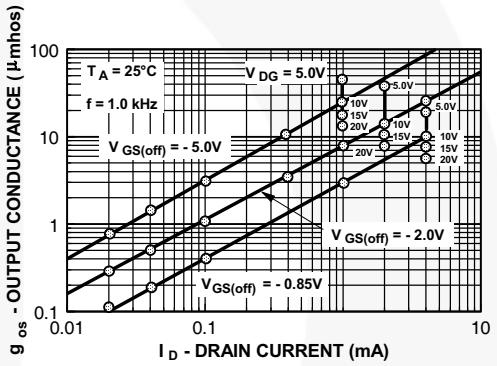



**Figure 12. Output Conductance vs. Drain Current**

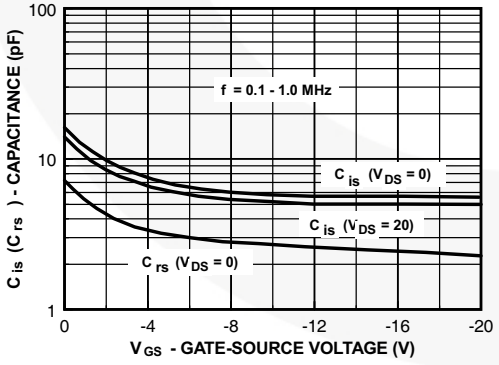



**Figure 13. Capacitance vs. Voltage**

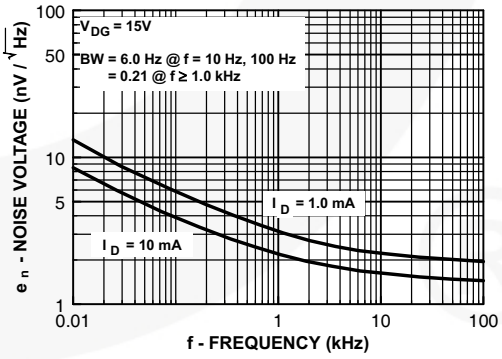



**Figure 14. Noise Voltage vs. Frequency**

## Typical Performance Characteristics (Continued)

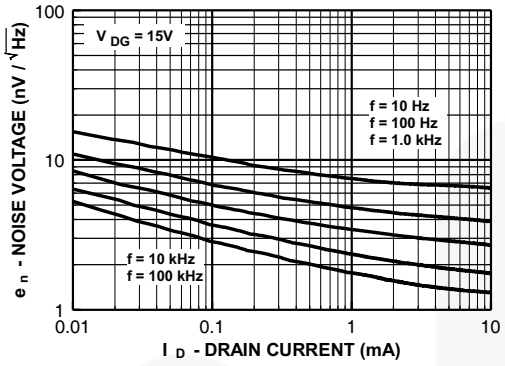



**Figure 15. Noise Voltage vs. Current**

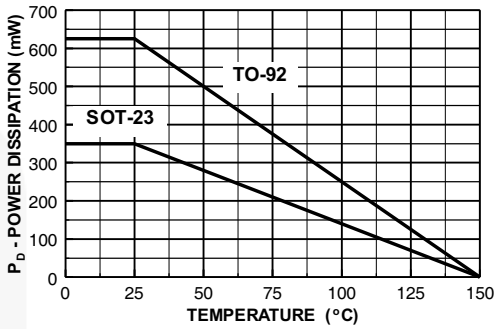



**Figure 16. Power Dissipation vs. Ambient Temperature**

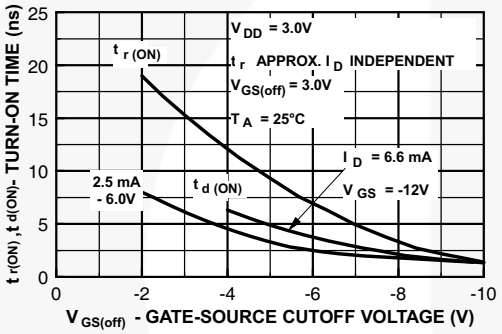



**Figure 17. Switching Turn-On Time vs. Gate-Source Voltage**

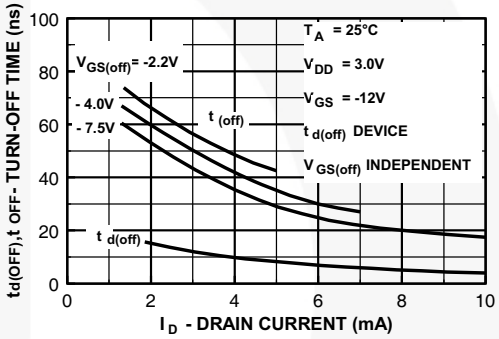
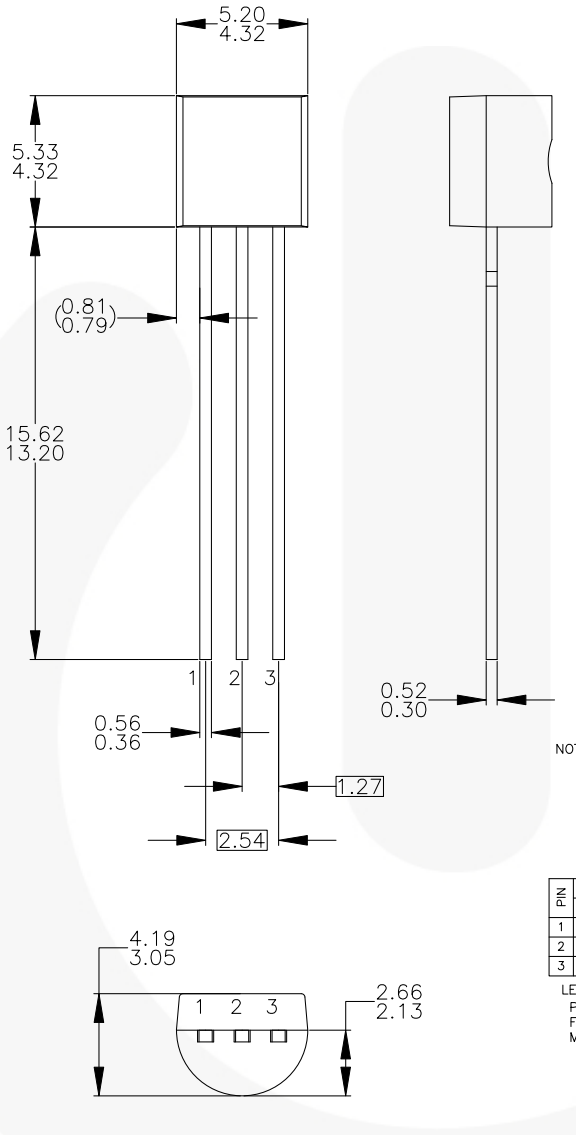



**Figure 18. Switching Turn-Off Time vs. Drain Current**

## Physical Dimensions




NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO−92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M−1994.
D) TO−92 (92,94,96,97,98) PIN CONFIGURATION:

| PIN | 92 | | | 94 | | | 96 | | | 97 | | | 98 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | P | F | M | P | F | M | B | F | M | P | F | M | P | F | M |
| 1 | E | S | S | E | S | S | B | D | G | C | G | D | C | G | D |
| 2 | B | D | G | C | G | D | E | S | S | B | D | G | E | S | S |
| 3 | C | G | D | B | D | G | C | G | D | E | S | S | B | D | G |

LEGEND:
P − BIPOLAR
F − JFET
M − DMOS
E − EMITTER
B − BASE
C − COLLECTOR
D − DRAIN
S − SOURCE
G − GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT−ZA03DREV3.

**Figure 19. 3-Lead, TO-92, JEDEC TO-92 Compliant Straight Lead Configuration, Bulk Type**

## Physical Dimensions (Continued)

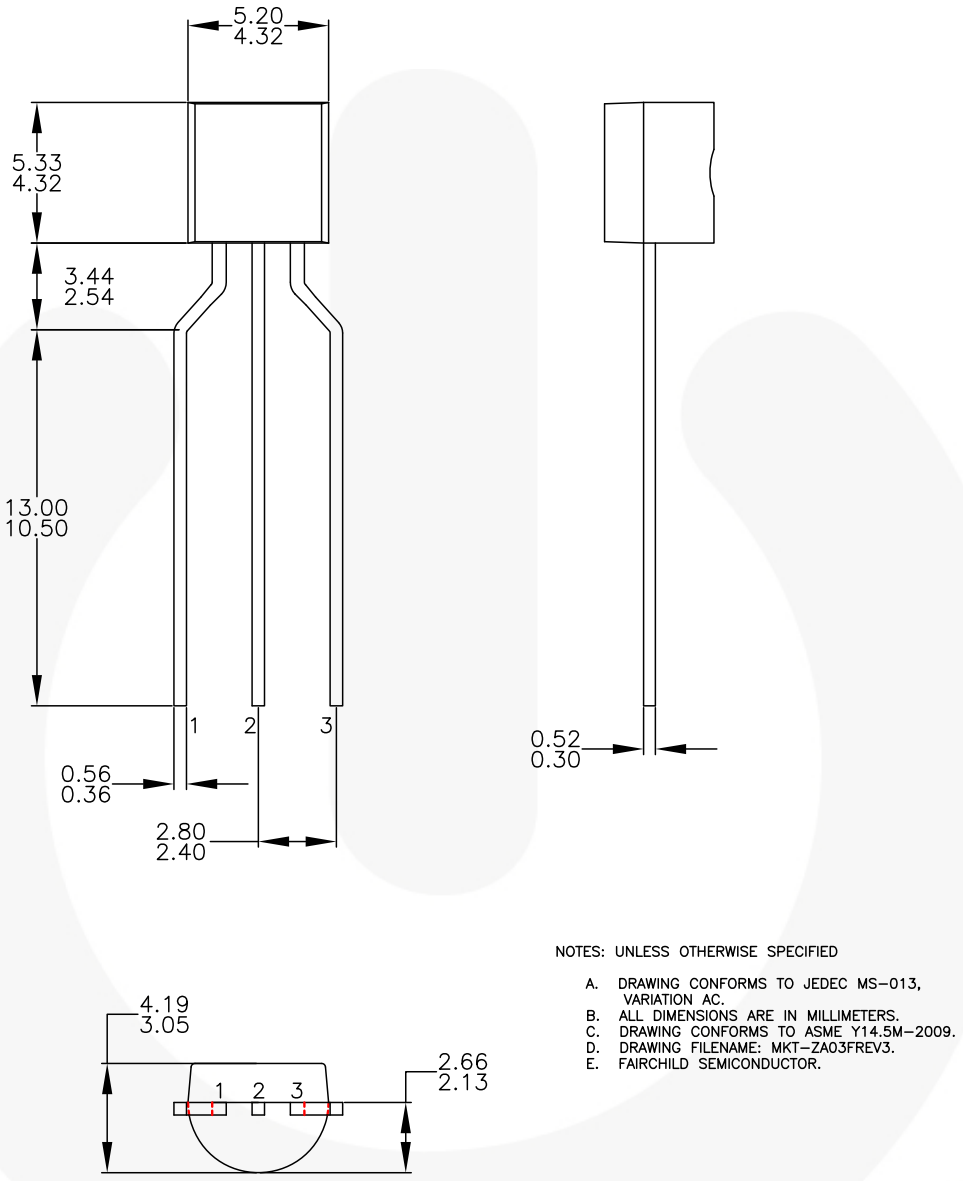



**Figure 20. 3-Lead, TO-92, Molded, 0.2 In Line Spacing Lead Form, Ammo, Tape and Reel Type**

## Physical Dimensions (Continued)

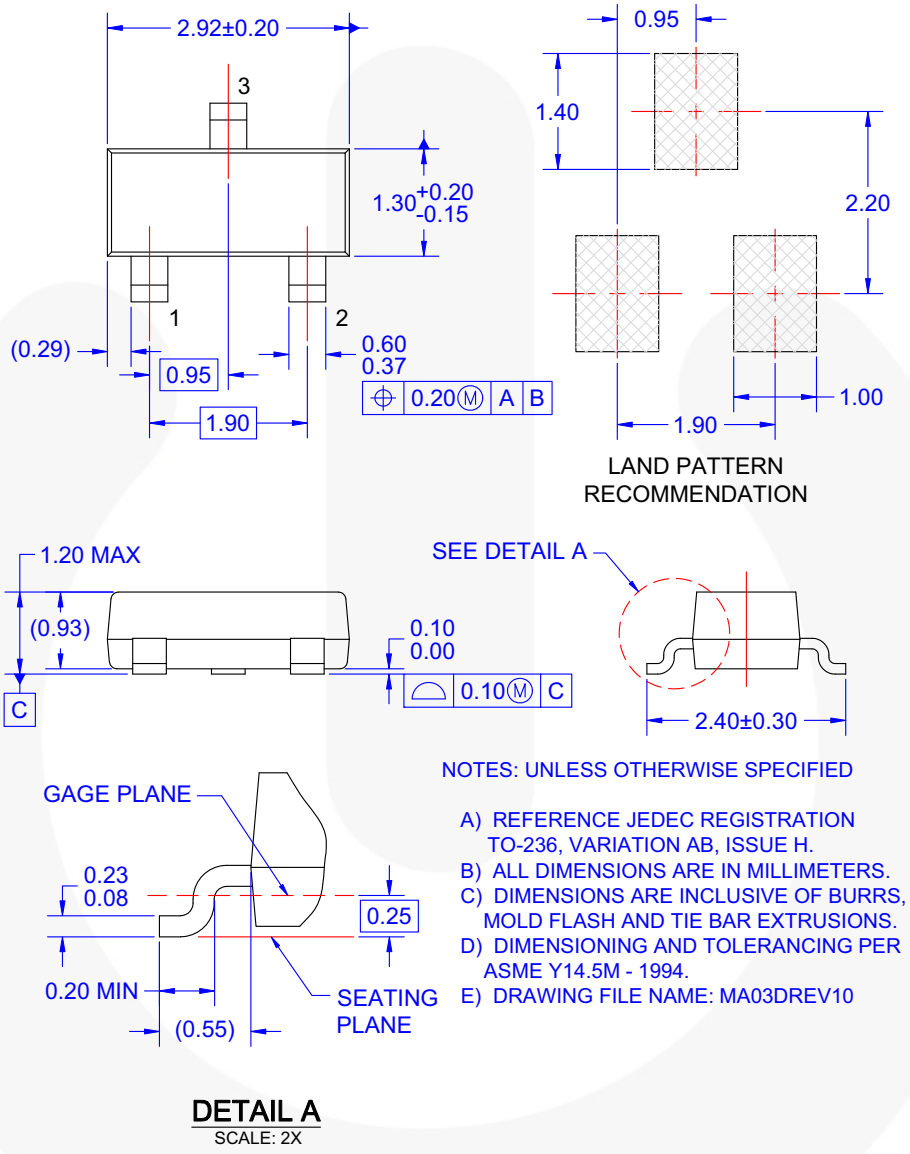



**Figure 21. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE**

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Rev. I73

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