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November 2013

### FDB12N50F

# N-Channel UniFET<sup>TM</sup> FRFET<sup>®</sup> MOSFET 500 V, 11.5 A, 700 m $\Omega$

#### **Features**

- $R_{DS(on)}$  = 590 m $\Omega$  (Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 6 A
- Low Gate Charge (Typ. 21 nC)
- Low C<sub>rss</sub> (Typ. 11 pF)
- · 100% Avalanche Tested
- · Improve dv/dt Capability
- · RoHS Compliant

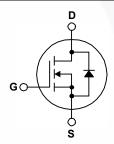
### **Applications**

- · Lighting
- · Uninterruptible Power Supply
- · AC-DC Power Supply

### Description

UniFET<sup>TM</sup> MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its t<sub>rr</sub> is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





### MOSFET Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol		Parameter		FDB12N50FTM_WS	Unit	
V <sub>DSS</sub>	Drain to Source Voltage			500	V	
V <sub>GSS</sub>	Gate to Source Voltage			±30	V	
	Drain Current	- Continuous (T <sub>C</sub> = 25°C)		11.5	^	
ID	Diamounent	- Continuous (T <sub>C</sub> = 100°C)		6.9	A	
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	46	Α	
E <sub>AS</sub>	Single Pulsed Avalanche	Energy	(Note 2)	456	mJ	
I <sub>AR</sub>	Avalanche Current		(Note 1)	11.5	Α	
E <sub>AR</sub>	Repetitive Avalanche Ene	ergy	(Note 1)	16.5	mJ	
dv/dt	Peak Diode Recovery dv/	dt	(Note 3)	20	V/ns	
n	Dawer Dissipation	(T <sub>C</sub> = 25°C)		165	W	
$P_{D}$	Power Dissipation	- Derate above 25°C		1.33	W/°C	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Te	emperature Range		-55 to +150	οС	
T <sub>L</sub>	Maximum Lead Temperat 1/8" from Case for 5 Seco	ure for Soldering Purpose, ands		300	°C	

#### **Thermal Characteristics**

Symbol	Parameter	FQB12N50FTM_WS	Unit
$R_{ heta JC}$	Thermal Resistance, Junction to Case, Max	0.75	
В	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (1 in <sup>2</sup> pad of 2 oz copper), Max.	40	

### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB12N50F	FDB12N50FTM_WS	D2-PAK	330mm	24mm	800 units

### **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu A, V_{GS} = 0V, T_J = 25^{\circ}C$	500	-	-	V
ΔBV <sub>DSS</sub> / ΔΤ <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	-	0.5	-	V/°C
1	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500V, V <sub>GS</sub> = 0V	-	-	10	^
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 400V, T_{C} = 125^{\circ}C$	-	-	100	μΑ
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 30V, V_{DS} = 0V$	-	-	±100	nA

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10V, I_D = 6A$	1	0.59	0.7	Ω
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 40V$ , $I_D = 6A$	-	12	-	S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 05V V 0V	$V_{DS} = 25V, V_{GS} = 0V$		1050	1395	pF
Coss	Output Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V f = 1MHz			135	180	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 = 1101112	-	-\	11	17	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V			- \	21	30	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	$V_{DS} = 400V, I_{D} = 11.5A$	-	- \	6	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	V <sub>GS</sub> = 10V	Note 4)	-	9	-	nC

#### **Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time		-	21	50	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 250V, I_{D} = 11.5A$	-	45	100	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$R_G = 25\Omega$	-	50	110	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	-	35	80	ns

#### **Drain-Source Diode Characteristics**

Is	Maximum Continuous Drain to Source Dioc	Maximum Continuous Drain to Source Diode Forward Current		-	11.5	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	46	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 11.5A	-	-	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 11.5A	-	134	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	-	0.37	-	μС

- **Notes:**1. Repetitive Rating: Pulse width limited by maximum junction temperature
- 2. L = 6.9mH, I $_{AS}$  = 11.5A, V $_{DD}$  = 50V, R $_{G}$  = 25 $\Omega$ , Starting T $_{J}$  = 25 $^{\circ}$ C
- 3.  $I_{SD} \le$  11.5A, di/dt  $\le$  200A/ $\mu$ s,  $V_{DD} \le$  BV $_{DSS}$ , Starting T $_J$  = 25°C
- 4. Essentially Independent of Operating Temperature Typical Characteristics

#### **Typical Characteristics**

Figure 1. On-Region Characteristics

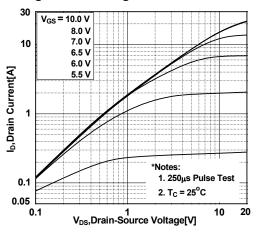


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

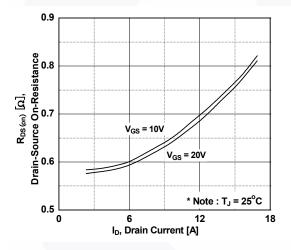
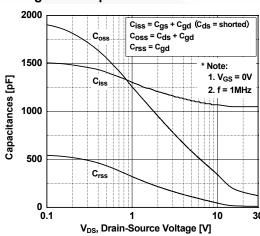


Figure 5. Capacitance Characteristics



**Figure 2. Transfer Characteristics** 

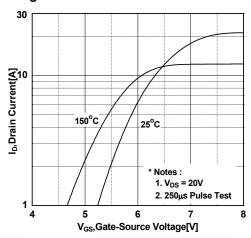


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

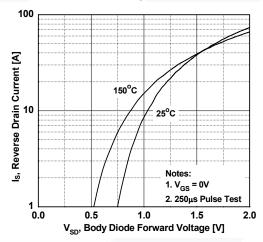
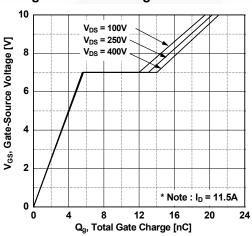


Figure 6. Gate Charge Characteristics



### Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

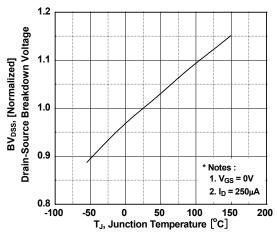


Figure 8. Maximum Safe Operating Area

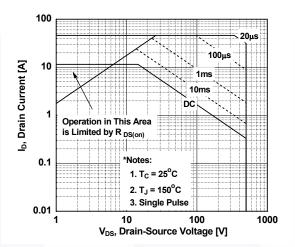


Figure 9. Maximum Drain Current vs. Case Temperature

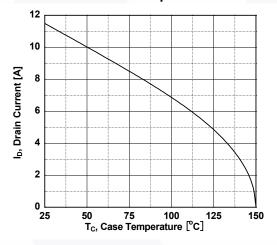


Figure 10. Transient Thermal Response Curve

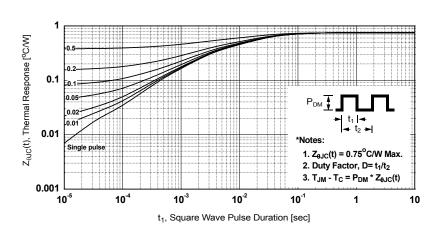


Figure 11. Gate Charge Test Circuit & Waveform

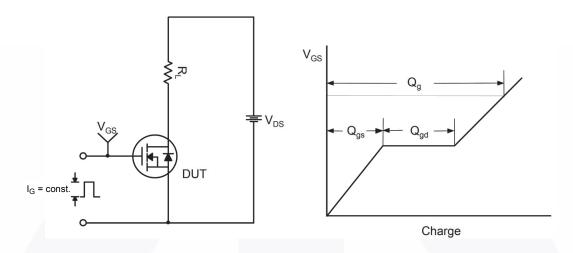


Figure 12. Resistive Switching Test Circuit & Waveforms

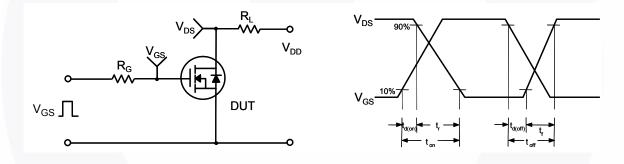
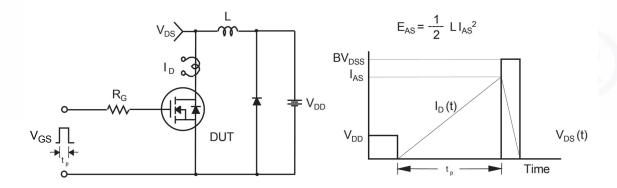


Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms



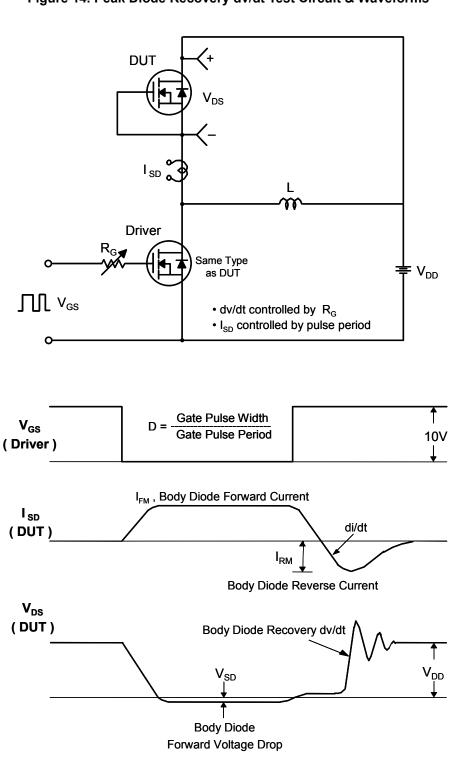


Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms

#### **Mechanical Dimensions**

# TO-263 2L (D<sup>2</sup>PAK)

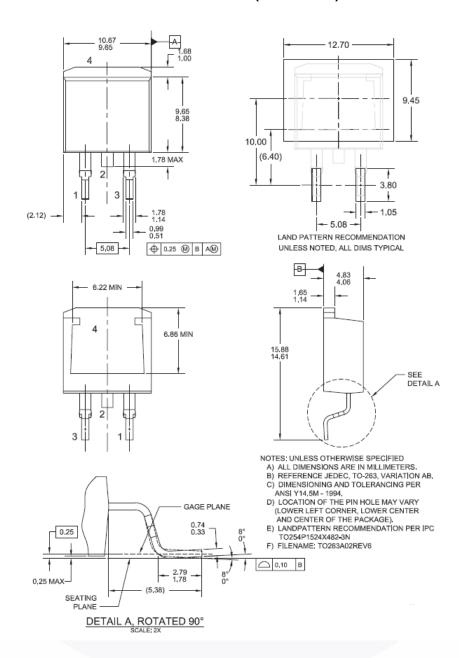


Figure 15. 2LD, TO263, Surface Mount

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Dimension in Millimeters





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