



STB12NM50ND STD12NM50ND, STF12NM50ND

N-channel 500 V, 0.29 Ω , 11 A, FDmesh™ II Power MOSFET
(with fast diode) in D²PAK, DPAK, TO-220FP

Features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)} max	I _D
STB12NM50ND	550 V	0.38 Ω	11 A
STD12NM50ND	550 V	0.38 Ω	11 A
STF12NM50ND	550 V	0.38 Ω	11 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Application

- Switching applications

Description

FDmesh™ technology combines the MDmesh™ features with an intrinsic fast-recovery body diode. The resulting product has reduced on-resistance and fast switching commutations, making it especially suitable for bridge topologies where low t_{rr} is required.

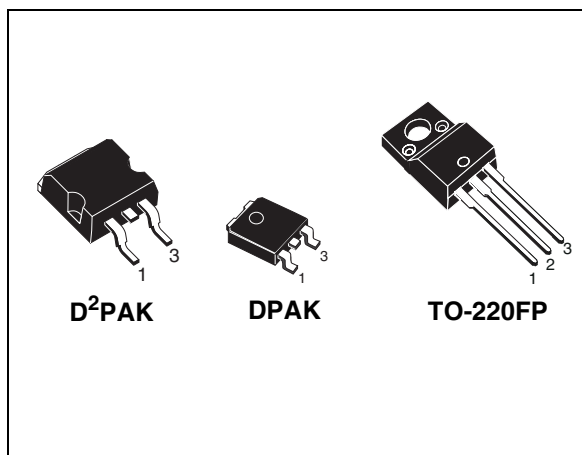
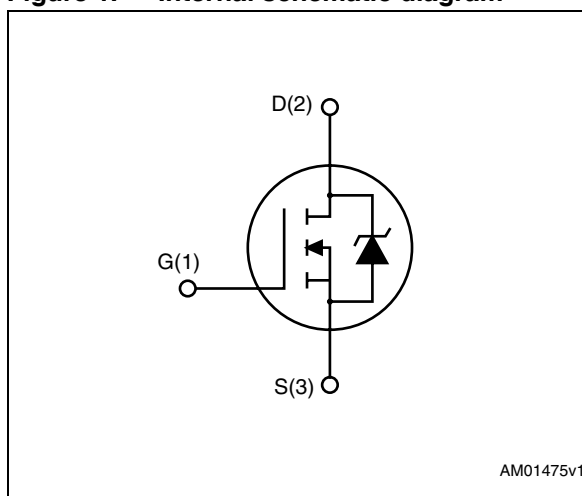


Figure 1. Internal schematic diagram



AM01475v1

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB12NM50ND	12NM50ND	D ² PAK	Tape and reel
STD12NM50ND	12NM50ND	DPAK	Tape and reel
STF12NM50ND	12NM50ND	TO-220FP	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		D ² PAK	DPAK	TO-220FP	
V _{DS}	Drain-source voltage (V _{GS} =0)	500			V
V _{GS}	Gate-source voltage	± 25			V
I _D	Drain current (continuous) at T _C = 25 °C	11		11 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	6.9		6.9 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	44		44 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	100		25	W
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T _C =25 °C)			2500	V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	40			V/ns
T _{stg}	Storage temperature	-55 to 150			°C
T _j	Operating junction temperature	150			°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤ 11 A, di/dt ≤ 600 A/μs, V_{DD} = 80% V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		D ² PAK	DPAK	TO-220FP	
R _{thj-case}	Thermal resistance junction-case max	1.25			°C/W
R _{thj-pcb}	Thermal resistance junction-pcb max	30	50		°C/W
R _{thj-amb}	Thermal resistance junction-amb max	62.5			°C/W
T _l	Maximum lead temperature for soldering purposes	300			°C

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I _{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _j max)	5	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AS} , V _{DD} = 50 V)	350	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	500			V
$dv/dt^{(1)}$	Drain-source voltage slope	$V_{DD} = 400\text{ V}$, $I_D = 11\text{ A}$, $V_{GS} = 10\text{ V}$	44			V/ns
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating}$, @ 125 °C			1 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 5.5\text{ A}$		0.29	0.38	Ω

1. Value measured at turn off under inductive load

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 5.5\text{ A}$	-	8	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	850 48 5	-	pF pF pF
$C_{oss\text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{ to }400\text{ V}$	-	100	-	pF
R_g	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias=0 Test signal level=20 mV open drain	-	4.5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 400\text{ V}$, $I_D = 11\text{ A}$ $V_{GS} = 10\text{ V}$ Figure 19	-	30 6 17	-	nC nC nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$, $I_D = 5.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ <i>Figure 18</i>	-	12	-	ns
t_r	Rise time			15		ns
$t_{d(off)}$	Turn-off delay time			40		ns
t_f	Fall time			17		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$ <i>Figure 20</i>	-	122		ns
Q_{rr}	Reverse recovery charge			650		nC
I_{RRM}	Reverse recovery current			11		A
t_{rr}	Reverse recovery time	$V_{DD} = 100\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $I_{SD} = 11\text{ A}$ $T_j = 150\text{ }^\circ\text{C}$, <i>Figure 20</i>	-	160		ns
Q_{rr}	Reverse recovery charge			940		nC
I_{RRM}	Reverse recovery current			12		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

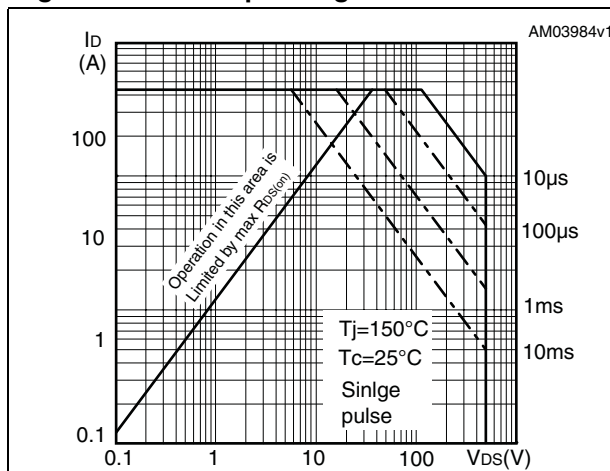
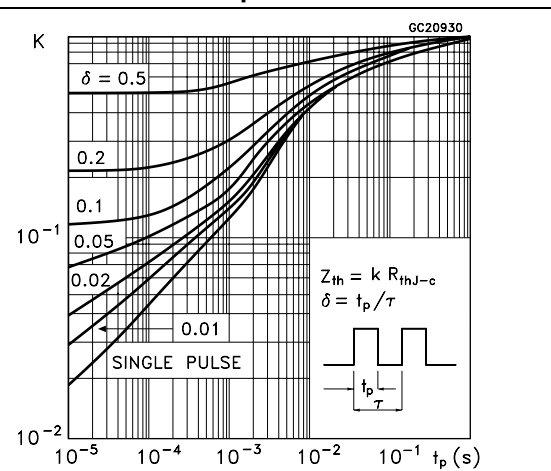
Figure 2. Safe operating area for D²PAKFigure 3. Thermal impedance for D²PAK

Figure 4. Safe operating area for TO-220FP

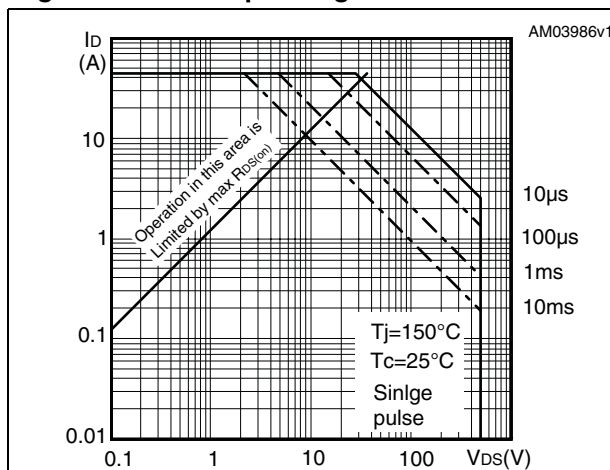


Figure 5. Thermal impedance for TO-220FP

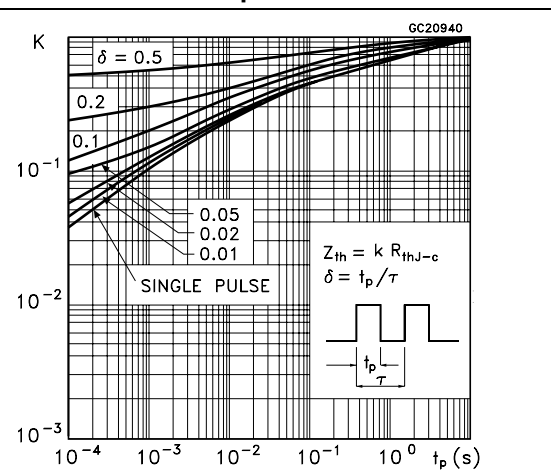


Figure 6. Safe operating area for DPAK

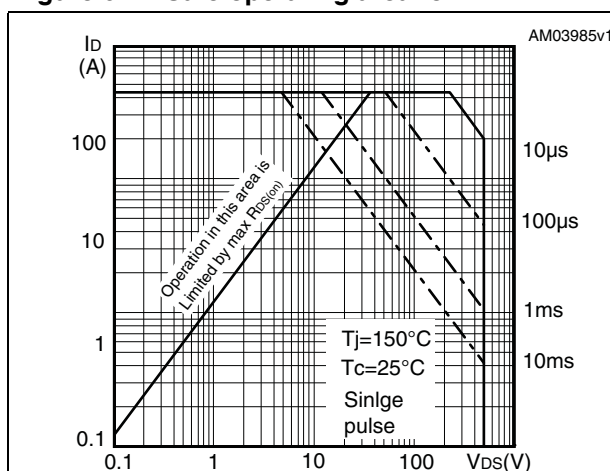


Figure 7. Thermal impedance for DPAK

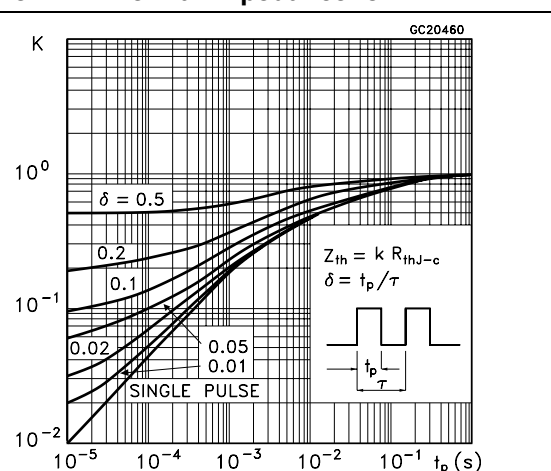


Figure 8. Output characteristics

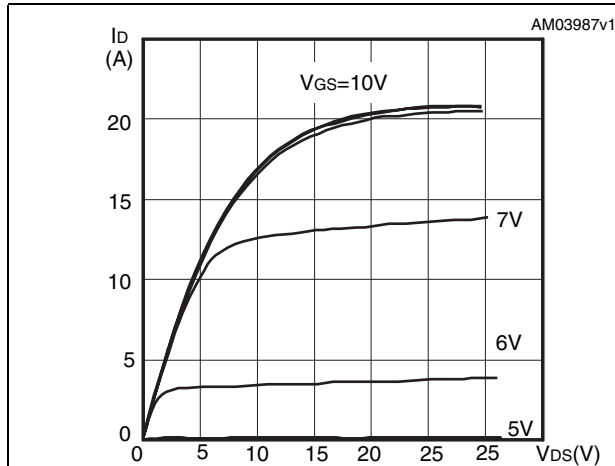


Figure 9. Transfer characteristics

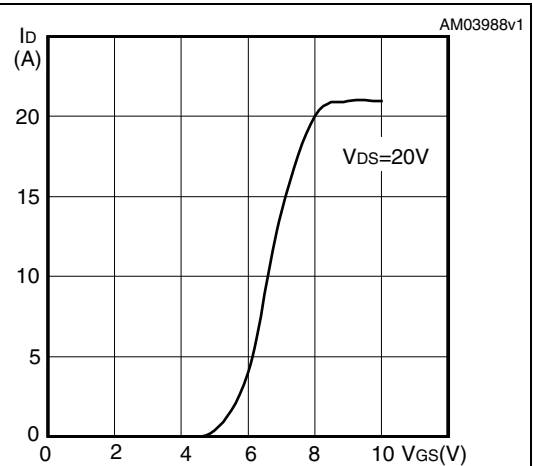


Figure 10. Transconductance

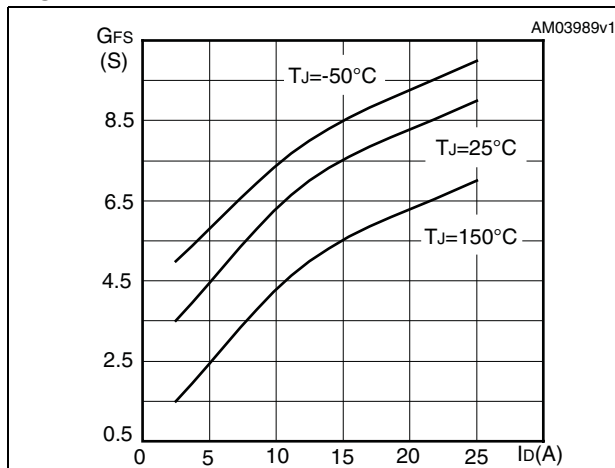


Figure 11. Static drain-source on resistance

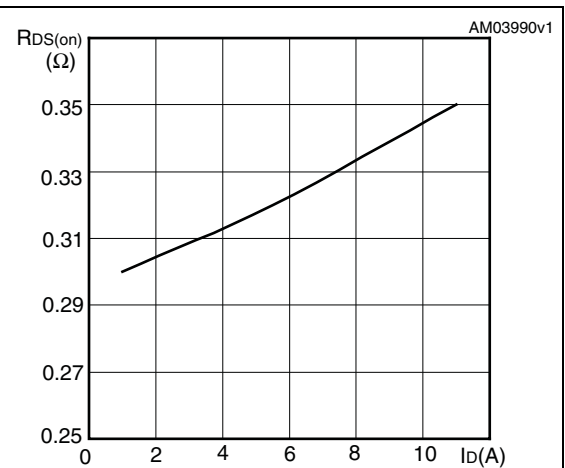


Figure 12. Gate charge vs gate-source voltage

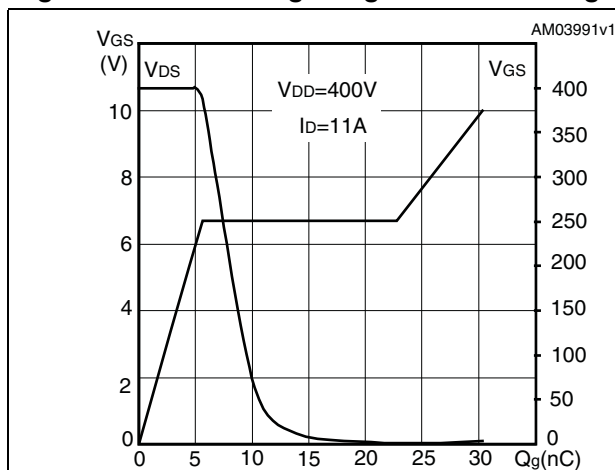


Figure 13. Capacitance variations

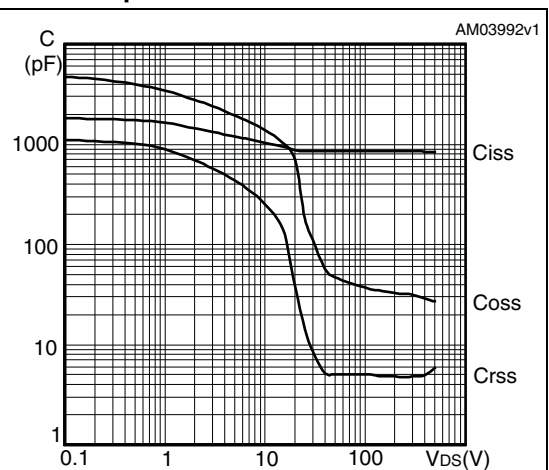


Figure 14. Normalized gate threshold voltage vs temperature

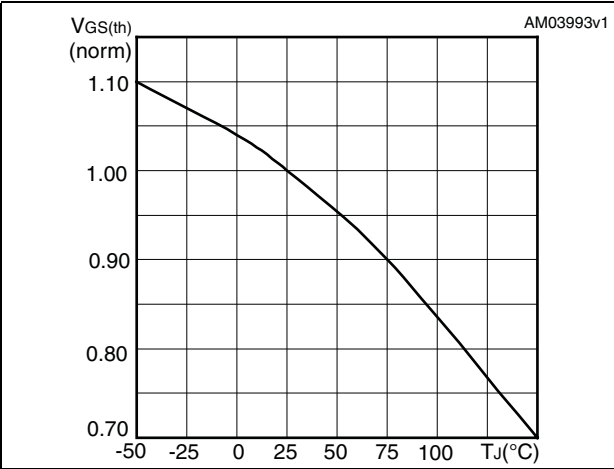


Figure 15. Normalized on resistance vs temperature

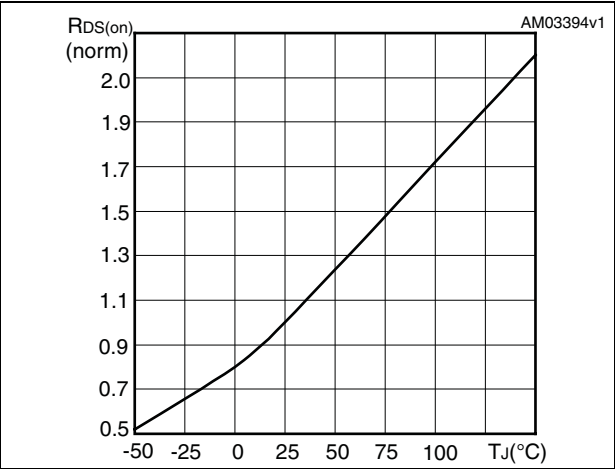


Figure 16. Source-drain diode forward characteristics

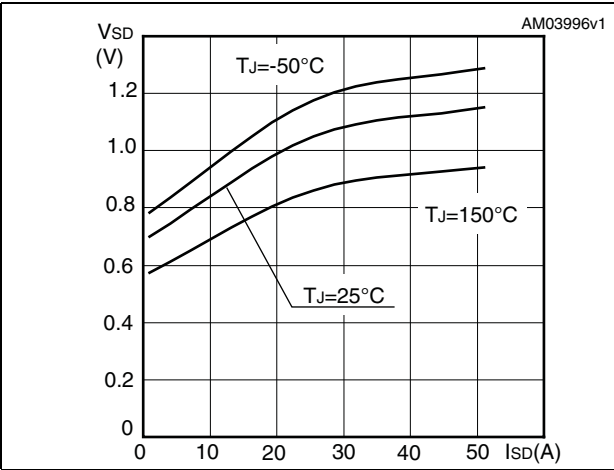
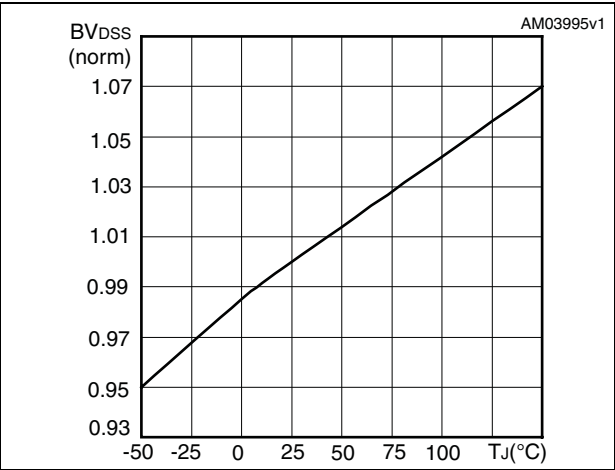


Figure 17. Normalized B_{VDSS} vs temperature



3 Test circuits

Figure 18. Switching times test circuit for resistive load

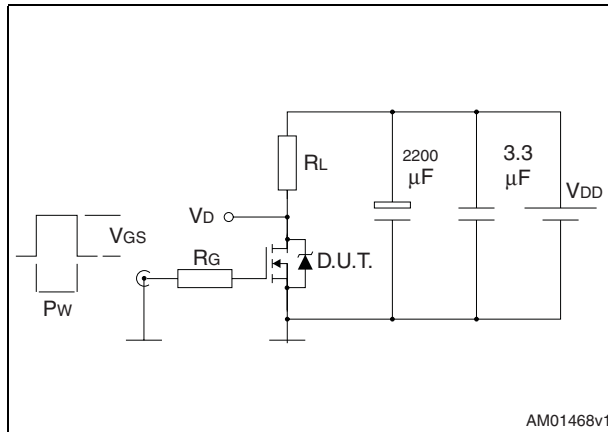


Figure 19. Gate charge test circuit

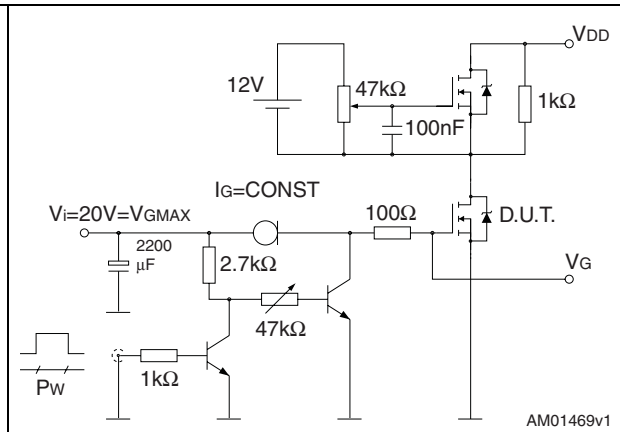


Figure 20. Test circuit for inductive load switching and diode recovery times

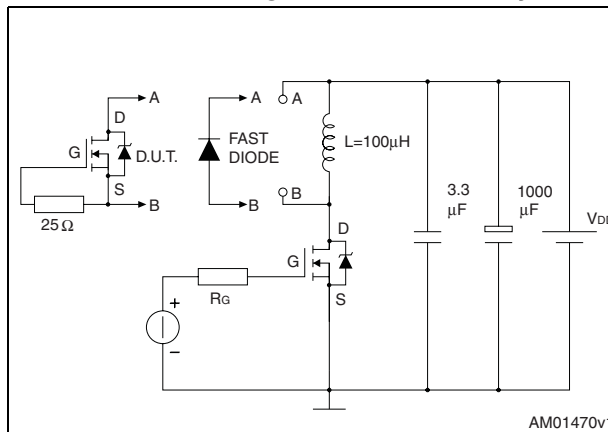


Figure 21. Unclamped inductive load test circuit

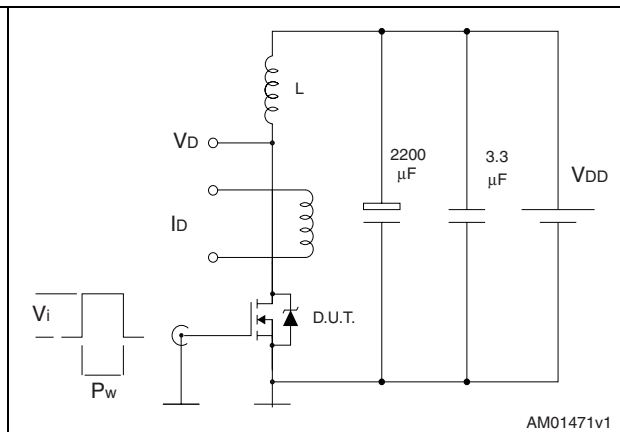


Figure 22. Unclamped inductive waveform

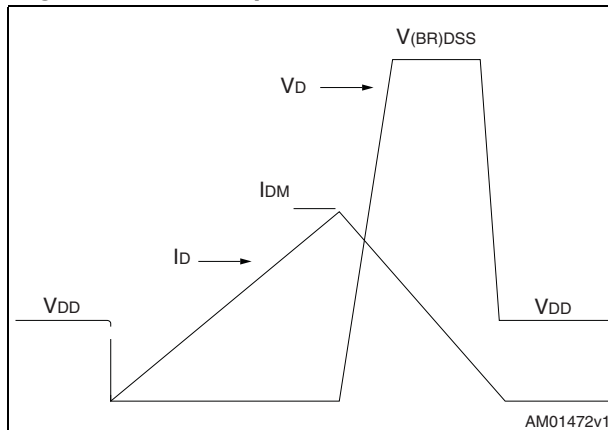
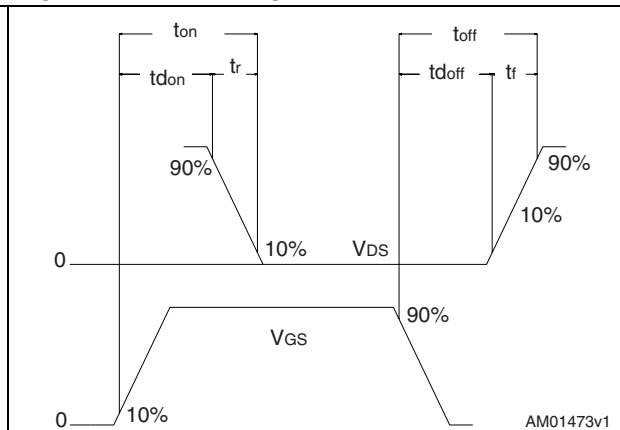


Figure 23. Switching time waveform

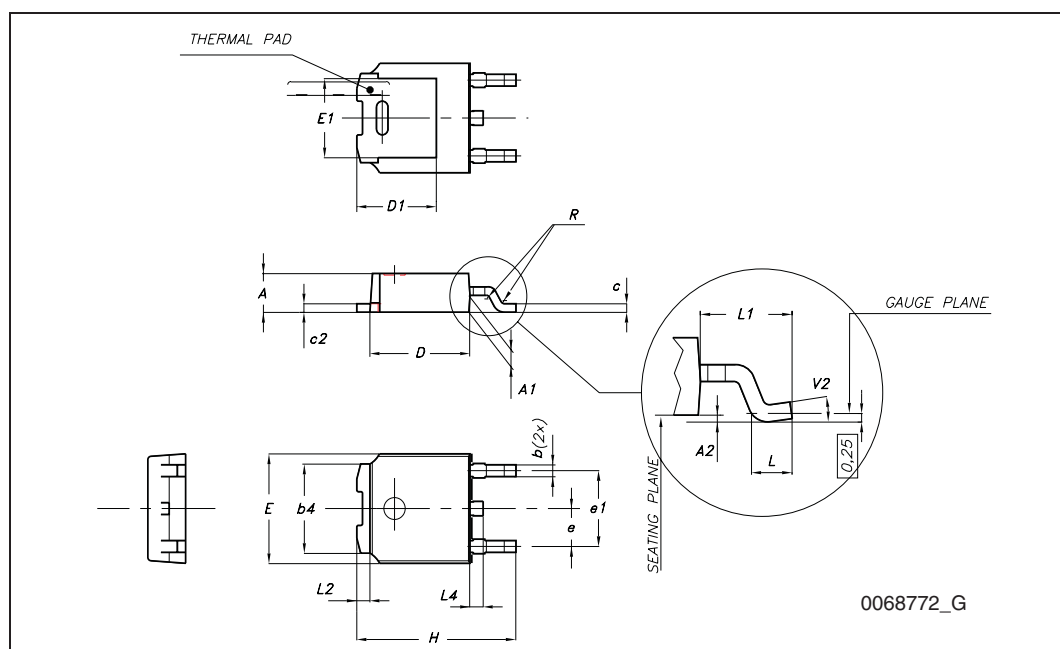


4 Package mechanical data

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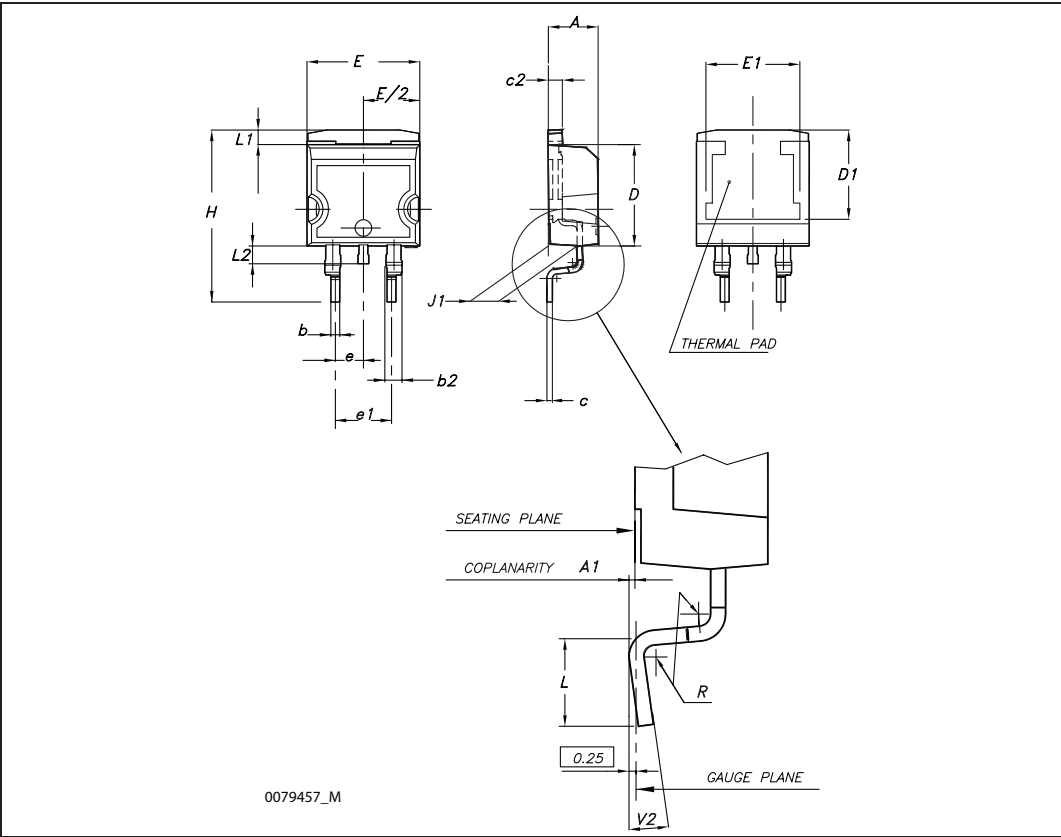
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°



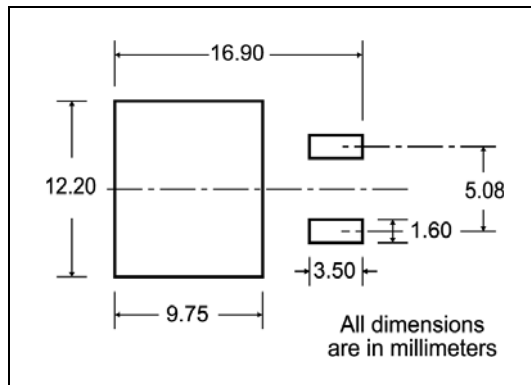
D²PAK (TO-263) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	0.03		0.23	0.001		0.009
b	0.70		0.93	0.027		0.037
b2	1.14		1.70	0.045		0.067
c	0.45		0.60	0.017		0.024
c2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1	7.50			0.295		
E	10		10.40	0.394		0.409
E1	8.50			0.334		
e		2.54			0.1	
e1	4.88		5.28	0.192		0.208
H	15		15.85	0.590		0.624
J1	2.49		2.69	0.099		0.106
L	2.29		2.79	0.090		0.110
L1	1.27		1.40	0.05		0.055
L2	1.30		1.75	0.051		0.069
R		0.4			0.016	
V2	0°		8°	0°		8°

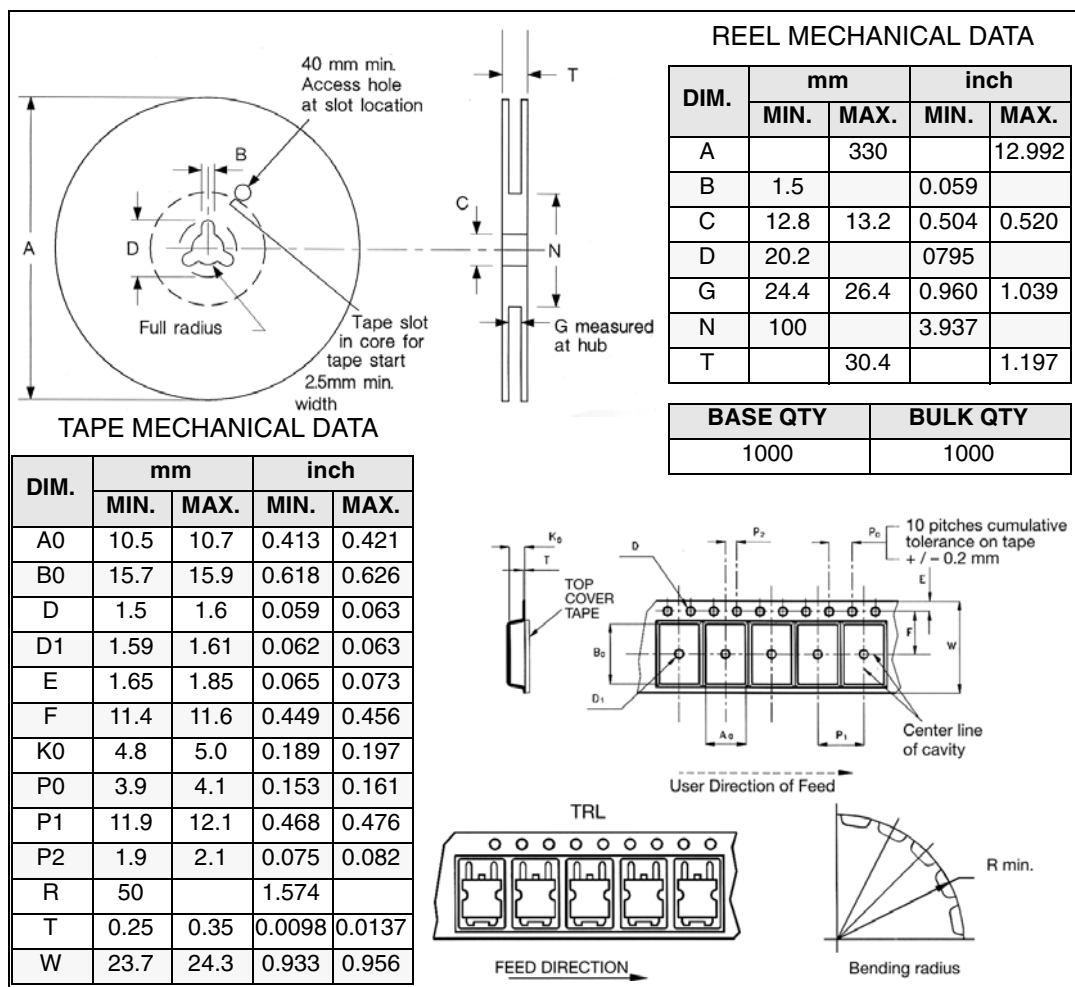


5 Packaging mechanical data

D²PAK FOOTPRINT

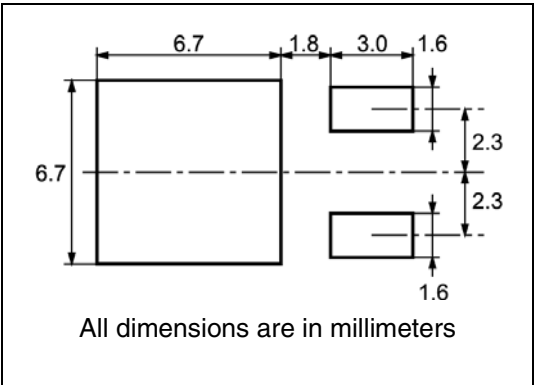


TAPE AND REEL SHIPMENT

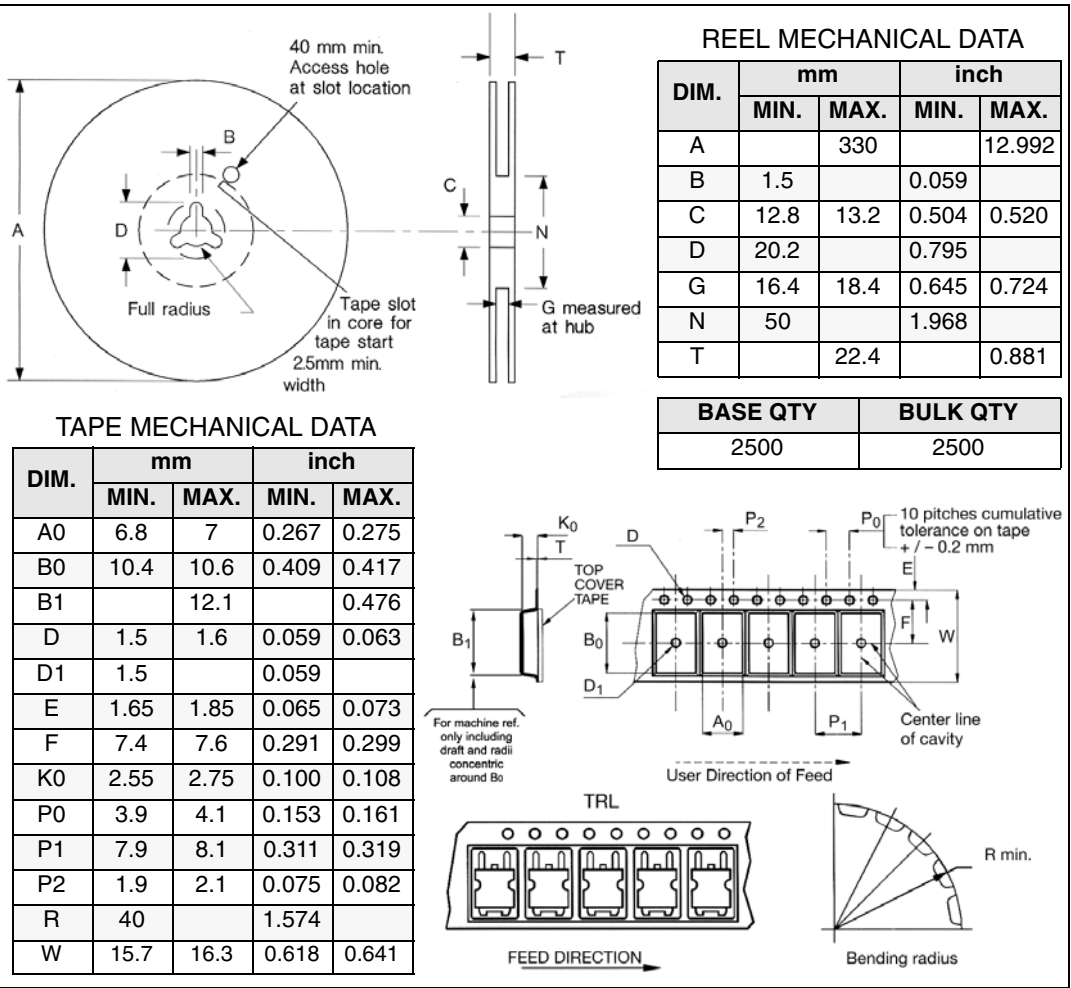


* on sales type

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
23-Sep-2008	1	First release
10-Jun-2009	2	Added new package, mechanical data: TO-220FP

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