INTEGRATED CIRCUITS



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74HC/HCT7030

FEATURES

- Synchronous or asynchronous operation
- 3-state outputs
- · Master-reset input to clear control functions
- 33 MHz (typ.) shift-in, shift-out rates with or without flags
- Very low power consumption
- Cascadable to 25 MHz (typ.)
- Readily expandable in word and bit dimensions
- Pinning arranged for easy board layout: input pins directly opposite output pins
- Output capability: standard
- I_{CC} category: LSI

GENERAL DESCRIPTION

The 74HC/HCT7030 are high-speed Si-gate CMOS devices specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7030 is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 9 bits. A 33 MHz data-rate makes it ideal for high-speed applications. Even at high frequencies, the I_{CC} dynamic is very low ($f_{max} = 18$ MHz; $V_{CC} = 5$ V produces a dynamic I_{CC} of 80 mA). If the device is not continuously operating at f_{max} , then I_{CC} will decrease proportionally.

With separate controls for shift-in (SI) and shift-out (SO), reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a master-reset input ($\overline{\text{MR}}$) and an output enable input ($\overline{\text{OE}}$). Flags for data-in-ready (DIR) and data-out-ready (DOR) indicate the status of the device.

Devices can be interconnected easily to expand word and bit dimensions. All output pins are directly opposite the corresponding input pins thus simplifying board layout in expanded applications.

INPUTS AND OUTPUTS

Data inputs (D₀ to D₈)

As there is no weighting of the inputs, any input can be assigned as the MSB. The size of the FIFO memory can be reduced from the 9 × 64 configuration, i.e. 8 × 64, 7 × 64, down to 1 × 64, by tying unused data input pins to V_{CC} or GND.

Data outputs (Q₀ to Q₈)

As there is no weighting of the outputs, any output can be assigned as the MSB. The size of the FIFO memory can be reduced from the 9×64 configuration as described for data inputs. In a reduced format, the unused data output pins must be left open circuit.

Master-reset (MR)

When $\overline{\text{MR}}$ is LOW, the control functions within the FIFO are cleared, and data content is declared invalid. The data-in-ready (DIR) flag is set HIGH and the data-out-ready (DOR) flag is set LOW. The output stage remains in the state of the last word that was shifted out, or in the random state existing at power-up.

Status flag outputs (DIR, DOR)

Indication of the status of the FIFO is given by two status flags, data-in-ready (DIR) and data-out-ready (DOR):

- DIR = HIGH indicates the input stage is empty and ready to accept valid data
- DIR = LOW indicates that the FIFO is full or that a previous shift-in operation is not complete (busy)
- $\label{eq:DOR} \begin{array}{ll} \mbox{=} & HIGH \mbox{ assures valid data is present at the} \\ & \mbox{ outputs } Q_0 \mbox{ to } Q_8 \mbox{ (does not indicate that new} \\ & \mbox{ data is awaiting transfer into the output stage)} \end{array}$
- DOR = LOW indicates the output stage is busy or there is no valid data

Shift-in control (SI)

Data is loaded into the input stage on a LOW-to-HIGH transition of SI. A HIGH-to-LOW transition triggers an automatic data transfer process (ripple through). If SI is held HIGH during reset, data will be loaded at the rising edge of the $\overline{\text{MR}}$ signal.

Shift-out control (SO)

A LOW-to-HIGH transition of \overline{SO} causes the DOR flags to go LOW. A HIGH-to-LOW transition of \overline{SO} causes upstream data to move into the output stage, and empty locations to move towards the input stage (bubble-up).

Output enable (OE)

The outputs Q_0 to Q_8 are enabled when \overline{OE} = LOW. When \overline{OE} = HIGH the outputs are in the high impedance OFF-state.

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QUICK REFERENCE DATA

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GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns
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SYMBOL		CONDITIONS	TYP		
STIVIDUL		CONDITIONS	НС	нст	
t _{PHL} / t _{PLH}	propagation delay	$C_{L} = 15 \text{ pF}; V_{CC} = 5 \text{ V}$			
	MR to DIR and DOR		21	26	ns
	SO to Q _n		36	40	ns
f _{max}	maximum clock frequency SI and SO		33	29	MHz
CI	input capacitance		3.5	3.5	pF
CP	power dissipation capacitance per package	notes 1 and 2	660	660	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

 $P_{D} = C_{PD} \times V_{CC}{}^{2} \times f_{i} + \Sigma \; (C_{L} \times V_{CC}{}^{2} \times f_{o})$ where:

- f_i = input frequency in MHz
- $f_o = output frequency in MHz$

 $\Sigma (C_L \times V_{CC}^2 \times f_0)$ = sum of outputs

- C_L = output load capacitance in pF
- V_{CC} = supply voltage in V
- 2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} 1.5 V

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 14	GND	ground (0 V)
3	DIR	data-in-ready output
4	SI	shift-in input (LOW-to-HIGH, edge-triggered)
5, 6, 7, 8, 9, 10, 11, 12, 13	D ₀ to D ₈	parallel data inputs
15	ŌĒ	output enable input (active LOW)
24, 23, 22, 21, 20, 19, 18, 17, 16	Q ₀ to Q ₈	3-state parallel data outputs
25	DOR	data-out-ready output
26	SO	shift-out input (HIGH-to-LOW, edge-triggered)
27	MR	asynchronous master-reset input (active LOW)
28	Vcc	positive supply voltage

Note

1. Pin 14 must be connected to GND. Pins 1 and 2 can be left floating or connected to GND, however it is not allowed to let current flow in either direction between pins 1, 2 and 14.



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APPLICATIONS

- High-speed disc or tape controller
- Video timebase correction
- A/D output buffers
- Voice synthesis
- Input/output formatter for digital filters and FFTs
- Bit-rate smoothing

there is valid data at the output (Q_0 to Q_8). The initial master-reset at power-on (MR = LOW) sets DOR to LOW (see Fig.8). After \overline{MR} = HIGH, data shifted into the FIFO moves through to the output stage causing DOR to go HIGH. As the DOR flag goes HIGH, data can be shifted-out using the \overline{SO} control input. With \overline{SO} = HIGH, data in the output stage is shifted out and a busy indication is given by DOR going LOW. When \overline{SO} is made LOW, data moves through the FIFO to fill the output stage and an empty location appears at the input stage. When the output stage is filled DOR goes HIGH, but if the last of the valid data has been shifted out leaving the FIFO empty the DOR flag remains LOW (see Fig.9). With the FIFO empty, the last word that was shifted-out is latched at the output

FIFO as data moves through the device.

Data output

After data has been transferred from the input stage of the FIFO following SI = LOW, data moves through the FIFO asynchronously and is stacked at the output end of the register. Empty locations appear at the input end of the

The data-out-ready flag (DOR = HIGH) indicates that

(SO) pulse occurs. Then, following a shift-out of data, an empty location appears at the FIFO input and DIR goes HIGH to allow the next data to be shifted-in. This remains at the first FIFO location until SI again goes LOW (see Fig.7).

Data transfer

DIR flag remains LOW if the FIFO is full (see Fig.6). The SI pulse must be made LOW in order to complete the

shift-in process. With the FIFO full, SI can be held HIGH until a shift-out

LOW to clear the FIFO memory (see Fig.8). The

9-bit x 64-word FIFO register; 3-state

Following power-up, the master-reset (MR) input is pulsed

data-in-ready flag (DIR = HIGH) indicates that the FIFO input stage is empty and ready to receive data. When DIR

is valid (HIGH), data present at D₀ to D₈ can be shifted-in using the SI control input. With SI = HIGH, data is shifted

into the input stage and a busy indication is given by DIR

The data remains at the first location in the FIFO until SI is

set to LOW. With SI = LOW data moves through the FIFO

(HIGH) to indicate that space is available in the FIFO. The

to the output stage, or to the last empty location. If the FIFO is not full after the SI pulse, DIR again becomes valid

With the FIFO empty, the \overline{SO} input can be held HIGH until the SI control input is used. Following an SI pulse, data moves through the FIFO to the output stage, resulting in the DOR flag pulsing HIGH and a shift-out of data occurring. The SO control must be made LOW before additional data can be shifted out (see Fig.10).

High-speed burst mode

If it is assumed that the shift-in/shift-out pulses are not applied until the respective status flags are valid, it follows that the shift-in/shift-out rates are determined by the status flags. However, without the status flags a high-speed burst mode can be implemented. In this mode, the burst-in/burst-out rates are determined by the pulse widths of the shift-in/shift-out inputs and burst rates of 35 MHz can be obtained. Shift pulses can be applied without regard to the status flags but shift-in pulses that would overflow the storage capacity of the FIFO are not allowed (see Figs 11 and 12).

Expanded format

With the addition of a logic gate, the FIFO is easily expanded to increase word length (see Fig.17). The basic operation and timing are identical to a single FIFO, with the exception of an additional gate delay on the flag outputs. If during application, the following occurs:

- · SI is held HIGH when the FIFO is empty, some additional logic is required to produce a composite DIR pulse (see Figs 7 and 18).
- SO is held HIGH when the FIFO is full, some additional logic is required to produce a composite DOR pulse (see Figs 10 and 18).

Due to the part-to-part spread of the ripple through time, the flag signals of FIFO_A and FIFO_B will not always coincide and the AND-gate will not produce a composite flag signal. The solution is given in Fig.18.

The "7030" is easily cascaded to increase the word capacity and no external components are needed. In the cascaded configuration, all necessary communications and timing are performed by the FIFOs. The intercommunication speed is determined by the minimum flag pulse widths and the flag delays. The data rate of cascaded devices is typically 25 MHz. Word-capacity can be expanded to and beyond 128-words \times 9-bits (see Fig.19).

FUNCTIONAL DESCRIPTION

Data input

going LOW.

Product specification



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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard I_{CC} category: LSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

		T _{amb} (°C)								TEST CONDITIONS		
SYMBOL					74HC							
STWBUL	PARAMETER		+25		_40 t	:o +85	-40 t	o +125		V _{CC}	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		(•)		
t _{PHL} / t _{PLH}	propagation delay MR to DIR, DOR		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.8	
t _{PHL} / t _{PLH}	propagation delay SI to DIR		77 28 22	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	Fig.6	
t _{PHL} / t _{PLH}	propagation delay SO to DOR		102 37 30	315 63 54		395 79 67		475 95 81	ns	2.0 4.5 6.0	Fig.9	
t _{PHL} / t _{PLH}	propagation delay DOR to Q _n		11 4 3	35 7 6		45 9 8		55 11 9	ns	2.0 4.5 6.0	Fig.10	
t _{PHL} / t _{PLH}	propagation delay SO to Q _n		113 41 33	345 69 59		430 86 73		520 104 88	ns	2.0 4.5 6.0	Fig.14	
t _{PLH}	propagation delay/ ripple_through delay SI to DOR		2.5 0.9 0.7	8.0 1.6 1.3		10 2.0 1.6		12 2.4 1.9	μs	2.0 4.5 6.0	Fig.10	
t _{PLH}	propagation delay/ bubble-up delay SO to DIR		3.3 1.2 1.0	10.0 2.0 1.6		12 2.5 2.0		15 3.0 2.4	μs	2.0 4.5 6.0	Fig.7	
t _{PZH} / t _{PZL}	3-state output enable OE to Q _n		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.16	
t _{PHZ} / t _{PLZ}	3-state output disable OE to Q _n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.16	
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.14	
t _W	SI pulse width HIGH or LOW	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.6	

				1	ר _{amb} (°		TEST CONDITIONS				
					74HC						
STIVIBUL	PARAMETER		+25		_40 t	o +85	-40 to	o +125	UNIT	V _{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t _W	SO pulse width HIGH or LOW	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.9
t _W	DIR pulse width HIGH	10 5 4	47 17 14	145 29 25	8 4 3	180 36 31	8 4 3	220 44 38	ns	2.0 4.5 6.0	Fig.7
t _W	DOR pulse width HIGH	10 5 4	47 17 14	145 29 25	8 4 3	180 36 31	8 4 3	220 44 38	ns	2.0 4.5 6.0	Fig.10
t _W	MR pulse width LOW	70 14 12	22 8 6		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig.8
t _{rem}	removal time MR to SI	80 16 14	24 8 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.15
t _{su}	set-up time D _n to SI	-35 -7 -6	-36 -13 -10		-45 -9 -8		-55 -11 -9		ns	2.0 4.5 6.0	Fig.13
t _h	hold time D _n to SI	135 27 23	44 16 13		170 34 29		205 41 35		ns	2.0 4.5 6.0	Fig.13
f _{max}	maximum clock pulse frequency SI, SO burst mode		9.9 30 36		2.8 14 16		2.4 12 14		MHz	2.0 4.5 6.0	Figs 11 and 12
f _{max}	maximum clock pulse frequency SI, SO using flags		9.9 30 36		2.8 14 16		2.4 12 14		MHz	2.0 4.5 6.0	Figs 6 and 9
f _{max}	maximum clock pulse frequency SI, SO cascaded		7.6 23 27		2.2 11 13		1.8 9.2 11		MHz	2.0 4.5 6.0	Figs 6 and 9

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard I_{CC} category: LSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
ŌE	1.00
SI	1.50
D _n	0.75
MR	1.50
SO	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6 ns$; $C_L = 50 pF$

			T _{amb} (°	°C)				TEST CONDITIONS			
SYMBOL					74HC	т					
STMBOL	PARAMETER		+25		-40 t	o +85	-40 to	o +125		V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay MR to DIR, DOR		30	51		53		63	ns	4.5	Fig.8
t _{PHL} / t _{PLH}	propagation delay SI to DIR		29	49		61		74	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay SO to DOR		39	67		84		101	ns	4.5	Fig.9
t _{PHL} / t _{PLH}	propagation delay SO to Q _n		46	78		98		117	ns	4.5	Fig.14
t _{PHL} / t _{PLH}	propagation delay DOR to Q _n		7	12		15		18	ns	4.5	Fig.10
t _{PLH}	propagation delay/ripple through delay SI to DOR		0.9	1.6		2.0		2.4	μs	4.5	Fig.10
t _{PLH}	propagation delay/ bubble-up delay SO to DIR		1.2	2.0		2.5		3.0	μs	4.5	Fig.7
t _{PZH} / t _{PZL}	$\begin{array}{c} \text{3-state output enable} \\ \overline{\text{OE}} \text{ to } Q_n \end{array}$		20	35		44		53	ns	4.5	Fig.16
t _{PHZ} / t _{PLZ}	$\frac{3\text{-state output disable}}{\overline{\text{OE}} \text{ to } Q_n}$		19	35		44		53	ns	4.5	Fig.16
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.14

		T _{amb} (°C)							TEST CONDITIONS		
SYMBOL					74HC	т					
STMBOL	PARAMETER		+25		-40 t	o +85	-40 to	o +125		V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t _W	SI pulse width HIGH or LOW	12	6		15		18		ns	4.5	Fig.6
t _W	SO pulse width HIGH or LOW	15	9		19		22		ns	4.5	Fig.9
t _W	DIR pulse width HIGH	7	22	37	6	46	6	56	ns	4.5	Fig.7
t _W	DOR pulse width HIGH	6	20	35	5	44	5	53	ns	4.5	Fig.10
t _W	MR pulse width LOW	18	10		23		27		ns	4.5	Fig.8
t _{rem}	removal time MR to SI	18	10		23		27		ns	4.5	Fig.15
t _{su}	set-up time D _n to SI	-5	-16		-4		-4		ns	4.5	Fig.13
t _h	hold time D _n to SI	30	18		38		45		ns	4.5	Fig.13
f _{max}	maximum clock pulse frequency SI, SO burst mode	15	26		12		10		MHz	4.5	Figs 11 and 12
f _{max}	maximum clock pulse frequency SI, SO using flags	15	26		12		10		MHz	4.5	Figs 6 and 9
f _{max}	maximum clock pulse frequency SI, SO cascaded	13	22		10		8.6		MHz	4.5	Figs 6 and 9

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AC WAVEFORMS

Shifting in sequence FIFO empty to FIFO full



With FIFO full; SI held HIGH in anticipation of empty location



Notes to Fig.6

- 1. DIR initially HIGH; FIFO is prepared for valid data.
- 2. SI set HIGH; data loaded into input stage.
- 3. DIR drops LOW, input stage "busy".
- 4. SI set LOW; data from first location "ripple through".
- 5. DIR goes HIGH, status flag indicates FIFO prepared for additional data.
- 6. Repeat process to load 2nd word through to 64th word into FIFO.
- DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

Notes to Fig.7

- 1. FIFO is initially full, shift-in is held HIGH.
- SO pulse; data in the output stage is unloaded, "bubble-up process of empty locations begins".
- DIR HIGH; when empty location reached input stage, flag indicates FIFO is prepared for data input.
- 4. DIR returns to LOW; FIFO is full again.
- SI brought LOW; necessary to complete shift-in process, DIR remains LOW, because FIFO is full.

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Shifting out sequence; FIFO full to FIFO empty



Notes to Fig.8

- 1. DIR LOW, output ready HIGH; assume FIFO is full.
- 2. MR pulse LOW; clears FIFO.
- 3. DIR goes HIGH; flag indicates input prepared for valid data.
- 4. DOR drops LOW; flag indicates FIFO empty.

Notes to Fig.9

- DOR HIGH; no data transfer in progress, valid data is present at output stage.
- 2. SO set HIGH; results in DOR going LOW.
- 3. DOR drops LOW; output stage "busy".
- SO is set LOW; data in the input stage is unloaded, and new data replaces it as empty location "bubbles-up" to input stage.
- 5. DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay.
- Repeat process to unload the 3rd through to the 64th word from FIFO.
- 7. DOR remains LOW; FIFO is empty.



With FIFO empty; SO is held HIGH in anticipation

Notes to Fig.10

- 1. FIFO is initially empty, \overline{SO} is held HIGH.
- SI pulse; loads data into FIFO and initiates ripple through process.
- 3. DOR flag signals the arrival of valid data at the output stage.
- Output transition; data arrives at output stage after the specified propagation delay between the rising edge of the DOR pulse to the Q_n output.
- 5. DOR goes LOW; FIFO is empty again.
- SO set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty.

Shift-in operation; high-speed burst mode













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APPLICATION INFORMATION





74HC/HCT7030

Product specification

Expanded format

Fig.19 shows two cascaded FIFOs providing a capacity of 128 words \times 9 bits.

Fig.20 shows the signals on the nodes of both FIFOs after the application of a SI pulse, when both FIFOs are initially empty. After a rippled through delay, data arrives at the output of FIFO_A. Due to \overline{SO}_A being HIGH, a DOR pulse is generated. The requirements of SI_B and D_{nB} are satisfied by the DOR_A pulse width and the timing between the rising edge of DOR_A and Q_{nA}. After a second ripple through delay, data arrives at the output of FIFO_B. Fig.21 shows the signals on the nodes of both FIFOs after the application of a \overline{SO}_B pulse, when both FIFOs are initially full. After a bubble-up delay a DIR_B pulse is generated, which acts as a \overline{SO}_A pulse for FIFO_A. One word is transferred

from the output of $FIFO_A$ to the input of $FIFO_B$. The requirements of the $\overline{SO_A}$ pulse for $FIFO_A$ is satisfied by the pulse width of DOR_B . After a second bubble-up delay an empty space arrives at D_{nA} , at which time DIR_A goes HIGH. Fig.22 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.



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9-bit x 64-word FIFO register; 3-state



Notes to Fig.20

- 1. $FIFO_A$ and $FIFO_B$ initially empty, \overline{SO}_A held HIGH in anticipation of data.
- Load one word into FIFO_A; SI pulse applied, results in DIR pulse.
- Data out _A/data in _B transition; valid data arrives at FIFO_A output stage after a specified delay of the DOR flag, meeting data input set-up requirements of FIFO_B.
- DOR_A and SI_B pulse HIGH; (ripple through delay after SI_A LOW) data is unloaded from FIFO_A as a result of the data output ready pulse, data is shifted into FIFO_B.
- 5. DIR_B and \overline{SO}_A go LOW; flag indicates input stage of FIFO_B is busy, shift-out of FIFO_A is complete.
- 6. DIR_B and \overline{SO}_A go HIGH automatically; the input stage of FIFO_B is again able to receive data, \overline{SO} is held HIGH in anticipation of additional data.
- DOR_B goes HIGH; (ripple through delay after SI_B LOW) valid data is present one propagation delay later at the FIFO_B output stage.



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Notes to Fig.21

- FIFO_A and FIFO_B initially full, SI_B held HIGH in anticipation of shifting in new data as empty location bubbles-up.
- Unload one word from FIFO_B; SO pulse applied, results in DOR pulse.
- 3. DIR_B and \overline{SO}_A pulse HIGH; (bubble-up delay after \overline{SO}_B LOW) data is loaded into FIFO_B as a result of the DIR pulse, data is shifted out of FIFO_A.
- DOR_A and SI_B go LOW; flag indicates the output stage of FIFO_A is busy, shift-in to FIFO_B is complete.
- DOR_A and SI_B go HIGH; flag indicates valid data is again available at FIFO_A output stage, SI_B is held HIGH, awaiting bubble-up of empty location.
- DIR_A goes HIGH; (bubble-up delay after SO_A LOW) an empty location is present at input stage of FIFO_A.



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PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".





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Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

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