

# PCA2002

## 32 kHz watch circuit with programmable output period and pulse width

Rev. 9 — 6 December 2019

Product data sheet

### 1. General description

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The PCA2002 is a CMOS<sup>1</sup> integrated circuit for battery operated wrist watches with a 32 kHz quartz crystal as the timing element and a bipolar stepping motor. The quartz crystal oscillator and the frequency divider are optimized for minimum current consumption. A timing accuracy of 1 ppm is achieved with a programmable, digital frequency adjustment.

The output period and the output pulse width can be programmed. It can be selected between a full output pulse or a chopped output pulse with a duty cycle of 75 %. In addition, a stretching pulse can be added to the primary driving pulse.

A pad RESET is provided (used for stopping the motor) for accurate time setting and for accelerated testing of the watch.

### 2. Features and benefits

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- Amplitude-regulated 32 kHz quartz crystal oscillator, with excellent frequency stability and high immunity to leakage currents
- Electrically programmable time calibration with 1 ppm resolution stored in One Time Programmable (OTP) memory
- The quartz crystal is the only external component required
- Very low current consumption: typically 90 nA
- Output pulses for bipolar stepping motors
- Five different programmable output periods (1 s to 30 s)
- Output pulse width programmable between 1 ms and 8 ms
- Full or chopped motor pulse and pulse stretching, selectable
- Stop function for accurate time setting and current saving during shelf life
- Test mode for accelerated testing of the mechanical parts of the watch
- Test bits for type recognition

### 3. Applications

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- Driver circuits for bipolar stepping motors
- High immunity motor drive circuits
- High production volumes

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1. The definition of the abbreviations and acronyms used in this data sheet can be found in [Section 14](#).



## 4. Ordering information

Table 1. Ordering information

Type number	Topside marking <sup>[1]</sup>	Package		
		Name	Description	Version
PCA2002U/AB/1	PC 2002-1	wire bond die	8 bonding pads; 1.16 × 0.86 × 0.22 mm	PCA200xU
PCA2002U/10AB/1	PC 2002-1	wire bond die	8 bonding pads; 1.16 × 0.86 × 0.22 mm	PCA200xU
PCA2002DUS/DA	PC 2002-1	WLCSP8	wafer level chip-size package; 8 bumps; 1.16 mm x 0.86 mm	SOT1455-1

[1] Marking "PC2002-1" on active side of die

### 4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA2002U/AB/1	PCA2002U/AB/1,026	wire bond die	bare die; chip in tray	36000	T <sub>amb</sub> = -10 °C to +60 °C
PCA2002U/10AB/1	PCA2002U/10AB/1,00	wire bond die	sawn wafer on Film Frame Carrier (FFC), see <a href="#">Figure 17</a>	45192	T <sub>amb</sub> = -10 °C to +60 °C
PCA2002DUS/DA	PCA2002DUS/DAZ	WLCSP8	Reel 7" Q1 in tape reel dry pack	4000	T <sub>amb</sub> = -10 °C to +60 °C

5. Block diagram

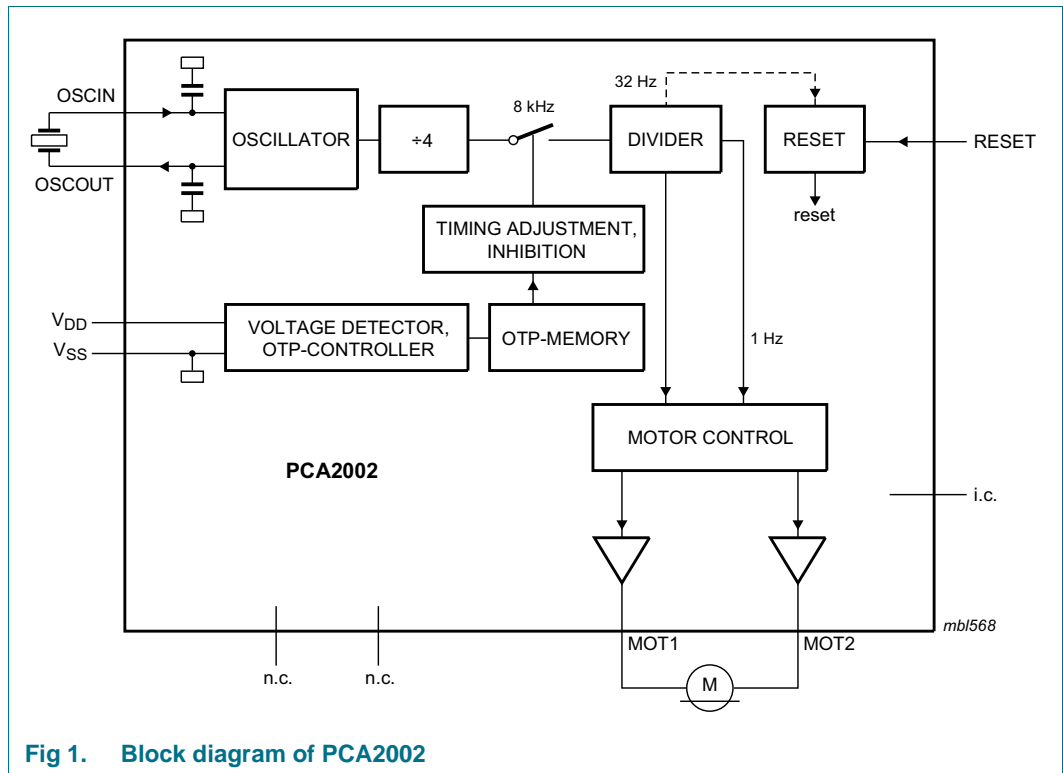
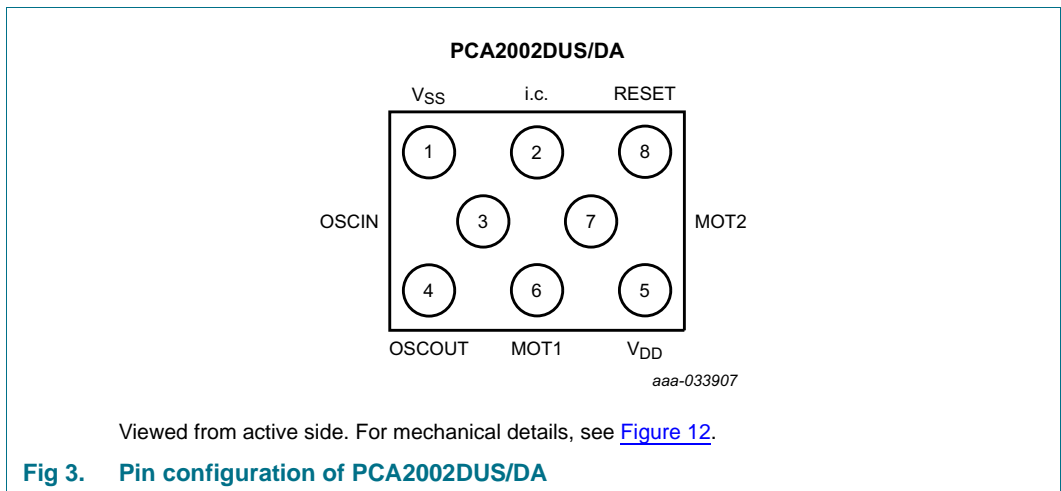
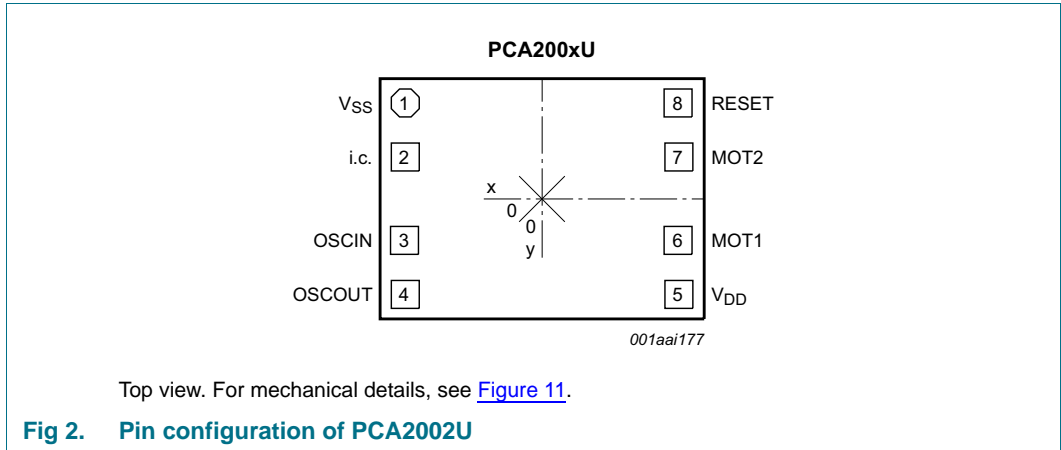


Fig 1. Block diagram of PCA2002

## 6. Pinning information

### 6.1 Pinning



## 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$V_{SS}$ <sup>[1]</sup>	1	ground
i.c. <sup>[2]</sup>	2	internally connected
OSCIN	3	oscillator input
OSCOUT	4	oscillator output
$V_{DD}$	5	supply voltage
MOT1	6	motor 1 output
MOT2	7	motor 2 output
RESET	8	reset input

[1] The substrate (rear side of the chip) is connected to  $V_{SS}$ . Therefore the die pad must be either floating or connected to  $V_{SS}$ .

[2] Pad i.c. is used for factory tests; in normal operation it should be left open-circuit, and it has an internal pull-down resistance to  $V_{SS}$ .

## 7. Functional description

### 7.1 Motor pulse

The motor driver delivers pulses with an alternating polarity. The output waveform across the motor terminals is illustrated in [Figure 4](#). Between the motor pulses, both terminals are connected to  $V_{DD}$ , which means that the motor is short-circuit.

The following parameters can be selected and are stored in a One Time Programmable (OTP) memory:

- Output periods of 1 s, 5 s, 10 s, 20 s and 30 s
- Pulse width ( $t_p$ ) between 0.98 ms and 7.8 ms in steps of 0.98 ms
- Full or chopped (75 %) output pulse
- Pulse stretching: an enlargement pulse is added to the primary motor pulse. This enlargement pulse has a duty cycle of 25 % and a width, which is twice the programmed motor pulse width.

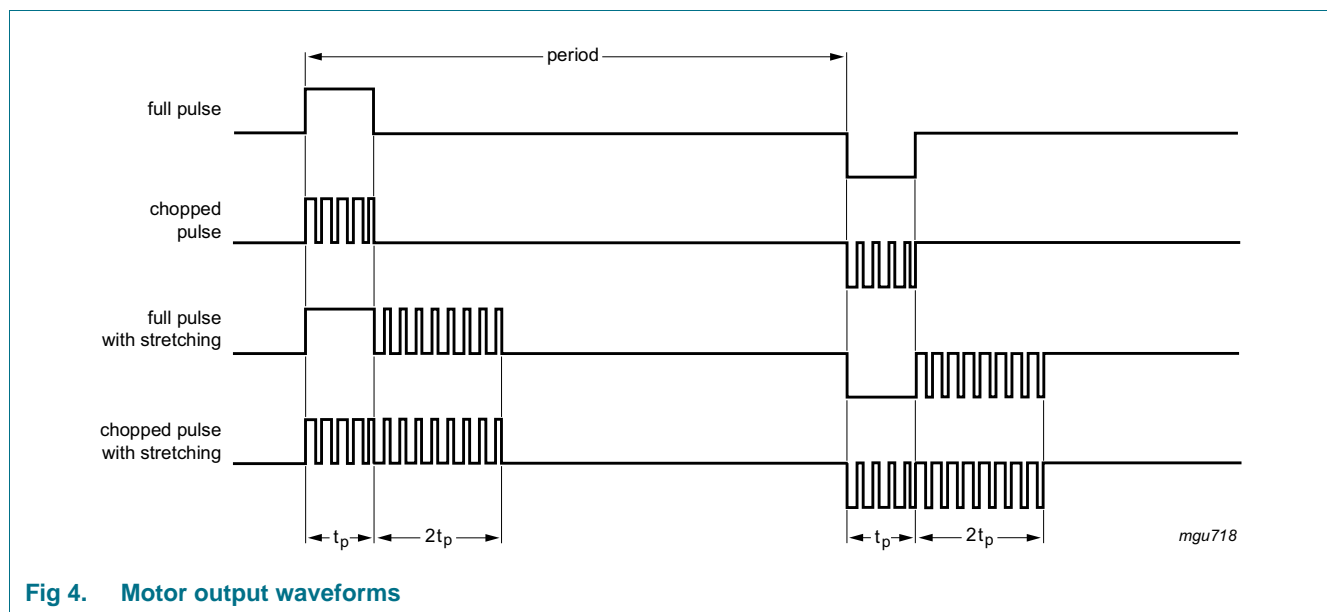


Fig 4. Motor output waveforms

### 7.2 Time calibration

The quartz crystal oscillator has an integrated capacitance of 5.2 pF, which is lower than the specified capacitance ( $C_L$ ) of 8.2 pF for the quartz crystal (see [Table 10](#)). Therefore, the oscillator frequency is typically 60 ppm higher than 32.768 kHz. This positive frequency offset is compensated by removing the appropriate number of 8192 Hz pulses in the divider chain (maximum 127 pulses), every 1 or 2 minutes. The time correction is given in [Table 4](#).

**Table 4. Time calibration**

Calibration period	Correction per step (n = 1)		Correction per step (n = 127)	
	ppm	seconds per day	ppm	seconds per day
1 minute	2.03	0.176	258	22.3
2 minutes	1.017	0.088	129	11.15

After measuring the effective oscillator frequency, the number of correction pulses must be calculated and stored together with the calibration period in the OTP memory (see [Section 7.6](#)).

The oscillator frequency can be measured at pad RESET, where a square wave signal with the frequency of  $\frac{1}{1024} \times f_{osc}$  is provided.

This frequency shows a jitter every minute or every two minutes, depending on the programmed calibration period, which originates from the time calibration.

Details on how to measure the oscillator frequency and the programmed inhibition time are given in [Section 7.10](#).

### 7.3 Reset

At pin RESET an output signal with a frequency of  $\frac{1}{1024} \times f_{osc} = 32Hz$  is provided.

Connecting pin RESET to V<sub>DD</sub> stops the motor drive and opens the motor switches.

After releasing pin RESET, the first motor pulse is generated exactly one period later with the opposite polarity to the last pulse before stopping. The debounce time for the reset function is between 31 ms and 62 ms.

Connecting pin RESET to V<sub>SS</sub> activates the test mode. In this mode the motor output frequency is 32 Hz, which can be used to test the mechanical function of the watch.

### 7.4 Programming possibilities

The programming data is organized in an array of 8-bit words (see [Table 5](#)): Word A contains the time calibration, word B the setting for the monitor pulses, word C is not used and word D contains the type recognition.

**Table 5. Words and bits**

Word	Bit							
	1	2	3	4	5	6	7	8
A	number of 8192 Hz pulses to be removed							calibration period
B	pulse width			output period			duty cycle	pulse stretching
C								
D	type				factory test bit			

Table 6. Description of word A bits

Bit	Value	Description
<b>Inhibit time</b>		
1 to 7	-	adjust the number of the 8192 Hz pulses to be removed; bit 1 is the MSB and bit 7 is the LSB
<b>Calibration period</b>		
8	0	1 minute
	1	2 minutes

Table 7. Description of word B bits

Bit	Value	Description
<b>Pulse width <math>t_p</math> (ms)</b>		
1 to 3	000	0.98
	001	1.95
	010	2.9
	011	3.9
	100	4.9
	101	5.9
	110	6.8
	111	7.8
<b>Output period (s)</b>		
4 to 6	000	1
	001	5
	010	10
	011	20
	100	30
<b>Duty cycle of motor pulse</b>		
7	0	75 %
	1	100 %
<b>Pulse stretching</b>		
8	0	no pulse stretching
	1	a pulse width of $2 \times t_p$ and a duty factor of 25 % are added

## 7.5 Type recognition

Byte D is read to determine, which type of the PCA200x family is used in a particular application.

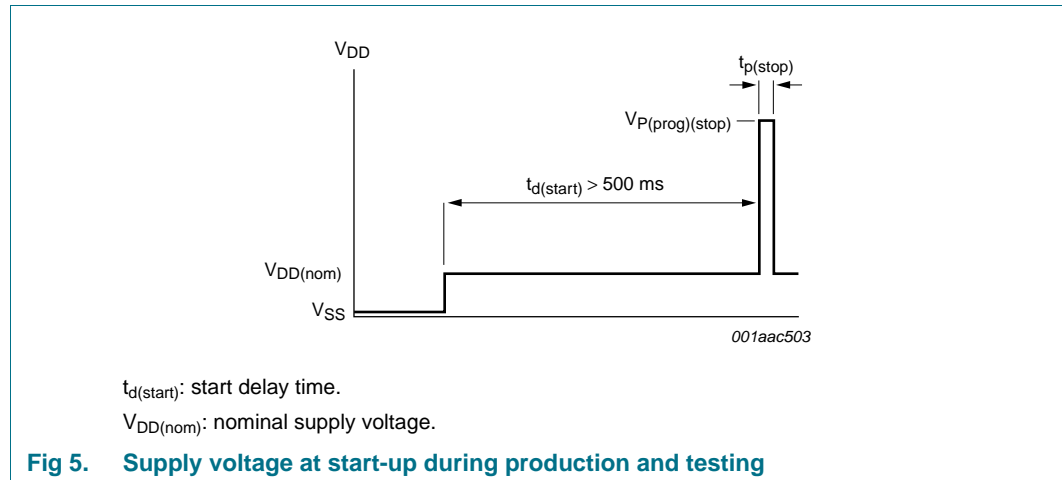
Table 8. Description of word D bits

Bit	Value	Description
<b>Type recognition</b>		
1 to 4	0000	PCA2002
	1000	PCA2000
	0100	PCA2001
	1100	PCA2003



## 7.6 Programming procedure

To ensure that the oscillator starts up correctly you must execute a reset sequence (see [Figure 5](#)).



**Fig 5. Supply voltage at start-up during production and testing**

For a watch it is essential that the timing calibration can be made after the watch is fully assembled. In this situation, the supply pins are often the only terminals which are still accessible.

Writing to the OTP cells and performing the related functional checks is achieved in the PCA2002 by modulating the supply voltage. The necessary control circuit consists basically of a voltage level detector, an instruction counter, which determines the function to be performed, and an 8-bit shift register, which allows writing the OTP cells of an 8-bit word in one step and which acts as data pointer for checking the OTP content.

- State 1; measurement of the crystal oscillator frequency (divided by 1024)
- State 2; measurement of the inhibition time
- State 3; write/check word A
- State 4; write/check word B
- State 5; check word C (don't care since no meaning)
- State 6; check word D (type recognition)

Each instruction state is switched on with a pulse to  $V_{P(prog)(start)}$ . After this large pulse, an initial waiting time of  $t_0$  is required. The programming instructions are then entered by modulating the supply voltage with small pulses (amplitude  $V_{P(mod)}$  and pulse width  $t_{mod}$ ). The first small pulse defines the start time, the following pulses perform three different functions, depending on the time delay ( $t_d$ ) from the preceding pulse (see [Figure 6](#), [Figure 7](#), [Figure 8](#), [Figure 9](#) and [Figure 10](#)):

- $t_d = t_1$  (0.7 ms); increments the instruction counter
- $t_d = t_2$  (1.7 ms); clocks the shift register with data = logic 0
- $t_d = t_3$  (2.7 ms); clocks the shift register with data = logic 1

The programming procedure requires a stable oscillator, which means that a waiting time, determined by the start-up time of the oscillator, is necessary after power-up of the circuit.

After the  $V_{P(prog)(start)}$  pulse, the instruction counter is in state 1 and the data shift register is cleared.

The instruction state ends with a second pulse to  $V_{P(prog)(stop)}$  or with the pulse to  $V_{store}$ .

In any case, the instruction states are terminated automatically 2 seconds after the last supply modulation pulse.

### 7.7 Programming the memory cells

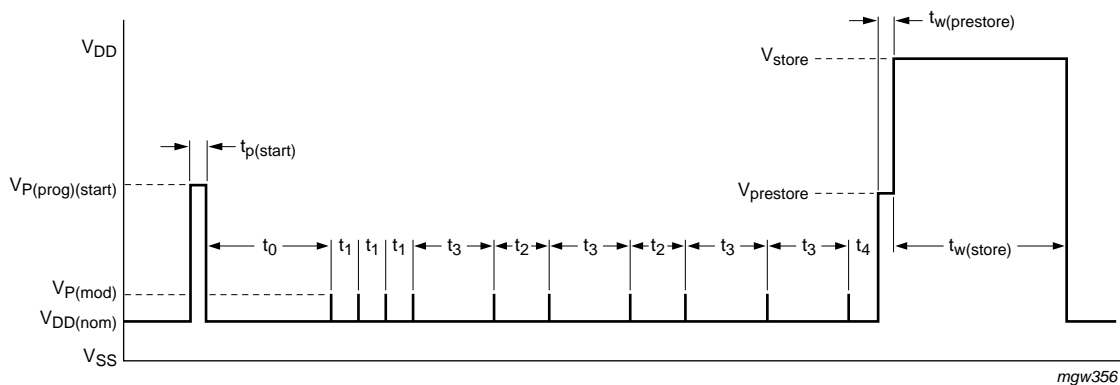
Applying the two-stage programming pulse (see [Figure 6](#)) transfers the stored data in the shift register to the OTP cells.

Perform the following to program a memory word:

1. Starting with a  $V_{P(prog)(start)}$  pulse, wait for the time period  $t_0$  then set the instruction counter to the word to be written ( $t_d = t_1$ ).
2. Enter the data to be stored into the shift register ( $t_d = t_2$  or  $t_3$ ), LSB first (bit 8) and MSB last (bit 1).
3. Applying the two-stage programming pulse  $V_{prestore}$  followed by  $V_{store}$  stores the word. The delay between the last data bit and the pre-store pulse  $V_{prestore}$  is  $t_d = t_4$ . Store the word by raising the supply voltage to  $V_{store}$ ; the delay between the last data bit and the store pulse is  $t_d$ .

The example shown in [Figure 6](#) performs the following functions:

- Start
- Setting the instruction counter to state 4 (word B)
- Entering data word 110101 into the shift register (sequence: LSB first and MSB last)
- Writing the OTP cells for word B



The example shows the programming of B = 110101 (the sequence is MSB first and LSB last).

$V_{DD(nom)}$ : nominal supply voltage.

**Fig 6. Supply voltage modulation for programming**

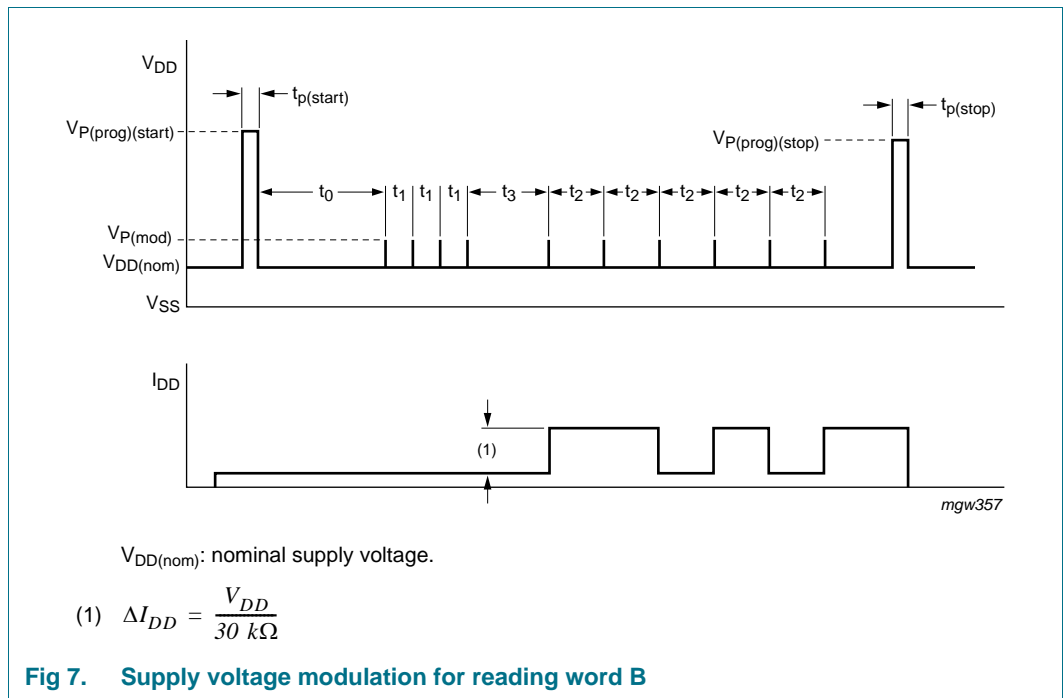
### 7.8 Checking the memory content

The stored data of the OTP array can be checked bit wise by measuring the supply current (see [Figure 7](#)). The array word is selected by the instruction state and the bit is addressed by the shift register.

To read a word, the word is first selected ( $t_d = t_1$ ) and a logic 1 is written into the first cell of the shift register ( $t_d = t_3$ ). This logic 1 is then shifted through the entire shift register ( $t_d = t_2$ ), so that it points with each clock pulse to the next bit.

If the addressed OTP cell contains a logic 1, a 30 kΩ resistor is connected between  $V_{DD}$  and  $V_{SS}$ ; this increases the supply current accordingly.

[Figure 7](#) shows the supply voltage modulation for reading word B, with the corresponding supply current variation for word B = 110101 (sequence: first MSB and last LSB).



**Fig 7. Supply voltage modulation for reading word B**

### 7.9 Frequency tuning at assembled watch

Figure 8 shows the test set-up for frequency tuning the assembled watch.

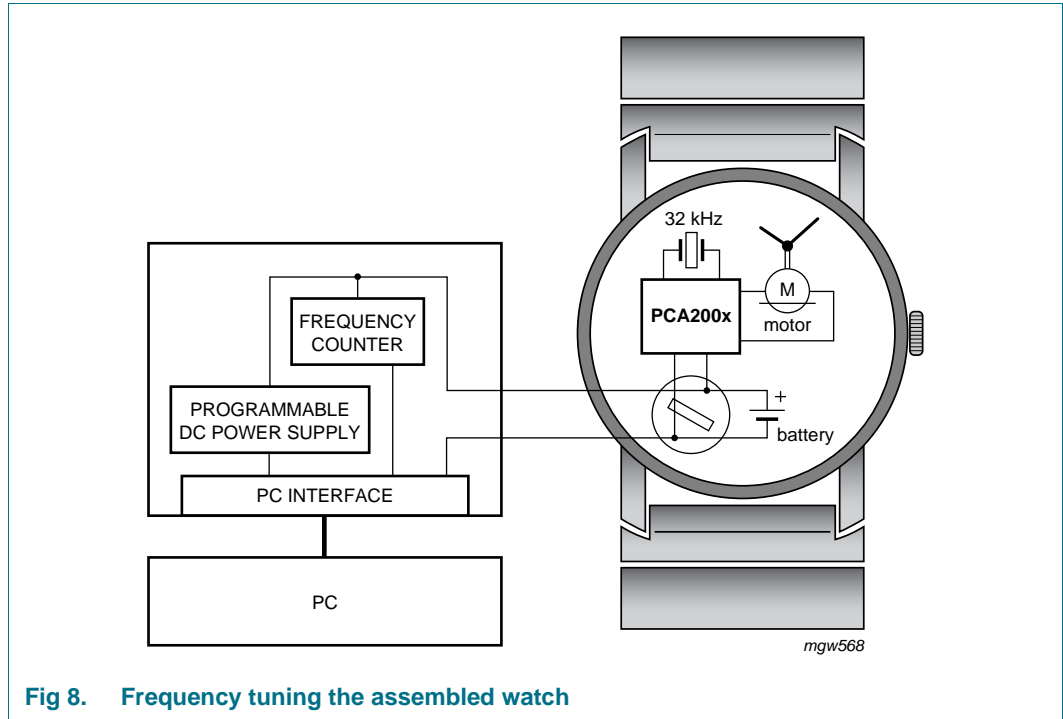


Fig 8. Frequency tuning the assembled watch

### 7.10 Measurement of the oscillator frequency and the inhibition time

The output of the two measuring states can either be monitored directly at pin RESET or as a modulation of the supply current (a modulating resistor of 30 kΩ is connected between V<sub>DD</sub> and V<sub>SS</sub> when the signal at pin RESET is at HIGH-level).

The supply voltage modulation must be followed as shown in Figure 5 in order to guarantee the correct start-up of the circuit during production and testing.

Measuring states:

- State 1; quartz crystal oscillator frequency divided by 1024; state 1 starts with a pulse to V<sub>P</sub> and ends with a second pulse to V<sub>P</sub>
- State 2; inhibition time has a value of n × 0.122 ms. A signal with the periodicity of 31.25 ms + n × 0.122 ms appears at pin RESET and as current modulation at pin V<sub>DD</sub> (see Figure 9 and Figure 10)

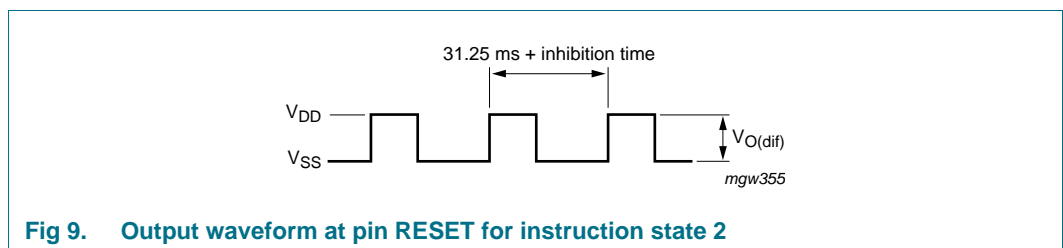
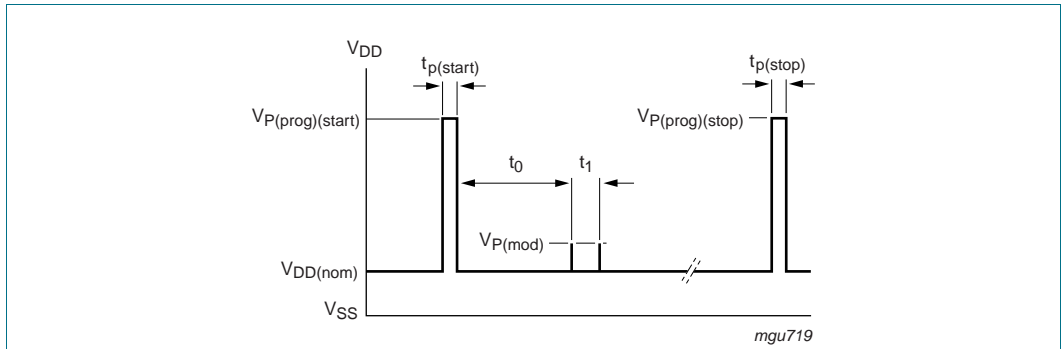


Fig 9. Output waveform at pin RESET for instruction state 2



$V_{DD(nom)}$ : nominal supply voltage.

**Fig 10. Supply voltage modulation for start and stop of instruction state 2**

## 8. Limiting values

**Table 9. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage	$V_{SS} = 0\text{ V}$	[1][2] -1.8	+7.0	V
$V_I$	input voltage		-0.5	+7.5	V
$t_{sc}$	short circuit duration time	output	-	indefinite	s
$V_{ESD}$	electrostatic discharge voltage	HBM	[3] -	±2000	V
		MM	[4] -	±200	V
$I_{lu}$	latch-up current		[5] -	100	mA
$T_{stg}$	storage temperature		[6] -30	+100	°C
$T_{amb}$	ambient temperature		-10	+60	°C

- [1] When writing to the OTP cells, the supply voltage ( $V_{DD}$ ) can be raised to a maximum of 12 V for a time period of 1 s.
- [2] Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows which rapidly discharges the battery.
- [3] Pass level; Human Body Model (HBM), according to [Ref. 6 "JESD22-A114"](#).
- [4] Pass level; Machine Model (MM), according to [Ref. 7 "JESD22-A115"](#).
- [5] Pass level; latch-up testing according to [Ref. 8 "JESD78"](#) at maximum ambient temperature ( $T_{amb(max)}$ ).
- [6] According to the NXP store and transport requirements (see [Ref. 10 "NX3-00092"](#)) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

## 9. Characteristics

**Table 10. Characteristics**

$V_{DD} = 1.55$  V;  $V_{SS} = 0$  V;  $f_{osc} = 32.768$  kHz;  $T_{amb} = 25$  °C; quartz crystal:  $R_s = 40$  k $\Omega$ ,  $C_1 = 2$  fF to 3 fF,  $C_L = 8.2$  pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supplies</b>						
$V_{DD}$	supply voltage	normal operating mode; $T_{amb} = -10$ °C to $+60$ °C	1.1	1.55	3.6	V
$\Delta V_{DD}$	supply voltage variation	$\Delta V/\Delta t = 1$ V/ $\mu$ s	-	-	0.25	V
$I_{DD}$	supply current	between motor pulses	-	90	120	nA
		between motor pulses at $V_{DD} = 3.5$ V	-	120	180	nA
		$T_{amb} = -10$ °C to $+60$ °C	-	-	200	nA
		stop mode; pin RESET connected to $V_{DD}$	-	100	135	nA
<b>Motor output</b>						
$V_{sat}$	saturation voltage	$R_{motor} = 2$ k $\Omega$ ; $T_{amb} = -10$ °C to $+60$ °C	-	150	200	mV
$Z_{o(sc)}$	output impedance (short circuit)	between motor pulses; $I_{motor} < 1$ mA	-	200	300	$\Omega$
<b>Oscillator</b>						
$V_{start}$	start voltage		1.1	-	-	V
$g_m$	transconductance	$V_{i(osc)} \leq 50$ mV(p-p)	5	10	-	$\mu$ S
$t_{startup}$	start-up time		-	0.3	0.9	s
$\Delta f/f$	frequency stability	$\Delta V_{DD} = 100$ mV	-	0.05	0.2	ppm
$C_{L(itg)}$	integrated load capacitance		4.3	5.2	6.3	pF
$R_{par}$	parasitic resistance	allowed resistance between adjacent pins	20	-	-	M $\Omega$
<b>Pad RESET</b>						
$f_o$	output frequency		-	32	-	Hz
$V_{O(dif)}$	differential output voltage	$R_L = 1$ M $\Omega$ ; $C_L = 10$ pF	[1] 1.4	-	-	V
$t_r$	rise time	$R_L = 1$ M $\Omega$ ; $C_L = 10$ pF	[1] -	1	-	$\mu$ s
$t_f$	fall time	$R_L = 1$ M $\Omega$ ; $C_L = 10$ pF	[1] -	1	-	$\mu$ s
$I_{i(AV)}$	average input current	pin RESET connected to $V_{DD}$ or $V_{SS}$	-	10	20	nA

[1]  $R_L$  and  $C_L$  are a load resistor and load capacitor, externally connected to pad RESET.

## 10. OTP programming characteristics

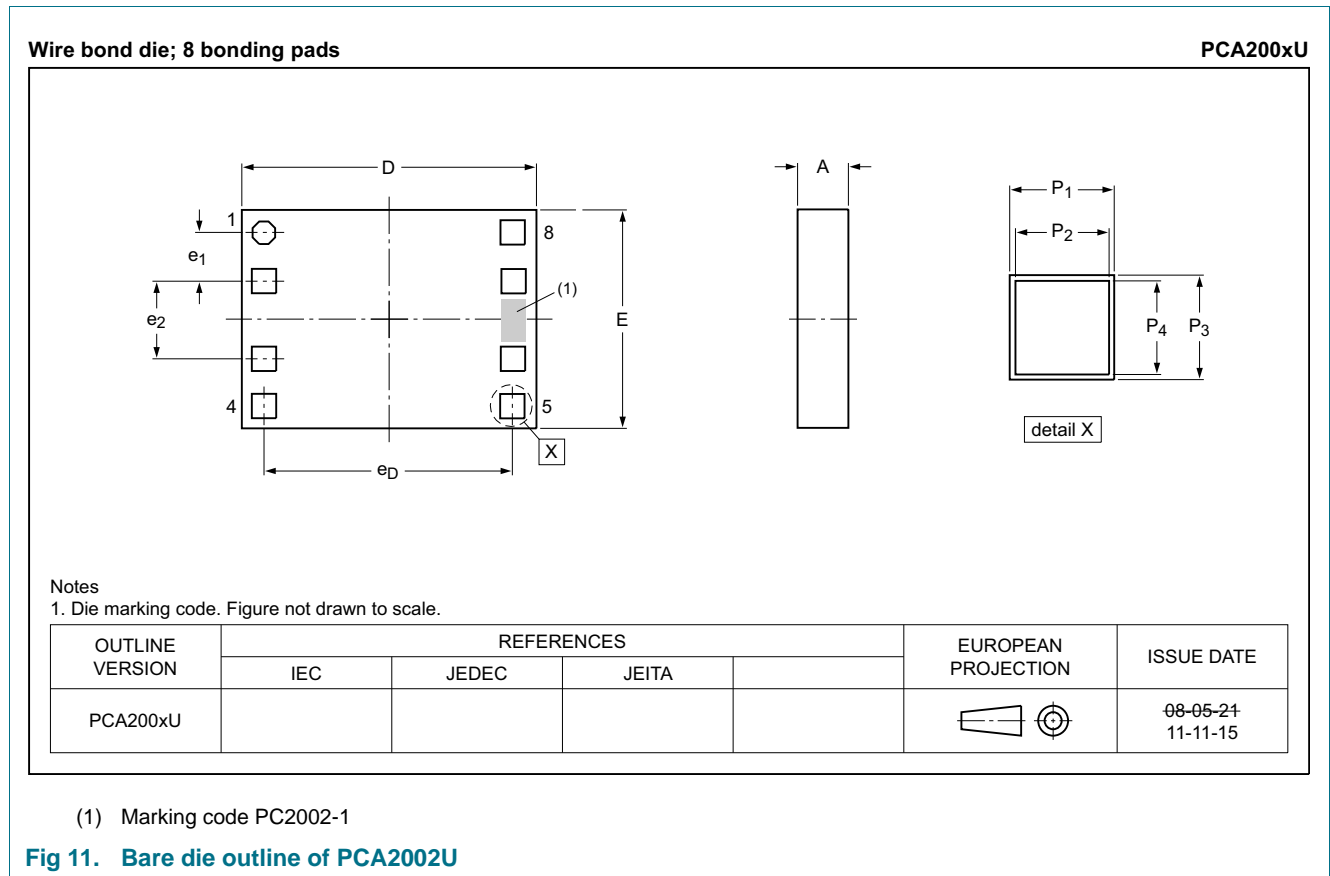
**Table 11. Specifications for OTP programming**

Symbol	Parameter <sup>[1]</sup>	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage	during programming procedure	1.5	-	3.0	V
$V_{P(prog)(start)}$	programming supply voltage (start)		6.6	-	6.8	V
$V_{P(prog)(stop)}$	programming supply voltage (stop)		6.2	-	6.4	V
$V_{P(mod)}$	supply voltage modulation	for entering instructions, referred to $V_{DD}$	320	350	380	mV
$V_{prestore}$	prestore voltage	for prestore pulse	6.2	-	6.4	V
$V_{store}$	supply voltage	for writing to the OTP cells	9.9	10.0	10.1	V
$I_{store}$	store current	for writing to the OTP cells	-	-	10	mA
$t_{p(start)}$	start pulse width		8	10	12	ms
$t_{p(stop)}$	pulse width of stop pulse		0.05	-	0.5	ms
$t_{mod}$	modulation pulse width		25	30	40	$\mu$ s
$t_{w(prestore)}$	prestore pulse width		0.05	-	0.5	ms
$t_{w(store)}$	store pulse width	for writing to the OTP cells	95	100	110	ms
$t_0$	time 0	waiting time after start pulse	20	-	30	ms
$t_1$	time 1	pulse distance for incrementing the state counter	0.6	0.7	0.8	ms
$t_2$	time 2	pulse distance for clocking the data register with data = logic 0	1.6	1.7	1.8	ms
$t_3$	time 3	pulse distance for clocking the data register with data = logic 1	2.6	2.7	2.8	ms
$t_4$	time 4	waiting time for writing to OTP cells	0.1	0.2	0.3	ms
SR	slew rate	for modulation of the supply voltage	0.5	-	5.0	V/ $\mu$ s
$R_{mod}$	modulation resistance	supply current modulation read-out resistor	18	30	45	k $\Omega$

[1] Program each word once only.



### 11. Bare die outline



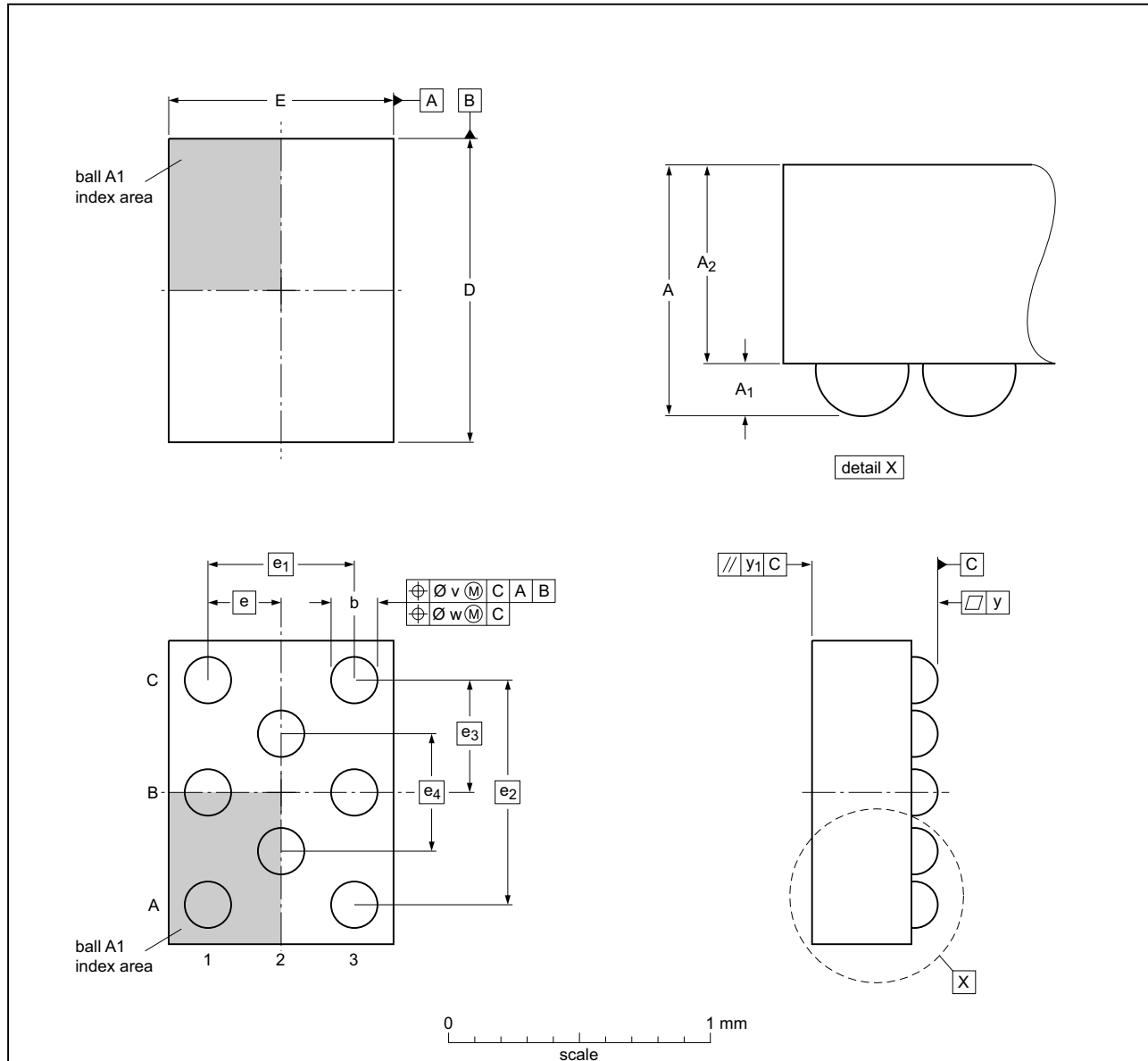
**Table 12. Dimensions of PCA2002U**

Original dimensions are in mm.

Unit (mm)	A	D	E	e <sub>1</sub>	e <sub>2</sub>	e <sub>D</sub>	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	P <sub>4</sub>
max	0.22	-	-	-	-	-	0.099	0.089	0.099	0.089
nom	0.20	1.16	0.86	0.17	0.32	0.96	0.096	0.086	0.096	0.086
min	0.18	-	-	-	-	-	0.093	0.083	0.093	0.083

WLCSP8: wafer level chip-scale package; 8 bumps; 1.16 x 0.86 x 0.48 mm

SOT1455-1



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	A <sub>2</sub>	b	D	E	e	e <sub>1</sub>	e <sub>2</sub>	e <sub>3</sub>	e <sub>4</sub>	v	w	y	y <sub>1</sub>
max	0.505	0.11	0.395	0.1958	1.19	0.89									
nom	0.480	0.10	0.380	0.1780	1.16	0.86	0.28	0.56	0.86	0.43	0.45	0.15	0.05	0.05	0.1
min	0.455	0.09	0.365	0.1602	1.13	0.83									

SOT1455-1\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
					-15-05-04- 15-08-17

Fig 12. Package outline SOT1455-1 (WLCSP8)

## 12. Packing information

### 12.1 Tape and reel information

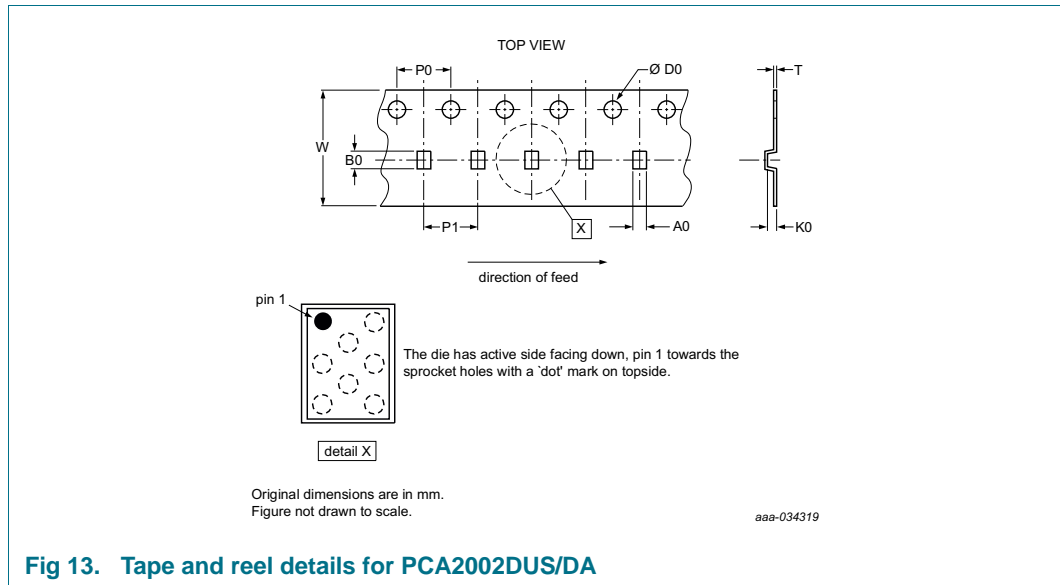


Fig 13. Tape and reel details for PCA2002DUS/DA

Table 13. Carrier tape dimensions of PCA2002DUS/DA

Nominal values with production tolerances.

Symbol	Description	Value	Unit
<b>Compartments</b>			
A0	pocket width in x direction	1.00 ± 0.05	mm
B0	pocket width in y direction	1.30 ± 0.05	mm
K0	pocket depth	0.62 ± 0.05	mm
<b>Overall dimensions</b>			
W	tape width	8	mm
T	tape thickness	0.2 ± 0.02	mm
D0	sprocket hole diameter	1.5	mm
P0	sprocket hole pitch	4 ± 0.1	mm
P1	pocket pitch	4 ± 0.1	mm

## 12.2 Tray information

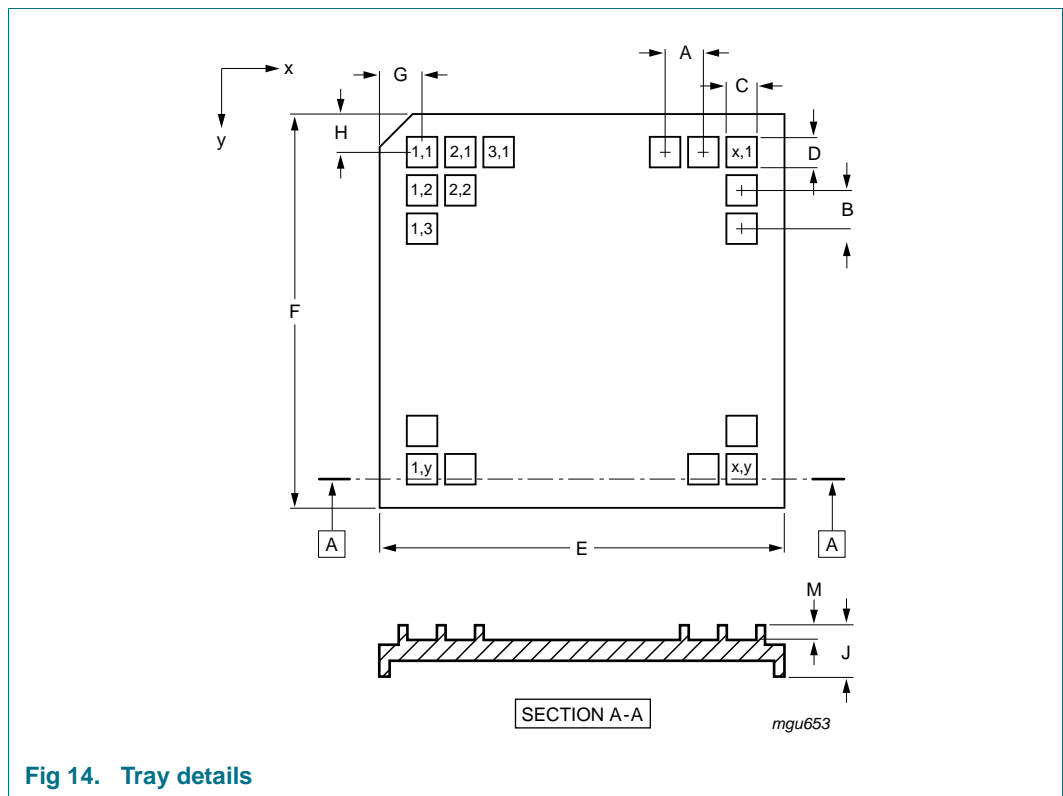
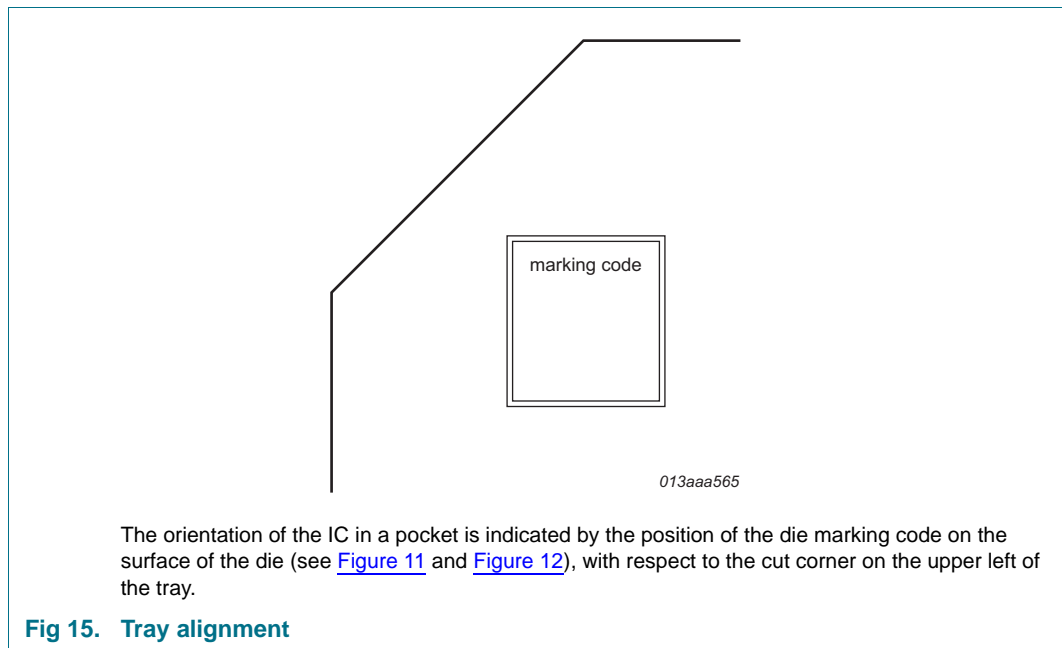


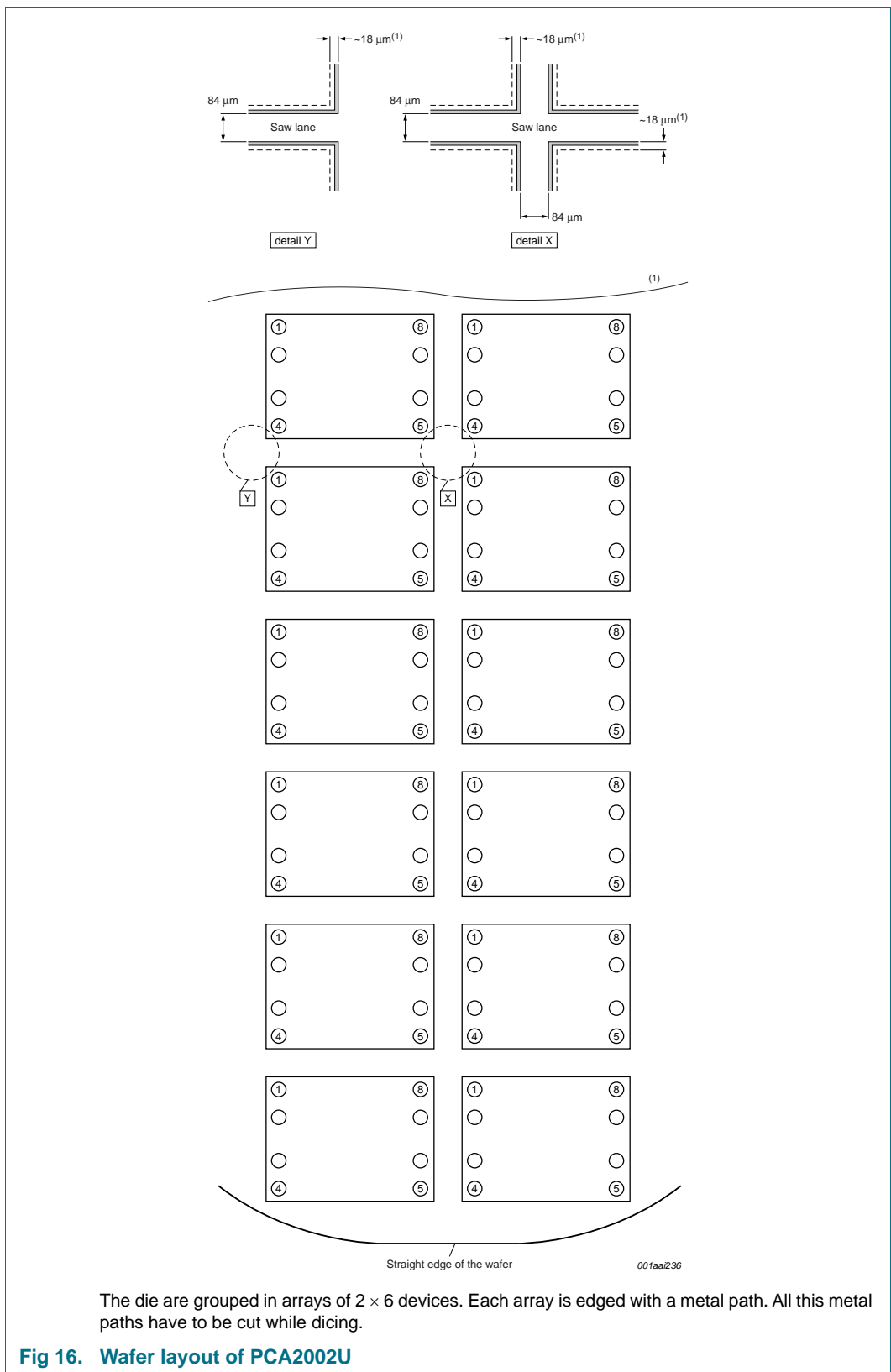
Fig 14. Tray details

Table 14. Tray dimensions

Dimension	Description	Value
A	pocket pitch; x direction	2.15 mm
B	pocket pitch; y direction	2.43 mm
C	pocket width; x direction	1.01 mm
D	pocket width; y direction	1.39 mm
E	tray width; x direction	50.67 mm
F	tray width; y direction	50.67 mm
G	distance from cut corner to pocket (1 and 1) center	4.86 mm
H	distance from cut corner to pocket (1 and 1) center	4.66 mm
J	tray thickness	3.94 mm
M	pocket depth	0.61 mm
x	number of pockets in x direction	20
y	number of pockets in y direction	18

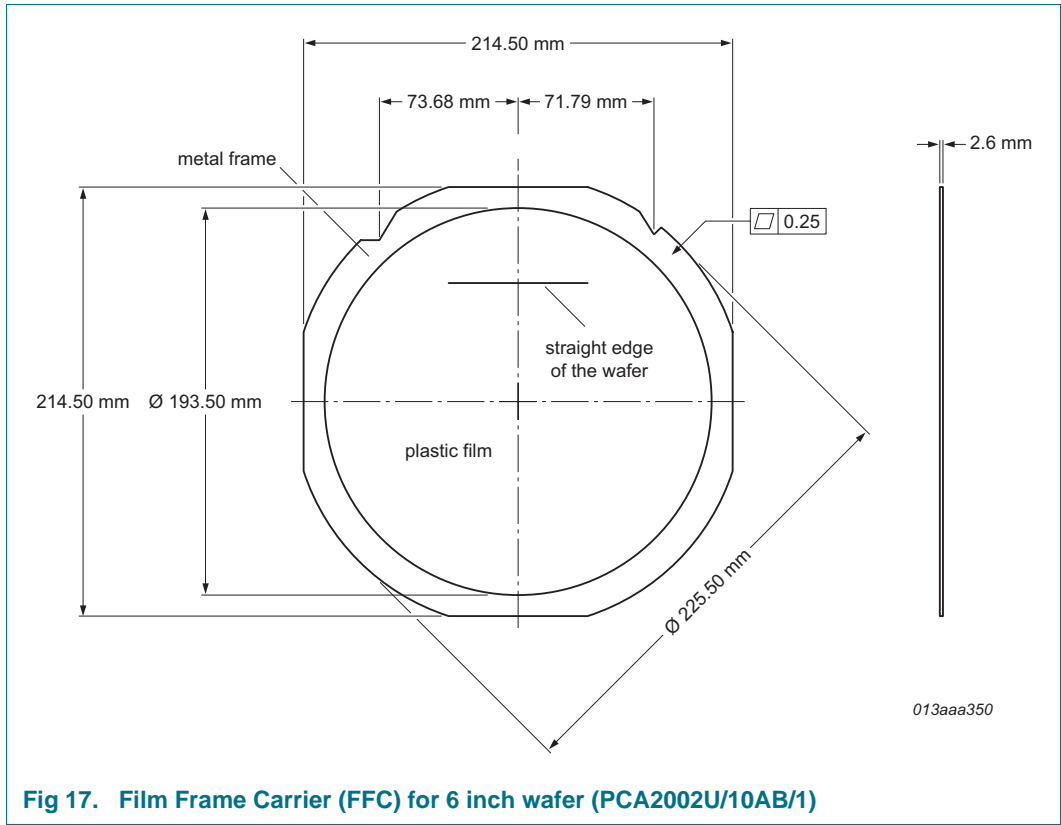


### 12.3 Wafer and Film Frame Carrier (FFC) information



The die are grouped in arrays of 2 × 6 devices. Each array is edged with a metal path. All this metal paths have to be cut while dicing.

**Fig 16. Wafer layout of PCA2002U**



**Table 15. PCA2002 wafer information**

Type number	Wafer thickness	Wafer diameter	FFC for wafer size	Marking of bad die
PCA2002U/10AB/1	0.20 mm	6 inch	6 inch	wafer mapping

## 13. Soldering of WLCSP packages

### 13.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note AN10439 “Wafer Level Chip Scale Package” and in application note AN10365 “Surface mount reflow soldering description”.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

### 13.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

### 13.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 18](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 16](#).

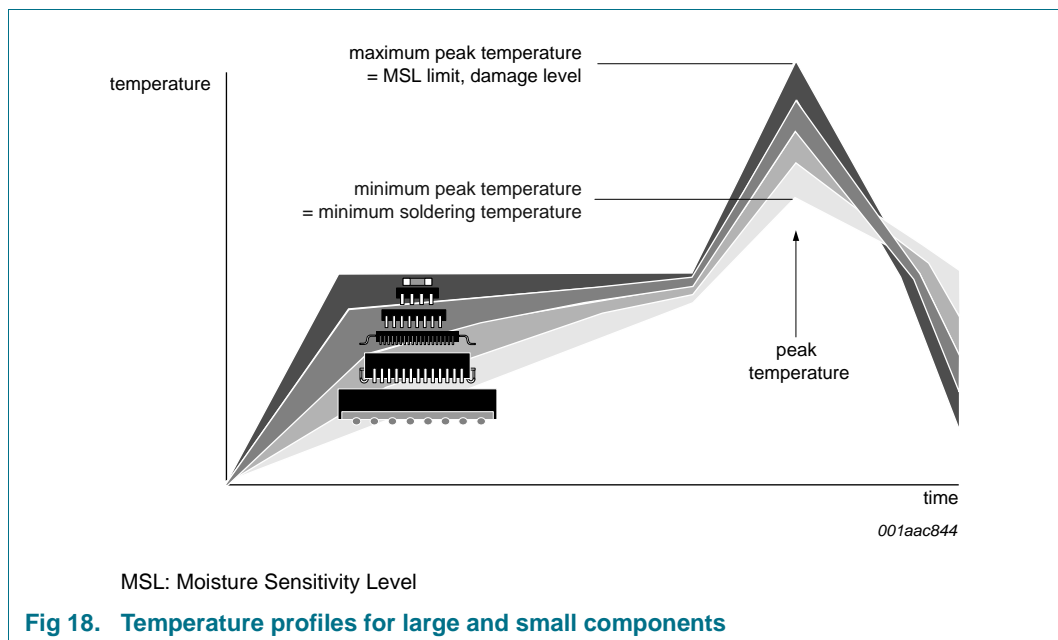
**Table 16. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 18](#).





For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

### 13.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

### 13.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

### 13.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note AN10365 "Surface mount reflow soldering description".

#### 13.3.4 Cleaning

Cleaning can be done after reflow soldering.

## 14. Abbreviations

**Table 17. Abbreviations**

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
FFC	Film Frame Carrier
HBM	Human Body Model
IC	Integrated Circuit
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
OTP	One Time Programmable
PCB	Printed-Circuit Board
TEC	Thermal Expansion Coefficient
WLCSP	Wafer Level Chip-Size Package

## 15. References

- [1] **AN10365** — Surface mount reflow soldering description
- [2] **AN10439** — Wafer Level Chip Size Package
- [3] **AN10706** — Handling bare die
- [4] **IEC 60134** — Rating systems for electronic tubes and valves and analogous semiconductor devices
- [5] **IEC 61340-5** — Protection of electronic devices from electrostatic phenomena
- [6] **JESD22-A114** — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [7] **JESD22-A115** — Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)
- [8] **JESD78** — IC Latch-Up Test
- [9] **JESD625-A** — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- [10] **NX3-00092** — NXP store and transport requirements

## 16. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA2002 v.9	20191206	Product data sheet	-	PCA2002 v.8
Modifications:	<ul style="list-style-type: none"> <li>Removed discontinued parts PCA2002CX8/5/1 and PCA2002CX8/12/1</li> <li>Added PCA2002DUS/DA</li> </ul>			
PCA2002 v.8	20111125	Product data sheet	-	PCA2002 v.7
Modifications:	<ul style="list-style-type: none"> <li>Added die marking codes</li> </ul>			
PCA2002 v.7	20101005	Product data sheet		PCA2002_6
PCA2002_6	20100506	Product data sheet	-	PCA2002_5
PCA2002_5	20081111	Product data sheet	-	PCA2002_4
PCA2002_4	20050907	Product data sheet	-	PCA2002_3
PCA2002_3	20040120	Product specification	-	PCA2002_2
PCA2002_2	20030204	Objective specification	-	PCA2002_1
PCA2002_1	20021025	Objective specification	-	-

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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