RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 107 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 720 to 960 MHz.

780 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 48 Vdc, I_{DQA} = 688 mA, V_{GSB} = 0.6 Vdc, P_{out} = 107 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

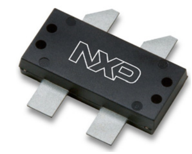
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
733 MHz	17.5	56.3	7.2	–31.3
780 MHz	18.0	55.8	7.2	–36.4
821 MHz	17.4	55.6	6.9	–35.0

Features

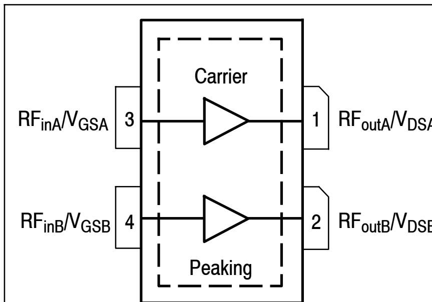
- Advanced high performance in-package Doherty
- Greater negative gate-source voltage range for improved Class C operation
- Designed for digital predistortion error correction systems

A2V09H400-04NR3

720–960 MHz, 107 W AVG., 48 V AIRFAST RF POWER LDMOS TRANSISTOR



OM-780-4L PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +105	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	55, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range [1,2]	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value [2,3]	Unit
Thermal Resistance, Junction to Case Case Temperature 76°C, 107 W Avg., W-CDMA, 48 Vdc, I_{DQA} = 688 mA, V_{GSB} = 0.6 Vdc, 780 MHz	$R_{\theta JC}$	0.50	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Charge Device Model (per JESD22-C101)	C3

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics [4]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 105 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 55 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 137 μAdc)	$V_{GS(th)}$	1.3	1.7	2.3	Vdc
Gate Quiescent Voltage (V_{DD} = 48 Vdc, I_D = 688 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.0	2.5	3.3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.4 Adc)	$V_{DS(on)}$	0.1	0.2	0.4	Vdc
On Characteristics - Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 211 μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.1 Adc)	$V_{DS(on)}$	0.1	0.2	0.5	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
4. Each side of device measured separately.

(continued)

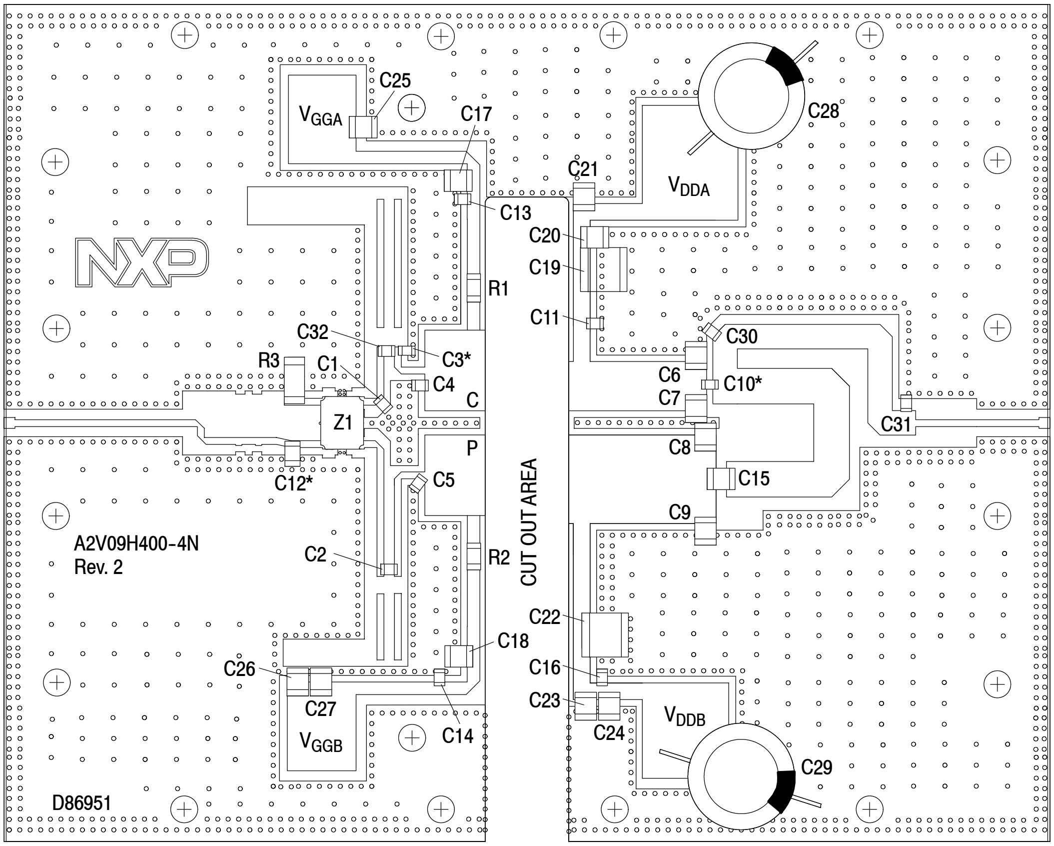
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1,2] (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 688 mA, V_{GSB} = 0.6 Vdc, P_{out} = 107 W Avg., f = 780 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	17.1	17.9	20.0	dB
Drain Efficiency	η_D	51.0	55.8	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.8	7.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	–36.4	–31.0	dBc
Load Mismatch [2] (In NXP Doherty Test Fixture, 50 ohm system) I_{DQA} = 688 mA, V_{GSB} = 0.6 Vdc, f = 780 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 52 Vdc, 437 W Pulsed CW Output Power (3 dB Input Overdrive from 200 W Pulsed CW Rated Power)		No Device Degradation			
Typical Performance [2] (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 688 mA, V_{GSB} = 0.6 Vdc, 733–821 MHz Bandwidth					
P_{out} @ 3 dB Compression Point [3]	P3dB	—	562	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 733-821 MHz frequency range)	Φ	—	–14	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	60	—	MHz
Gain Flatness in 88 MHz Bandwidth @ P_{out} = 107 W Avg.	G_F	—	0.6	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.007	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.003	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2V09H400-04NR3	R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel	OM-780-4L

1. Part internally input matched.
2. Measurement made with device in an asymmetrical Doherty configuration.
3. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



*C3, C10 and C12 are mounted vertically.

Figure 2. A2V09H400-04NR3 Test Circuit Component Layout

Table 7. A2V09H400-04NR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C4, C31	0.5 pF Chip Capacitor	ATC600F0R5BT250XT	ATC
C2, C10, C11, C13, C14, C16, C32	82 pF Chip Capacitor	ATC600F820JT250XT	ATC
C3	12 pF Chip Capacitor	ATC600F120JT250XT	ATC
C5	15 pF Chip Capacitor	ATC600F150JT250XT	ATC
C6, C8	8.2 pF Chip Capacitor	ATC100B8R2JT500XT	ATC
C7	5.6 pF Chip Capacitor	ATC100B5R6BP500XT	ATC
C9	9.1 pF Chip Capacitor	ATC100B9R1CT500XT	ATC
C12	1 pF Chip Capacitor	ATC100B1R0BT500XT	ATC
C15	18 pF Chip Capacitor	ATC100B180JT500XT	ATC
C17, C18	1000 pF Chip Capacitor	ATC800B102JW50XT	ATC
C19, C22	15 μF Chip Capacitor	C5750X7S2A156M230KB	TDK
C20, C21, C23, C24, C25, C26, C27	10 μF Chip Capacitor	GRM32ER61H106KA12L	Murata
C28, C29	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
C30	0.7 pF Chip Capacitor	ATC600F0R7BT250XT	ATC
R1, R2	3 Ω, 1/4 W Chip Resistor	CRCW12063R00JNEA	Vishay
R3	51 Ω, 1/2 W Chip Resistor	CRCW201051R0JNEF	Vishay
Z1	800–1000 MHz Band, 90°, 2 dB Asymmetric Coupler	CMX09Q02	Cemax
PCB	Rogers RO3006, 0.025″, ε_r = 6.5	D86951	MTL

TYPICAL CHARACTERISTICS

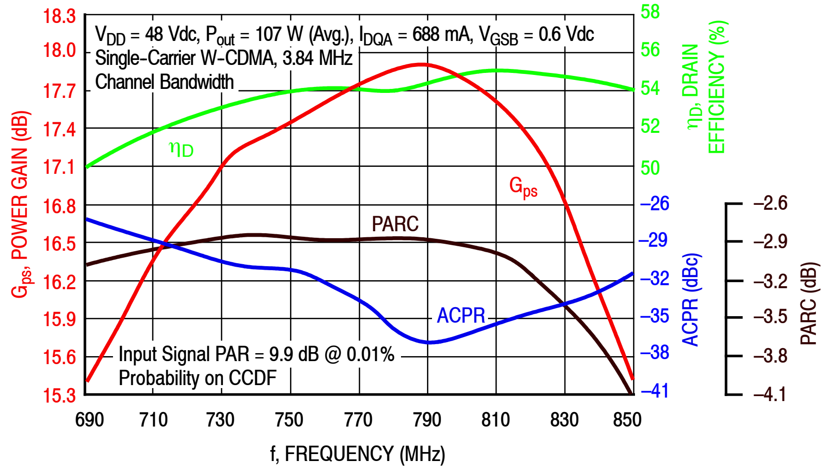


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 107 Watts Avg.

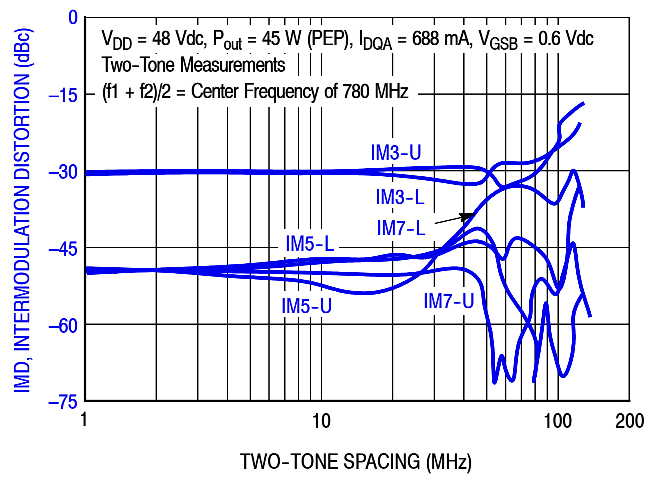


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

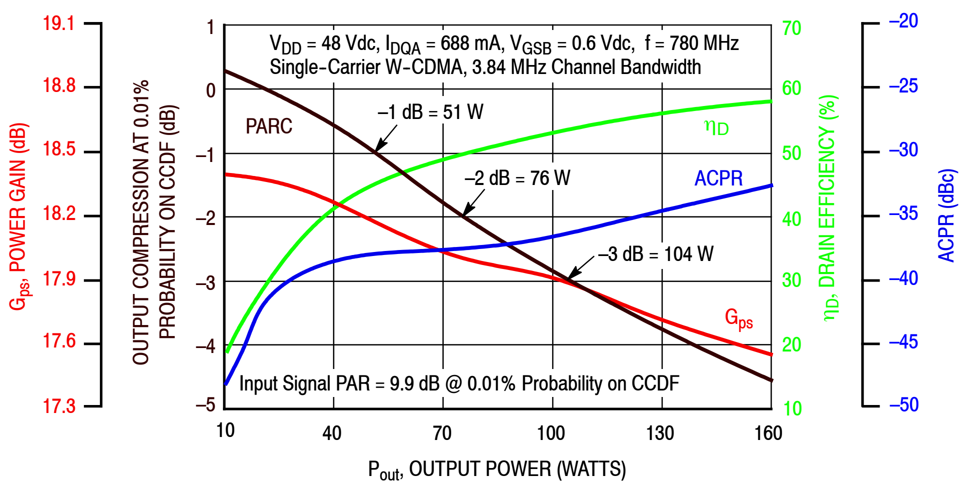


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

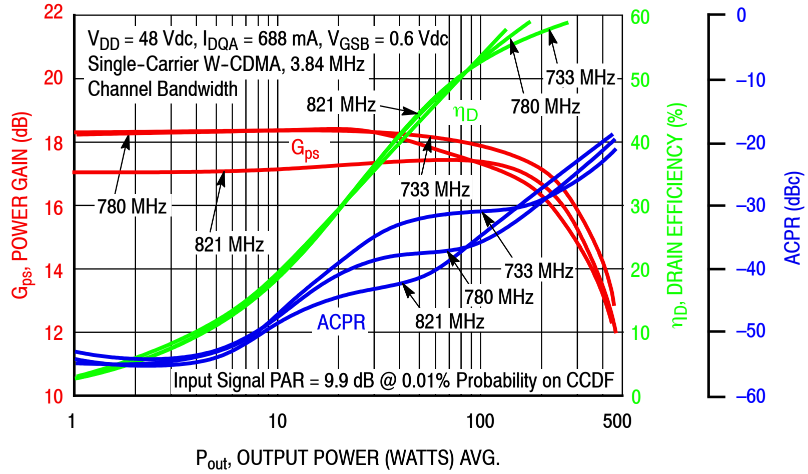


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

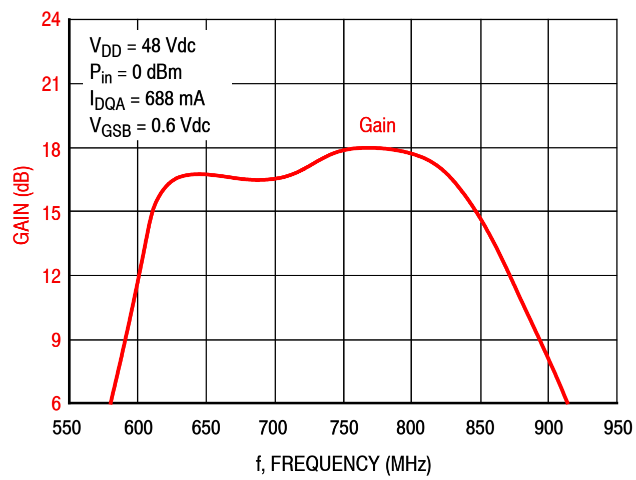


Figure 7. Broadband Frequency Response

Table 8. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQA} = 671 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	4.47 – j2.44	4.03 + j2.52	2.75 – j0.69	19.4	54.2	265	57.5	–10
780	3.47 – j2.93	3.34 + j2.89	2.13 – j0.09	20.4	54.4	275	61.9	–10
822	3.43 – j3.86	3.29 + j3.69	2.20 – j0.30	20.7	54.3	269	61.9	–12

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	4.47 – j2.44	3.75 + j2.70	2.85 – j0.74	17.3	54.9	307	59.5	–11
780	3.47 – j2.93	3.16 + j3.19	2.40 – j0.28	18.3	55.0	319	63.7	–14
822	3.43 – j3.86	3.13 + j4.04	2.40 – j0.48	18.6	54.9	311	63.1	–17

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

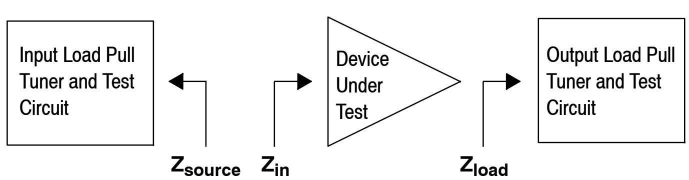
Table 9. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQA} = 671 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	4.47 – j2.44	3.66 + j2.54	2.99 + j1.14	21.1	53.1	203	64.8	–12
780	3.47 – j2.93	2.88 + j3.27	2.32 + j2.37	23.1	51.8	150	72.3	–16
822	3.43 – j3.86	2.85 + j4.05	2.10 + j1.87	23.3	51.9	155	71.9	–20

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	4.47 – j2.44	3.54 + j2.68	2.99 + j0.86	18.9	54.0	252	65.9	–14
780	3.47 – j2.93	3.04 + j3.30	2.92 + j0.91	19.7	54.4	276	72.5	–16
822	3.43 – j3.86	2.91 + j4.24	2.55 + j1.44	20.7	53.4	217	72.0	–22

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 780 MHz

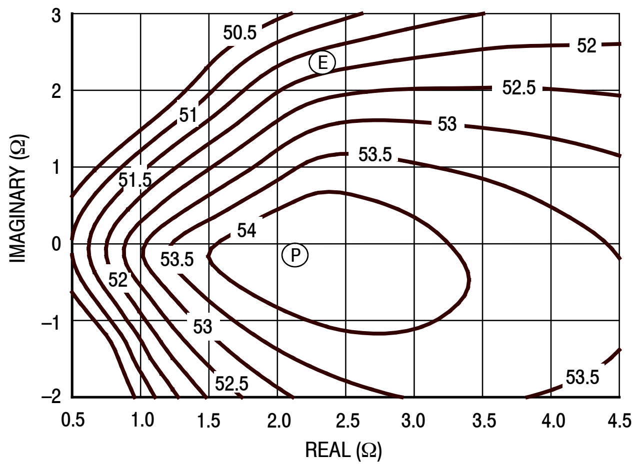


Figure 8. P1dB Load Pull Output Power Contours (dBm)

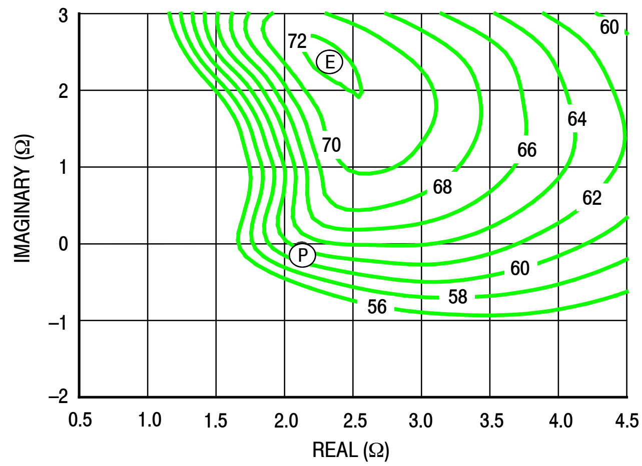


Figure 9. P1dB Load Pull Efficiency Contours (%)

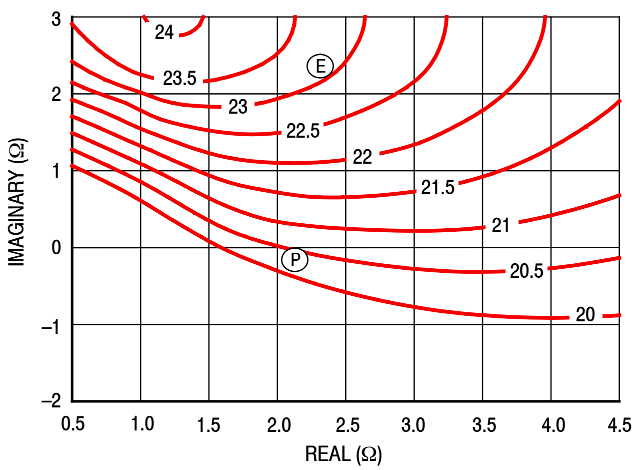


Figure 10. P1dB Load Pull Gain Contours (dB)

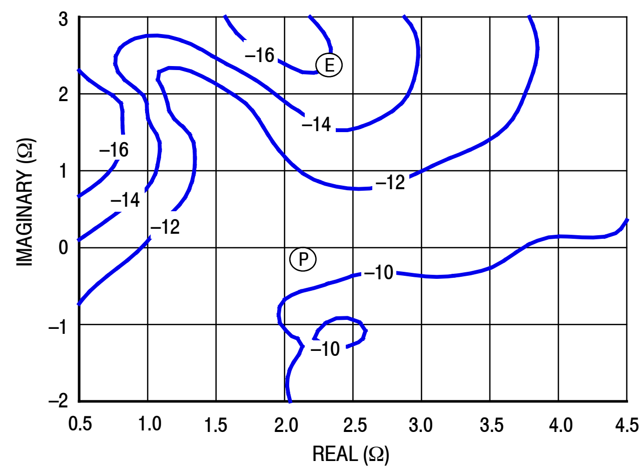


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 780 MHz

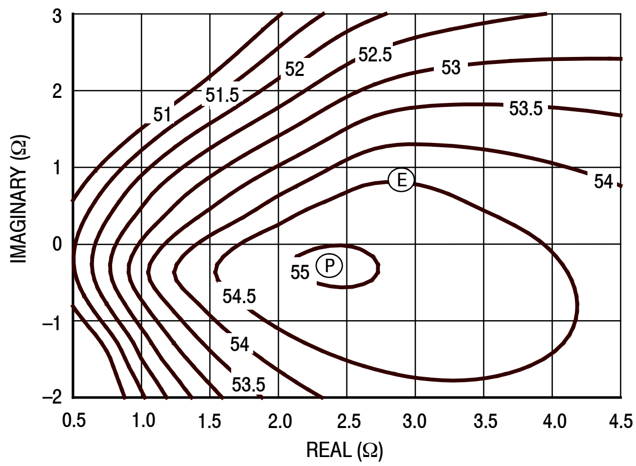


Figure 12. P3dB Load Pull Output Power Contours (dBm)

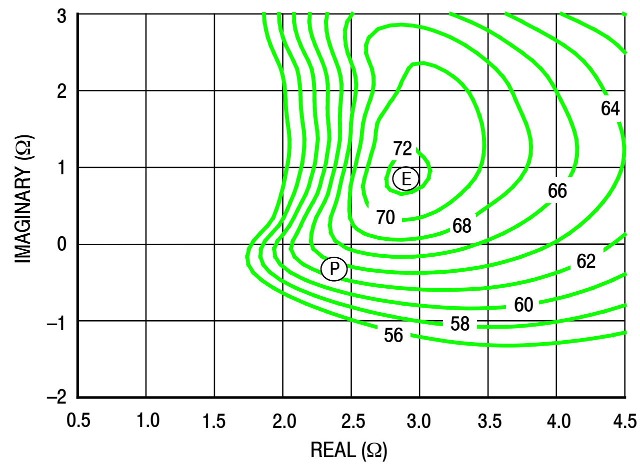


Figure 13. P3dB Load Pull Efficiency Contours (%)

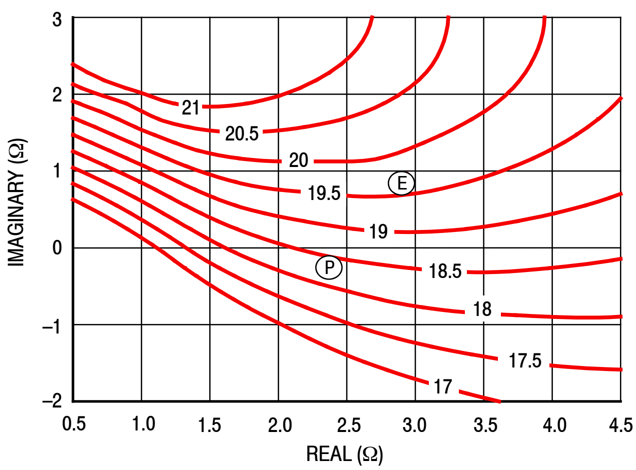


Figure 14. P3dB Load Pull Gain Contours (dB)

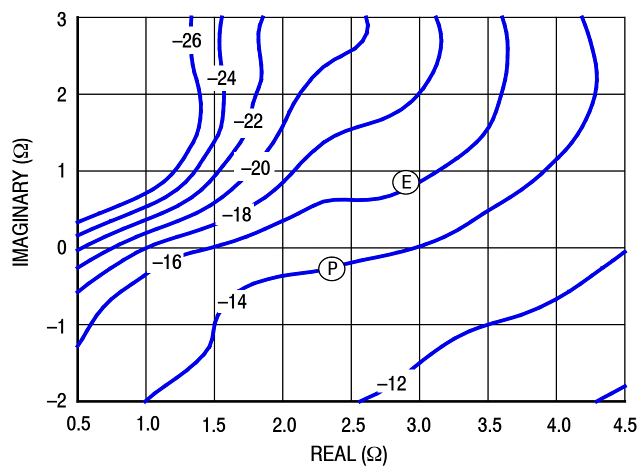


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

Table 10. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, V_{GSB} = 1.4 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	2.73 – j3.69	2.47 + j3.65	1.34 – j0.74	16.6	56.3	424	62.8	–21
780	2.44 – j4.29	2.28 + j4.37	1.34 – j0.92	16.9	56.4	434	62.7	–20
822	2.79 – j4.96	2.32 + j5.16	1.34 – j1.07	17.2	56.2	418	62.5	–20

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	2.73 – j3.69	2.21 + j3.92	1.51 – j1.12	14.2	56.9	490	60.9	–23
780	2.44 – j4.29	2.02 + j4.66	1.50 – j1.02	14.9	57.1	507	65.1	–25
822	2.79 – j4.96	2.08 + j5.50	1.45 – j1.16	15.2	56.9	485	63.8	–26

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

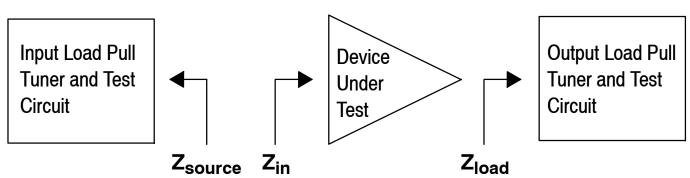
Table 11. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, V_{GSB} = 1.4 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	2.73 – j3.69	2.18 + j3.50	1.66 + j0.50	17.7	54.5	285	74.2	–25
780	2.44 – j4.29	1.97 + j4.28	1.83 + j0.34	18.4	54.9	311	77.2	–23
822	2.79 – j4.96	1.75 + j4.95	1.36 + j0.77	18.8	53.0	200	76.0	–27

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	2.73 – j3.69	2.00 + j3.77	1.87 + j0.45	15.7	55.2	333	73.8	–28
780	2.44 – j4.29	1.85 + j4.60	2.05 – j0.01	16.1	56.0	399	76.3	–27
822	2.79 – j4.96	1.80 + j5.39	1.84 + j0.26	16.7	55.0	314	74.4	–29

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 780 MHz

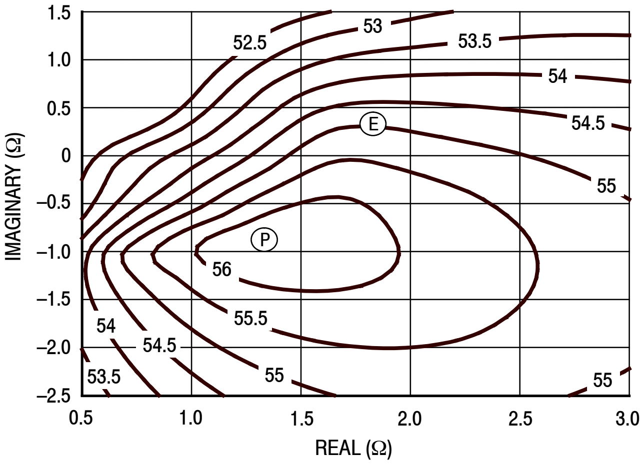


Figure 16. P1dB Load Pull Output Power Contours (dBm)

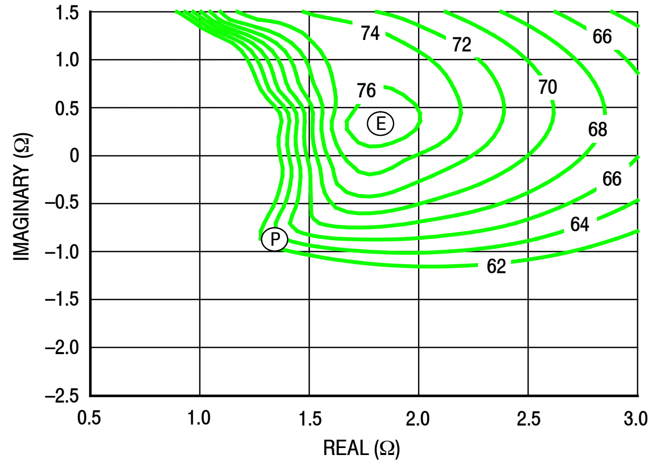


Figure 17. P1dB Load Pull Efficiency Contours (%)

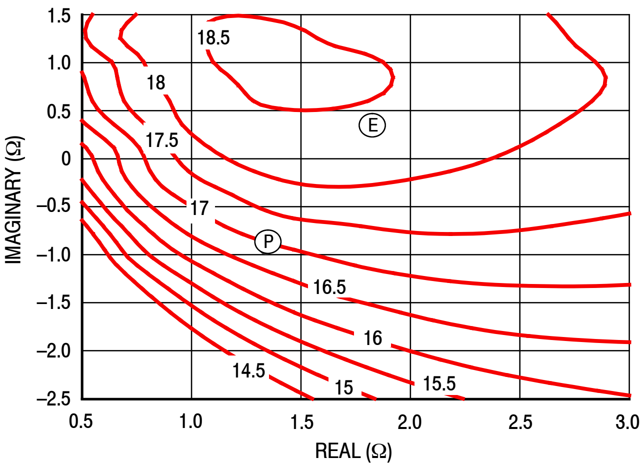


Figure 18. P1dB Load Pull Gain Contours (dB)

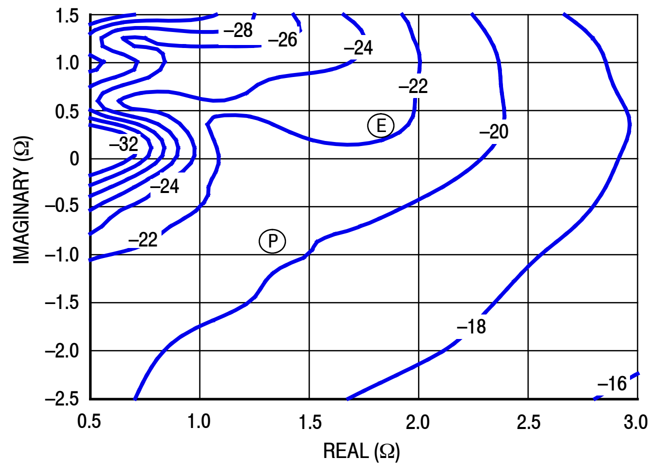


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 780 MHz

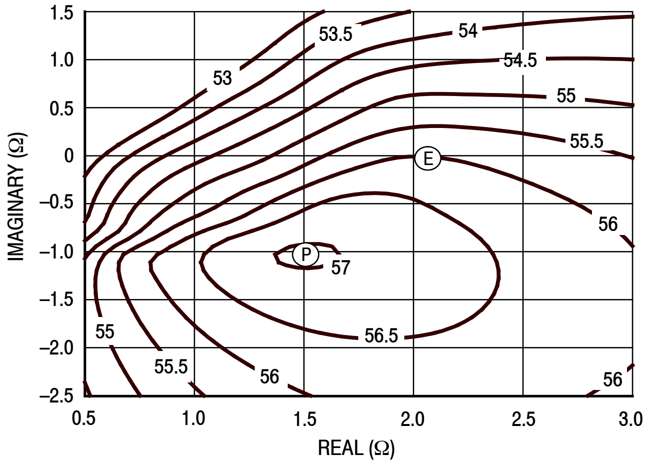


Figure 20. P3dB Load Pull Output Power Contours (dBm)

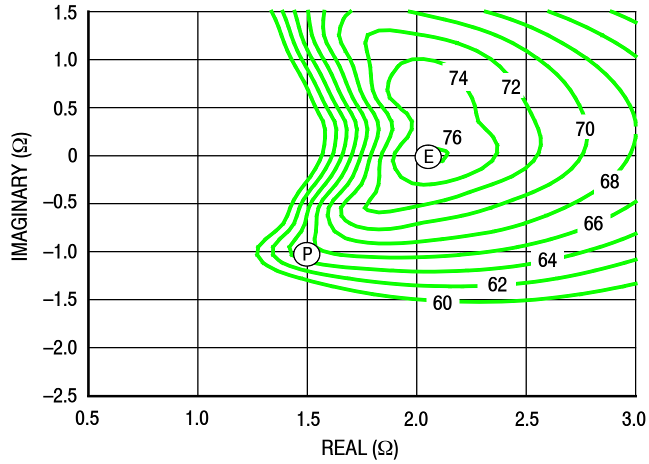


Figure 21. P3dB Load Pull Efficiency Contours (%)

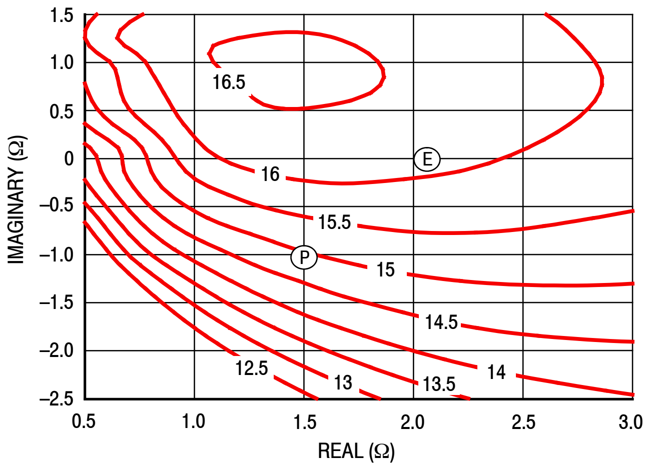


Figure 22. P3dB Load Pull Gain Contours (dB)

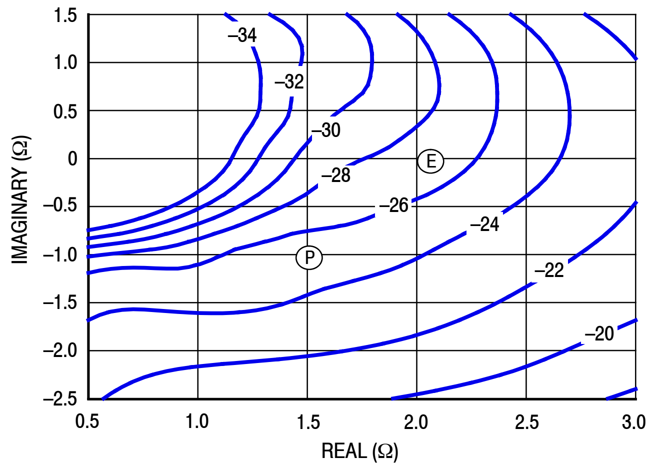


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

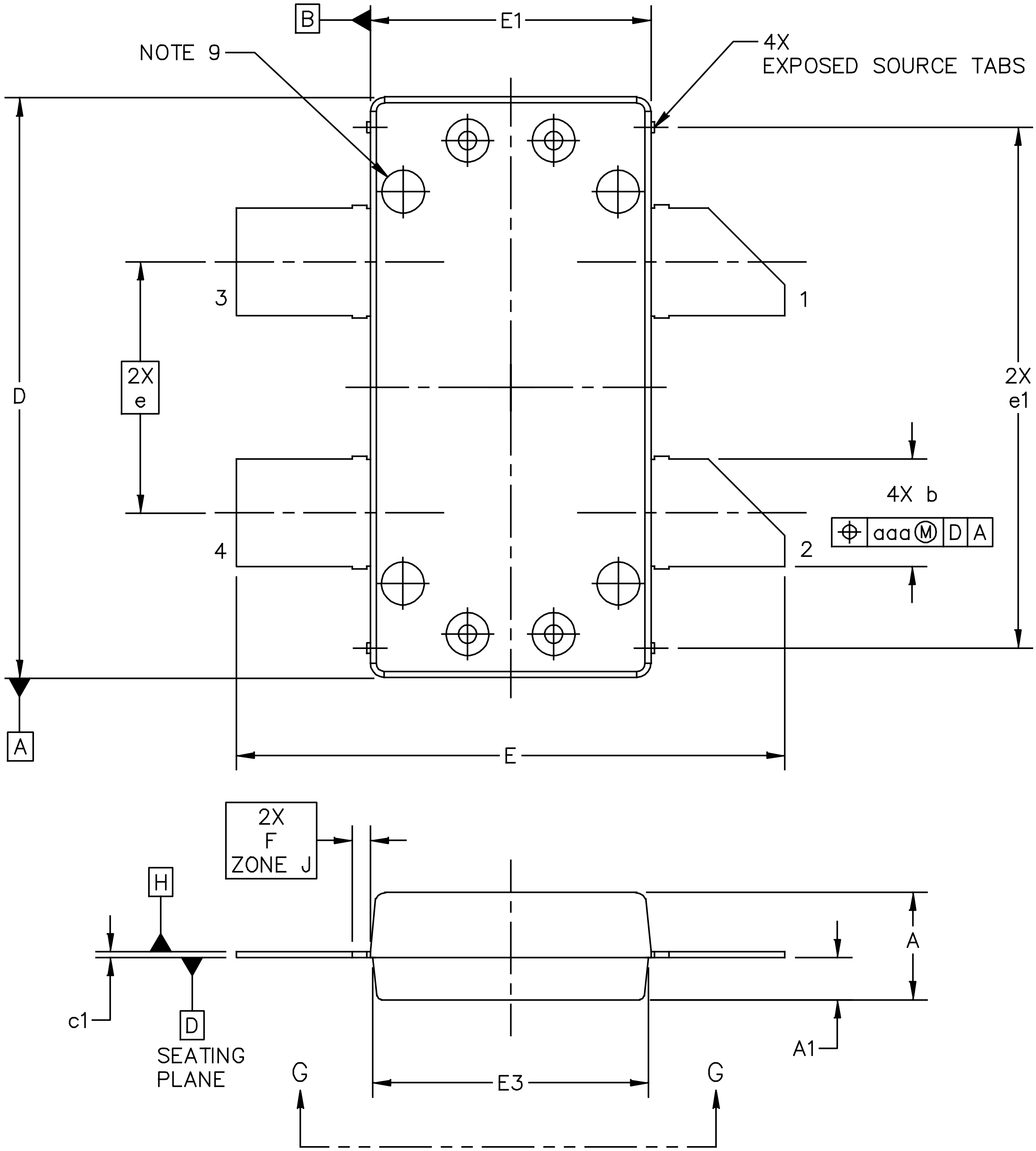
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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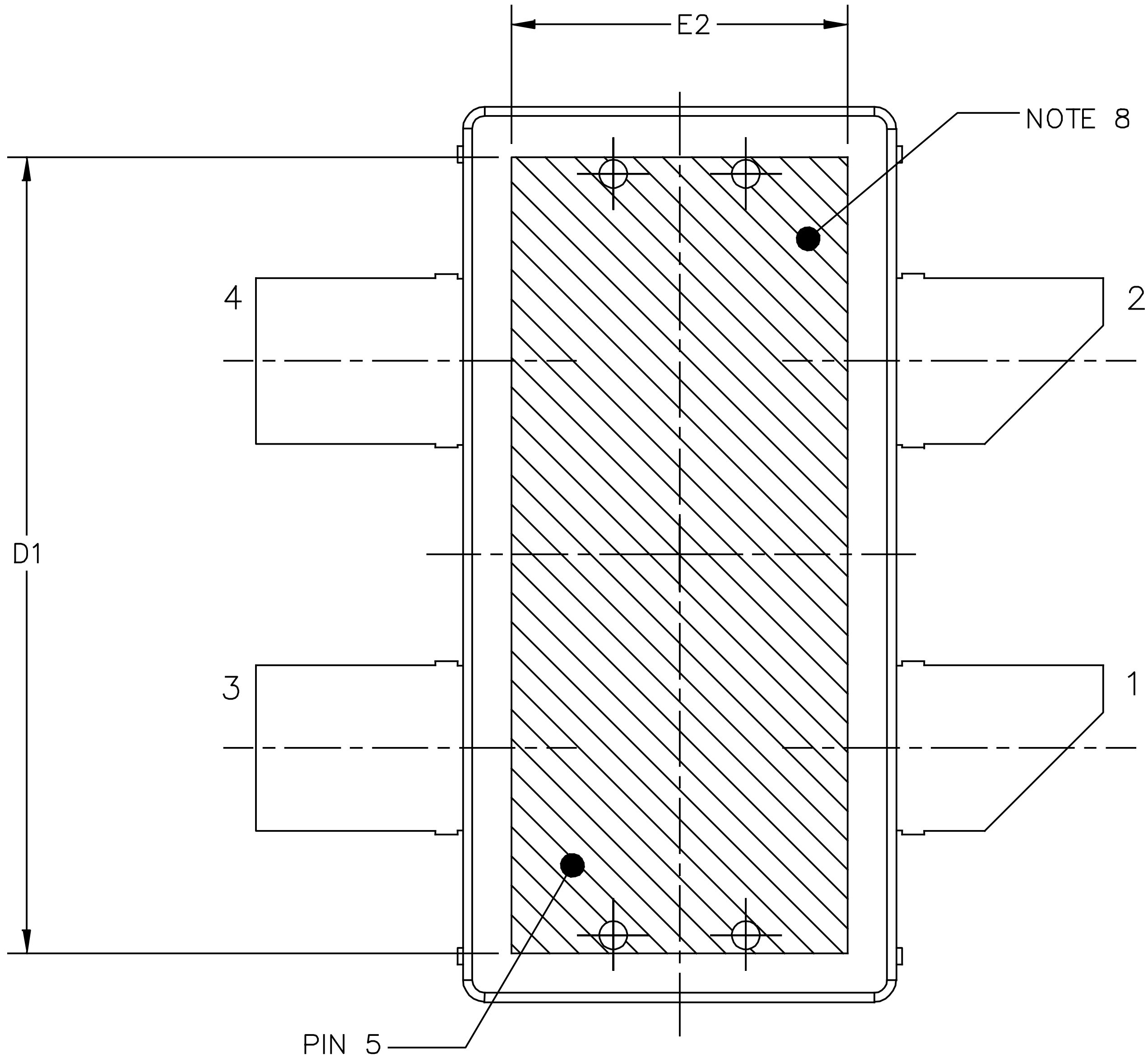
	SOT1818–4	16 MAR 2016



BOTTOM VIEW
VIEW G–G

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NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.
9. DIMPLED HOLE REPRESENTS INPUT SIDE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	0.148	.152	3.76	3.86	b	.147	.153	3.73	3.89
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
D	.808	.812	20.52	20.62	e	.350 BSC		8.89 BSC	
D1	.720	----	18.29	----	e1	.721	.729	18.31	18.52
E	.762	.770	19.36	19.56					
E1	.390	.394	9.91	10.01	aaa	.004		0.10	
E2	.306	----	7.77	----					
E3	.383	.387	9.72	9.83					
F	.025 BSC		0.635 BSC						

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Nov. 2016	• Initial release of data sheet
1	Mar. 2017	• On Characteristics table: Side A Carrier, Side B Peaking: updated $V_{GS(th)}$ Typ values and $V_{DS(on)}$ Min, Typ and Max values to reflect the actual performance of the device, p. 2 • Typical Performance table: added Gain Variation and Output Power Variation over Temperature typical values, p. 3 • 780 MHz: added load pull performance tables and contour graphs, pp. 7-12

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