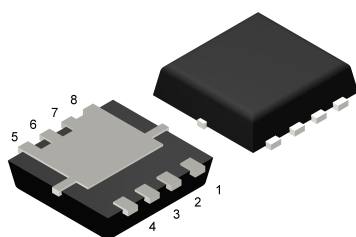
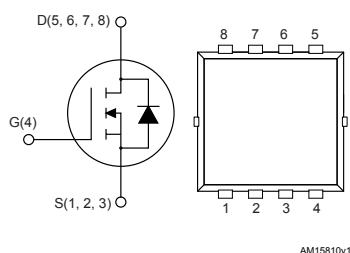


N-channel 100 V, 62 mΩ typ., 4.5 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 3.3x3.3 package



PowerFLAT™ 3.3x3.3



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STL4N10F7	100 V	70 mΩ	4.5 A

- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Maturity status link	
STL4N10F7	
Device summary	
Order code	STL4N10F7
Marking	4N1F7
Package	PowerFLAT™ 3.3x3.3
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	4.5	A
	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	3.2	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	18	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	2.9	W
$I_D^{(3)}$	Drain current (continuous) at $T_c = 25\text{ }^{\circ}\text{C}$	17	A
	Drain current (continuous) at $T_c = 100\text{ }^{\circ}\text{C}$	11	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	68	A
$P_{TOT}^{(3)}$	Total dissipation at $T_c = 25\text{ }^{\circ}\text{C}$	35.7	W
T_j	Operating junction temperature range	-55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		$^{\circ}\text{C}$

1. This value is rated according to $R_{thj-pcb}$.
2. Pulse width is limited by safe operating area.
3. This value is rated according to $R_{thj-case}$.

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	3.5	$^{\circ}\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	42.8	$^{\circ}\text{C/W}$

1. When mounted on an 1-inch² FR-4 board, 2oz Cu, $t < 10\text{ s}$

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	100			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.25\text{ A}$		62	70	m Ω

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	408	-	pF
C_{oss}	Output capacitance		-	112	-	pF
C_{rss}	Reverse transfer capacitance		-	10	-	pF
Q_g	Total gate charge	$V_{DD} = 50\text{ V}$, $I_D = 4.5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	7.8	-	nC
Q_{gs}	Gate-source charge		-	3	-	nC
Q_{gd}	Gate-drain charge		-	1.7	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}$, $I_D = 2.25\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	6.3	-	ns
t_r	Rise time		-	3	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	11	-	ns
t_f	Fall time		-	4	-	ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 2.25\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.1	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	$I_{SD} = 2.25\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 80\text{ V}$, $T_j = 150\text{ }^{\circ}\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	30		ns
Q_{rr}	Reverse recovery charge		-	24		nC
I_{RRM}	Reverse recovery current		-	1.6		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

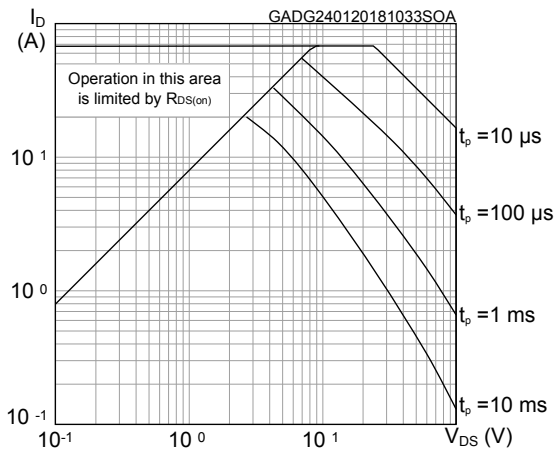
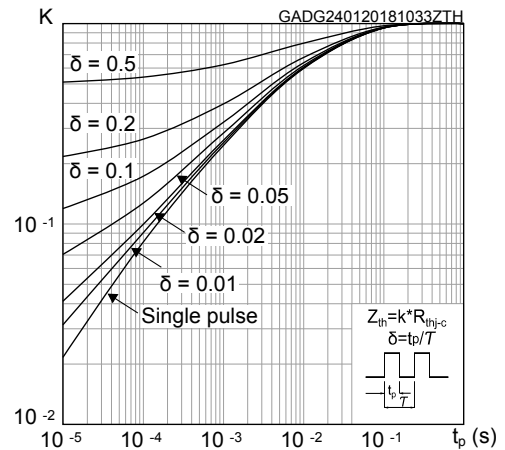
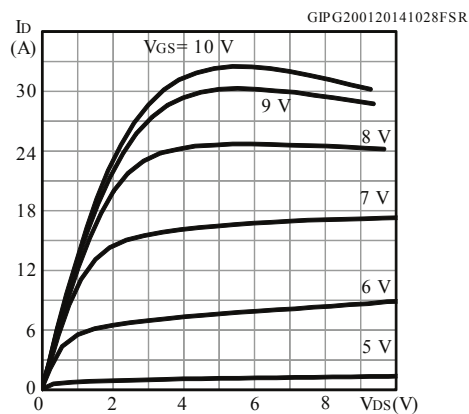
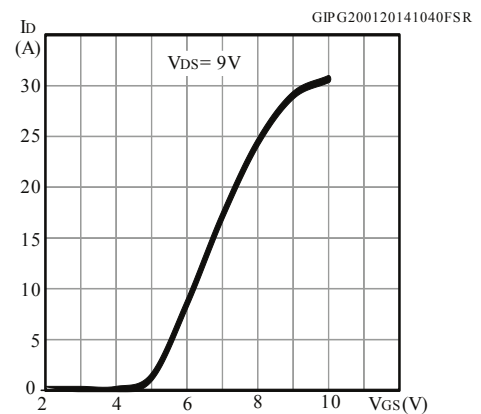
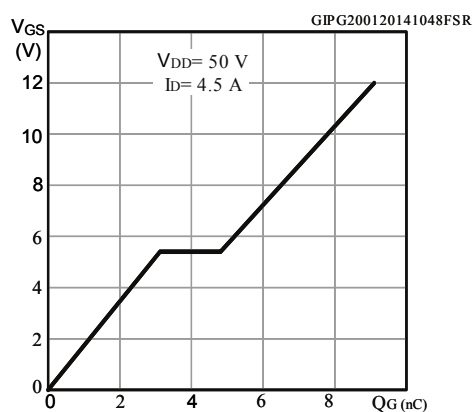
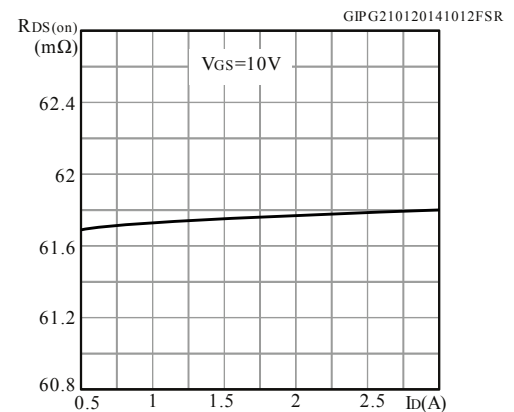
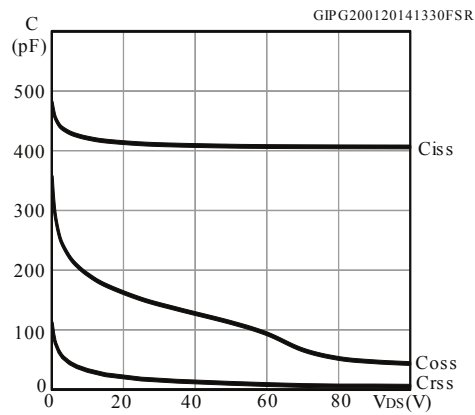
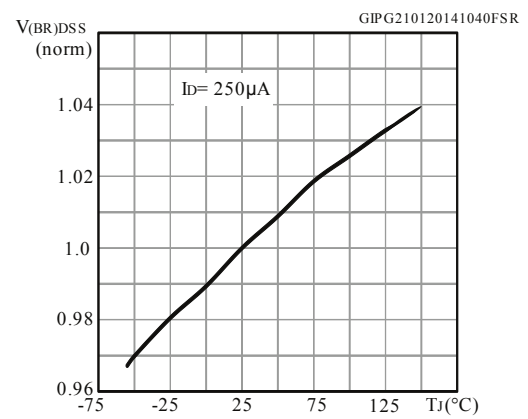
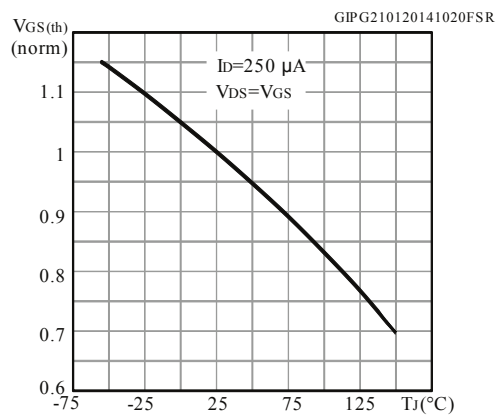
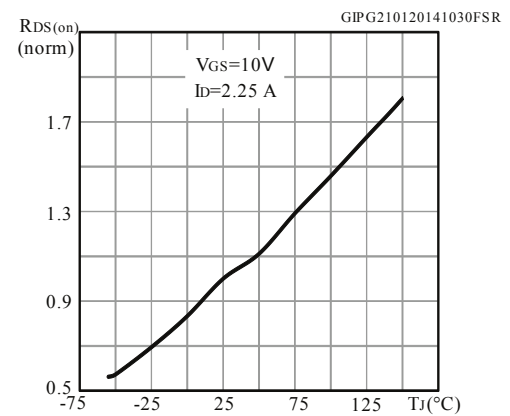
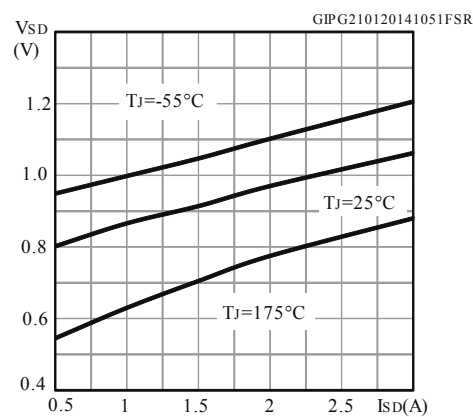
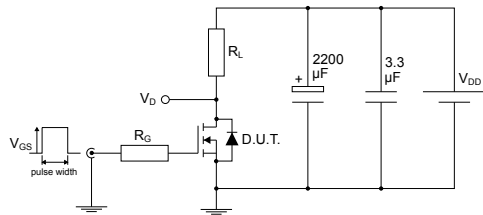
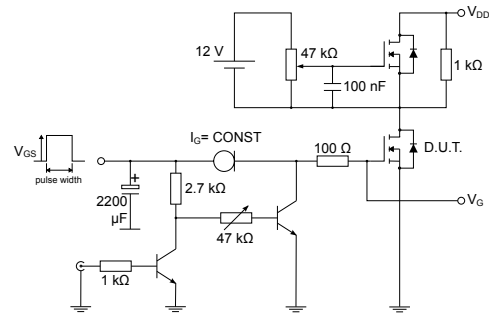
Figure 3. Safe operating area

Figure 4. Thermal impedance

Figure 5. Output characteristics

Figure 6. Transfer characteristics

Figure 7. Gate charge vs gate-source voltage

Figure 8. Static drain-source on-resistance


Figure 9. Capacitance variations

Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

Figure 11. Normalized gate threshold voltage vs temperature

Figure 12. Normalized on-resistance vs temperature

Figure 13. Source-drain diode forward characteristics


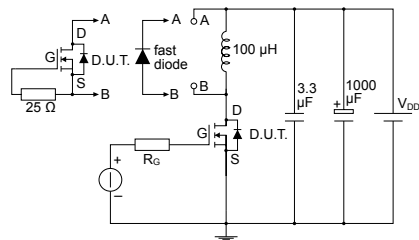
3 Test circuits

Figure 14. Test circuit for resistive load switching times


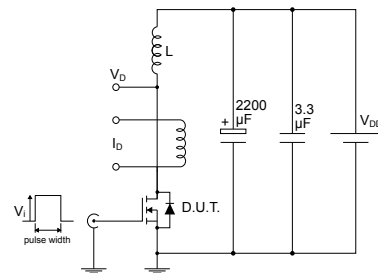
AM01468v1

Figure 15. Test circuit for gate charge behavior


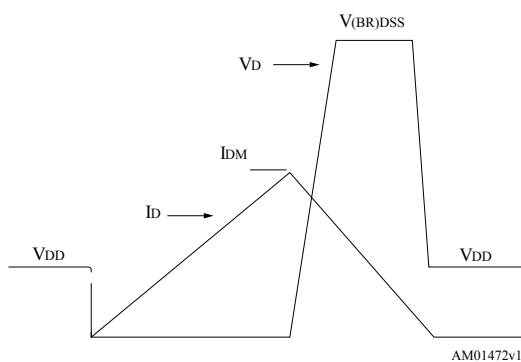
AM01469v1

Figure 16. Test circuit for inductive load switching and diode recovery times


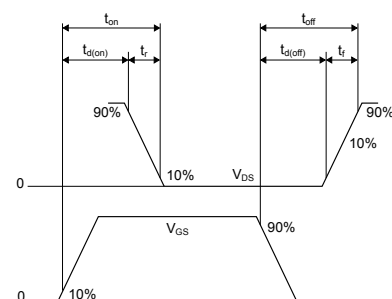
AM01470v1

Figure 17. Unclamped inductive load test circuit


AM01471v1

Figure 18. Unclamped inductive waveform


AM01472v1

Figure 19. Switching time waveform


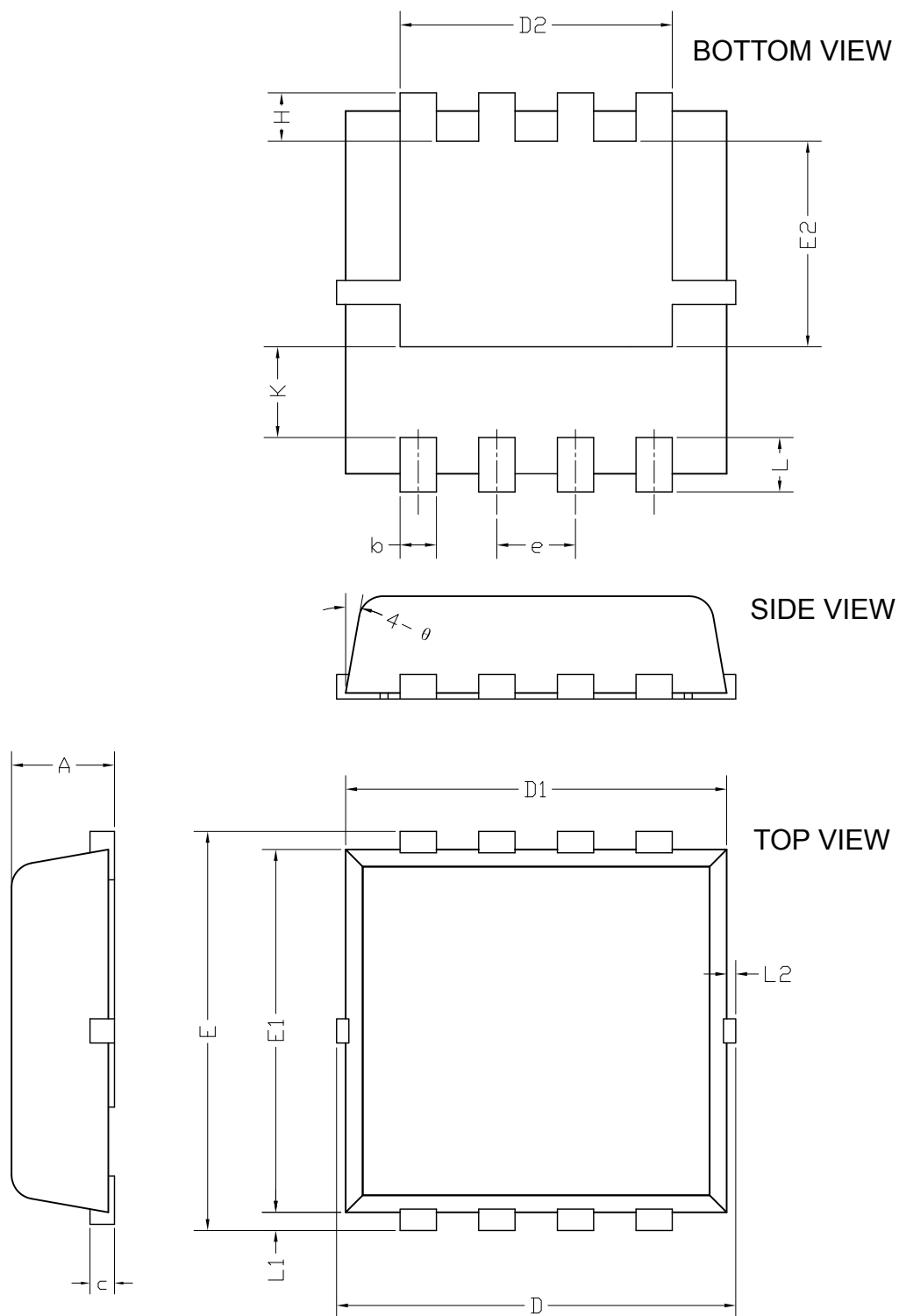
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 3.3x3.3 package information

Figure 20. PowerFLAT™ 3.3x3.3 package outline

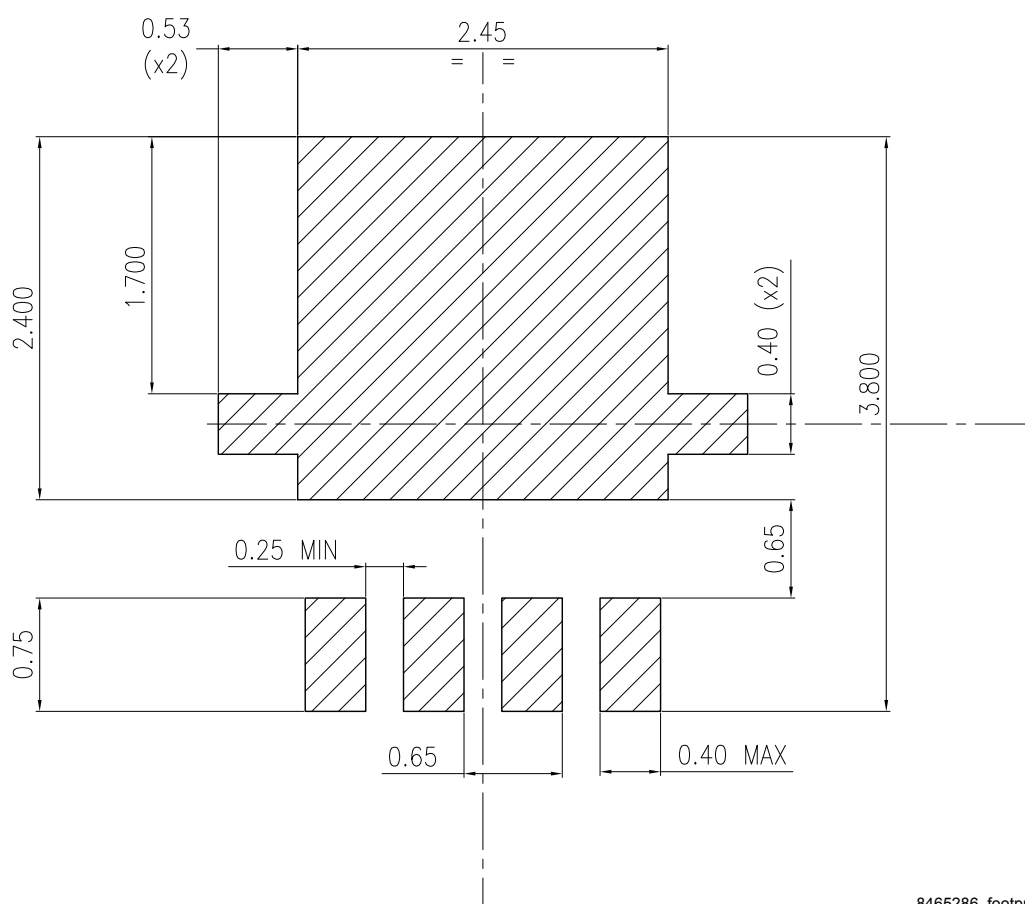


8465286_2

Table 7. PowerFLAT™ 3.3x3.3 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
θ	8°	10°	12°

Figure 21. PowerFLAT™ 3.3x3.3 recommended footprint (dimensions in mm)



8465286_footprint

Revision history

Table 8. Document revision history

Date	Revision	Changes
10-Jul-2013	1	First release.
21-Jan-2014	2	Inserted <i>Section 2.1: Electrical characteristics (curves)</i> . Document status promoted from preliminary to production data.
19-Feb-2014	3	Added: I_D (at $T_C = 25\text{ °C}$ and 125 °C), I_{DM} and P_{TOT} in <i>Table 2</i> Modified: <i>Figure 2</i> and <i>3</i> Minor text changes
10-Mar-2014	4	Modified: marking in <i>Table 1</i> Minor text changes
01-Feb-2018	5	Updated title, features and description on cover page. Removed maturity status indication from cover page. Updated Section 1 Electrical ratings . Updated Table 6. Source drain diode . Updated Section 2.1 Electrical characteristics (curves) . Minor text changes

Contents

1	Electrical ratings.....	2
2	Electrical characteristics.....	3
2.1	Electrical characteristics (curves).....	5
3	Test circuits	7
4	Package information.....	8
4.1	PowerFLAT™ 3.3x3.3 package information	8
	Revision history	12
	Contents	13
	Disclaimer.....	14

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9