Bulletin I25165 rev. C 03/03

International
IOR Rectifier

ST180S SERIES

PHASE CONTROL THYRISTORS

Stud Version

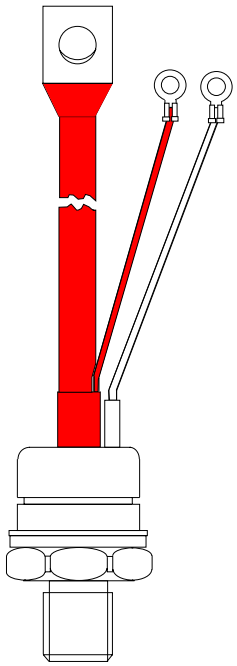
Features

- Center amplifying gate
- Hermetic metal case with ceramic insulator (Also available with glass-metal seal up to 1200V)
- International standard case TO-209AB (TO-93)
- Compression Bonded Encapsulation for heavy duty operations such as severe thermal cycling

200A

Typical Applications

- DC motor controls
- Controlled DC power supplies
- AC controllers



case style
TO-209AB (TO-93)

Major Ratings and Characteristics

Parameters		ST180S	Units
$I_{T(AV)}$		200	A
	@ T_C	85	°C
$I_{T(RMS)}$		314	A
I_{TSM}	@ 50Hz	5000	A
	@ 60Hz	5230	A
I^2t	@ 50Hz	125	KA^2s
	@ 60Hz	114	KA^2s
V_{DRM}/V_{RRM}		400 to 2000	V
t_q	typical	100	µs
T_J		- 40 to 125	°C

ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{DRM}/V_{RRM}, max. repetitive peak and off-state voltage V	V_{RSM}, maximum non-repetitive peak voltage V	I_{DRM}/I_{RRM} max. @ $T_J = T_J$ max mA
ST180S	04	400	500	30
	08	800	900	
	12	1200	1300	
	16	1600	1700	
	20	2000	2100	

On-state Conduction

	Parameter	ST180S	Units	Conditions		
$I_{T(AV)}$	Max. average on-state current	200	A	180° conduction, half sine wave		
	@ Case temperature	85	°C			
$I_{T(RMS)}$	Max. RMS on-state current	314	A	DC @ 76°C case temperature		
I_{TSM}	Max. peak, one-cycle non-repetitive surge current	5000	A	t = 10ms	No voltage reapplied	Sinusoidal half wave, Initial $T_J = T_J$ max.
		5230		t = 8.3ms		
		4200		t = 10ms	100% V_{RRM} reapplied	
		4400		t = 8.3ms		
I^2t	Maximum I^2t for fusing	125	KA^2s	t = 10ms	No voltage reapplied	
		114		t = 8.3ms		
		88		t = 10ms	100% V_{RRM} reapplied	
		81		t = 8.3ms		
$I^2\sqrt{t}$	Maximum $I^2\sqrt{t}$ for fusing	1250	$KA^2\sqrt{s}$	t = 0.1 to 10ms, no voltage reapplied		
$V_{T(TO)1}$	Low level value of threshold voltage	1.08	V	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ max.		
$V_{T(TO)2}$	High level value of threshold voltage	1.14		(I > π x $I_{T(AV)}$), $T_J = T_J$ max.		
r_{t1}	Low level value of on-state slope resistance	1.18	mΩ	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ max.		
r_{t2}	High level value of on-state slope resistance	1.14		(I > π x $I_{T(AV)}$), $T_J = T_J$ max.		
V_{TM}	Max. on-state voltage	1.75	V	I_{pk}= 570A, T_J = 125°C, t_p = 10ms sine pulse		
I_H	Maximum holding current	600	mA	$T_J = T_J$ max, anode supply 12V resistive load		
I_L	Max. (typical) latching current	1000 (300)				

Switching

	Parameter	ST180S	Units	Conditions
di/dt	Max. non-repetitive rate of rise of turned-on current	1000	A/µs	Gate drive 20V, 20Ω, $t_r \leq 1\mu s$ $T_J = T_J$ max, anode voltage ≤ 80% V_{DRM}
t_d	Typical delay time	1.0	µs	Gate current 1A, di_g/dt = 1A/µs V_d = 0.67% V_{DRM}, T_J = 25°C
t_q	Typical turn-off time	100		I_{TM} = 300A, $T_J = T_J$ max, di/dt = 20A/µs, V_R = 50V dv/dt = 20V/µs, Gate 0V 100Ω, t_p = 500µs

Blocking

	Parameter	ST180S	Units	Conditions
dv/dt	Maximum critical rate of rise of off-state voltage	500	V/µs	$T_J = T_J$ max linear to 80% rated V_{DRM}
I_{DRM} I_{RRM}	Max. peak reverse and off-state leakage current	30	mA	$T_J = T_J$ max, rated V_{DRM}/V_{RRM} applied

Triggering

	Parameter	ST180S		Units	Conditions	
P_{GM}	Maximum peak gate power	10		W	$T_J = T_J$ max, $t_p \leq 5$ms	
$P_{G(AV)}$	Maximum average gate power	2.0			$T_J = T_J$ max, f = 50Hz, d% = 50	
I_{GM}	Max. peak positive gate current	3.0		A	$T_J = T_J$ max, $t_p \leq 5$ms	
$+V_{GM}$	Maximum peak positive gate voltage	20		V	$T_J = T_J$ max, $t_p \leq 5$ms	
$-V_{GM}$	Maximum peak negative gate voltage	5.0				
		TYP.	MAX.			
I_{GT}	DC gate current required to trigger	180	-	mA	T_J = - 40°C	Max. required gate trigger/ current/ voltage are the lowest value which will trigger all units 12V anode-to-cathode applied
		90	150		T_J = 25°C	
		40	-		T_J = 125°C	
V_{GT}	DC gate voltage required to trigger	2.9	-	V	T_J = - 40°C	
		1.8	3.0		T_J = 25°C	
		1.2	-		T_J = 125°C	
I_{GD}	DC gate current not to trigger	10		mA	$T_J = T_J$ max	Max. gate current/ voltage not to trigger is the max. value which will not trigger any unit with rated V_{DRM} anode-to-cathode applied
V_{GD}	DC gate voltage not to trigger	0.25		V		

Thermal and Mechanical Specification

	Parameter	ST180S	Units	Conditions
T_J	Max. operating temperature range	-40 to 125	°C	
T_{stg}	Max. storage temperature range	-40 to 150		
R_{thJC}	Max. thermal resistance, junction to case	0.105	K/W	DC operation
R_{thCS}	Max. thermal resistance, case to heatsink	0.04		Mounting surface, smooth, flat and greased
T	Mounting torque, ± 10%	31 (275)	Nm (lbf-in)	Non lubricated threads
		24.5 (210)		Lubricated threads
wt	Approximate weight	280	g	
	Case style	TO - 209AB (TO-93)		See Outline Table

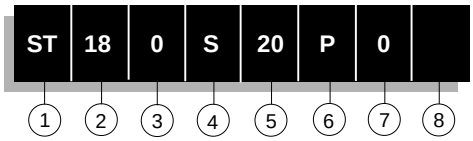
ΔR_{thJC} Conduction

(The following table shows the increment of thermal resistence R_{thJC} when devices operate at different conduction angles than DC)

Conduction angle	Sinusoidal conduction	Rectangular conduction	Units	Conditions
180°	0.015	0.012	K/W	$T_J = T_J$ max.
120°	0.019	0.020		
90°	0.025	0.027		
60°	0.036	0.037		
30°	0.060	0.060		

Ordering Information Table

Device Code



1 - Thyristor

2 - Essential part number

3 - 0 = Converter grade

4 - S = Compression bonding Stud

5 - Voltage code: Code x 100 = V_{RRM} (See Voltage Rating Table)

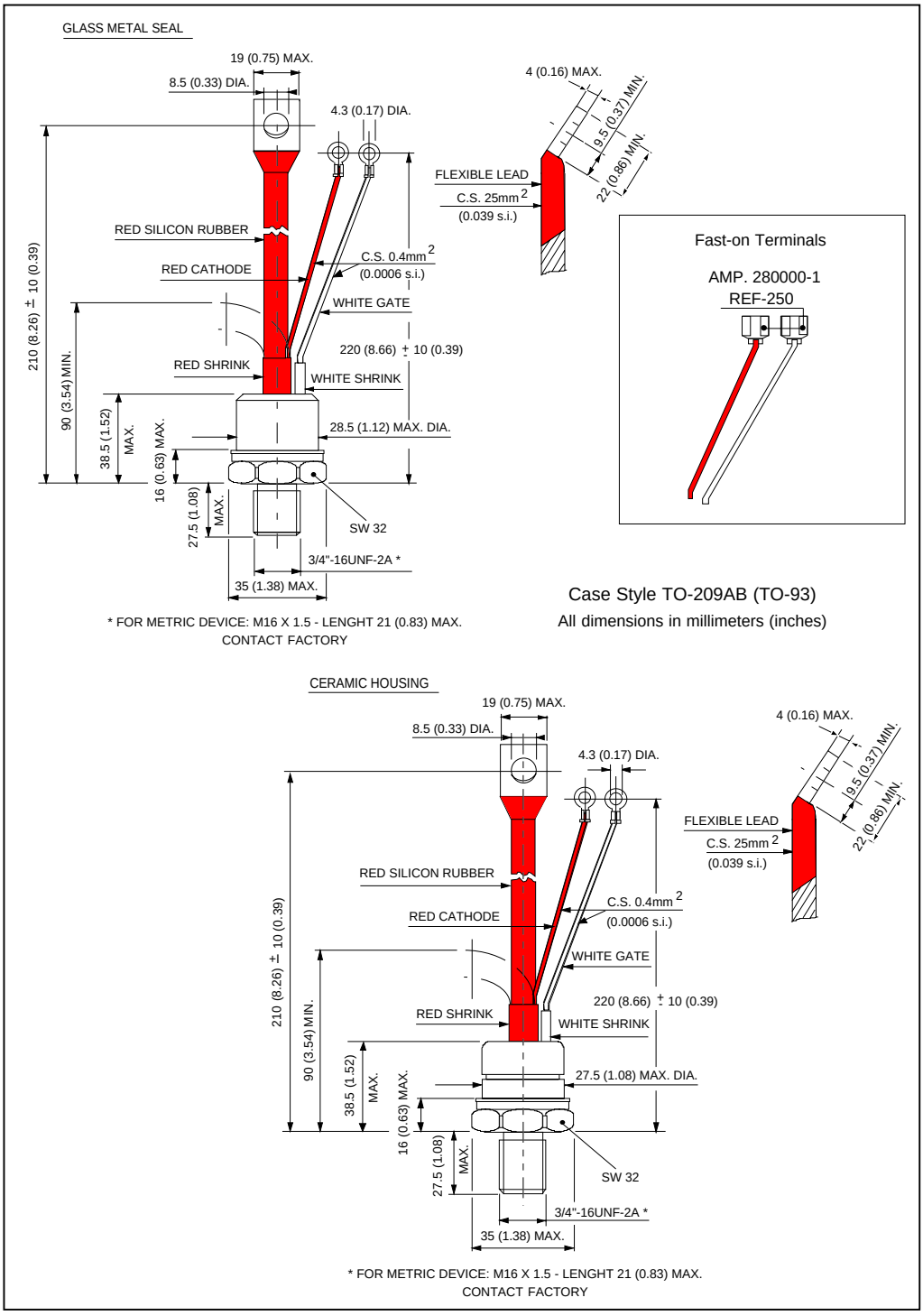
6 - P = Stud base 3/4"-16UNF2A threads

7 - 0 = Eyelet terminals (Gate and Auxiliary Cathode Leads)
1 = Fast - on terminals (Gate and Auxiliary Cathode Leads)

8 - V = Glass-metal seal (only up to 1200V)
None = Ceramic housing (over 1200V)

NOTE: For Metric device M16 x 1.5 Contact factory

Outline Table



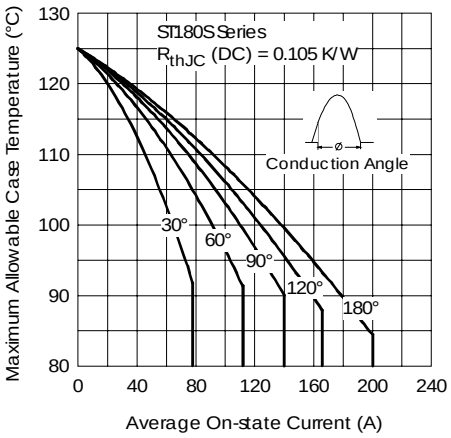


Fig. 1 - Current Ratings Characteristics

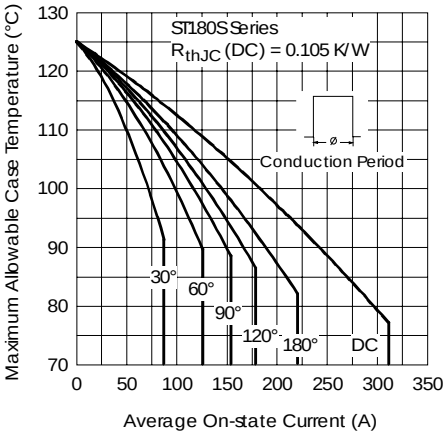


Fig. 2 - Current Ratings Characteristics

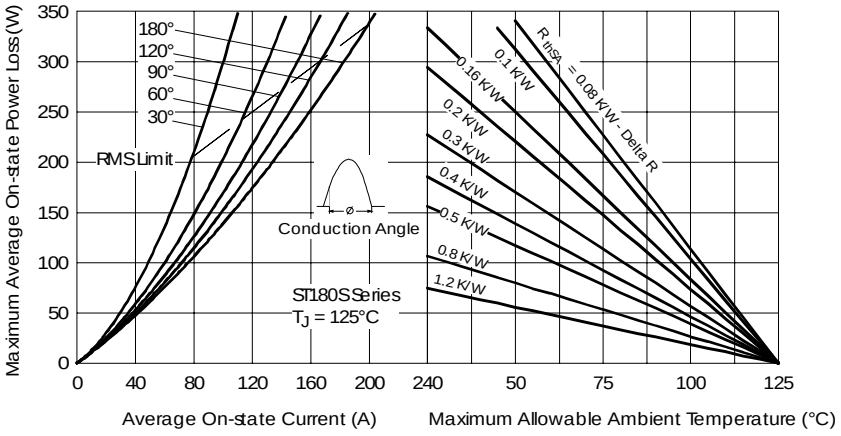


Fig. 3 - On-state Power Loss Characteristics

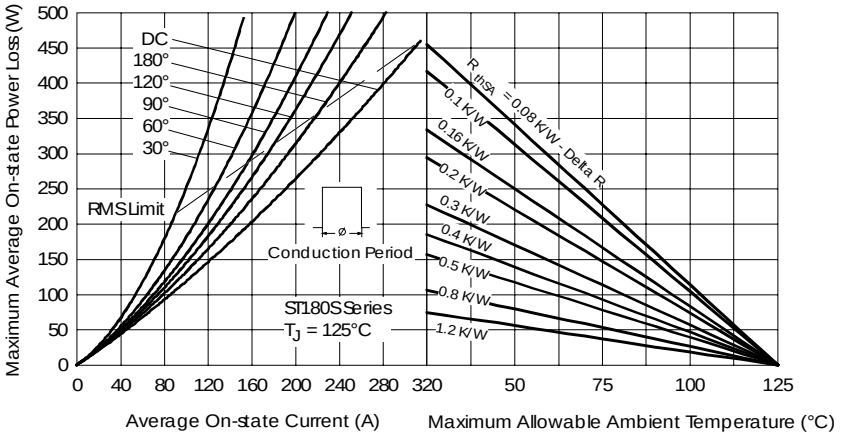


Fig. 4 - On-state Power Loss Characteristics

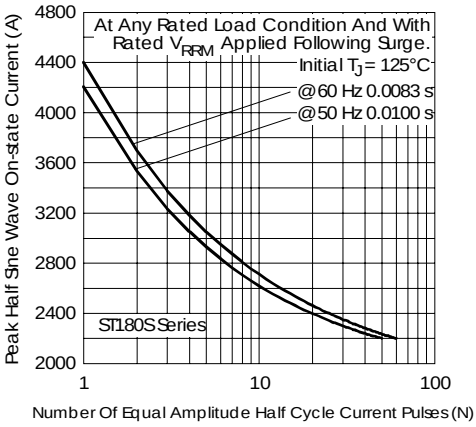


Fig. 5 - Maximum Non-Repetitive Surge Current

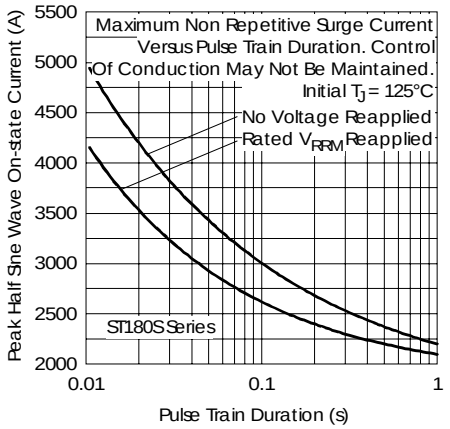


Fig. 6 - Maximum Non-Repetitive Surge Current

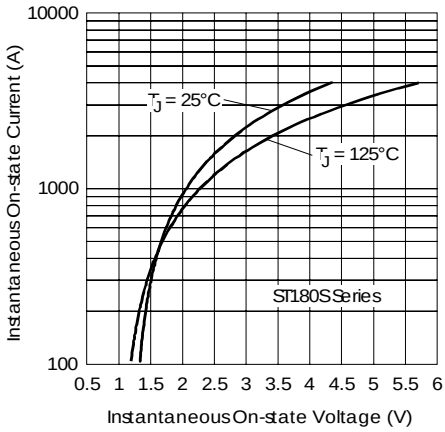


Fig. 7 - On-state Voltage Drop Characteristics

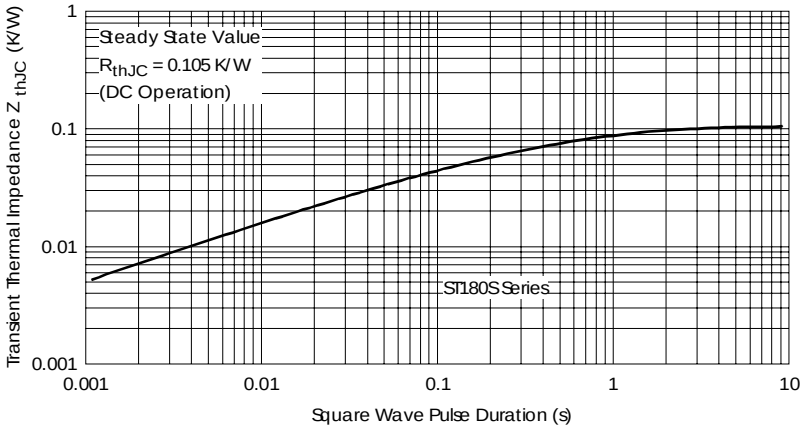


Fig. 8 - Thermal Impedance Z_{thJC} Characteristic

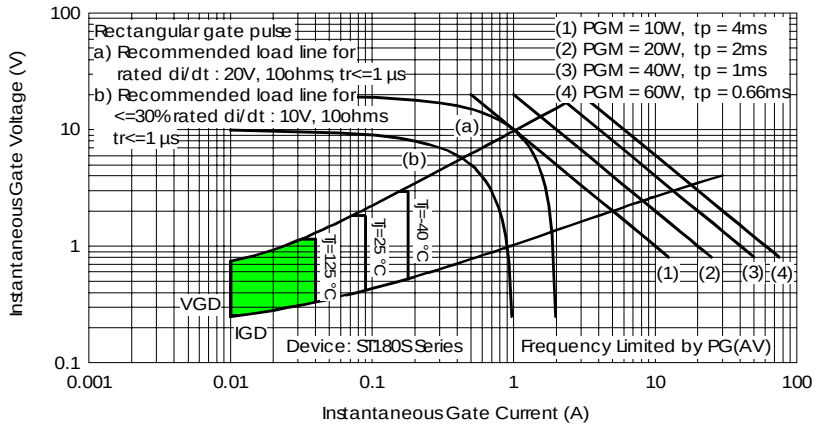


Fig. 9 - Gate Characteristics

Data and specifications subject to change without notice.
This product has been designed and qualified for Industrial Level.
Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7309
Visit us at www.irf.com for sales contact information. 03/03

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Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9