

## Dual FET Bus Switch 2.5-V/3.3-V Low-Voltage High-Bandwidth Bus Switch

 Check for Samples: [SN74CB3Q3306A-EP](#)

### FEATURES

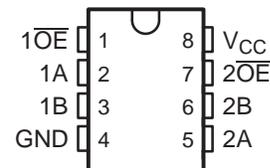
- High-Bandwidth Data Path (up to 500 MHz<sup>(1)</sup>)
- 5-V-Tolerant I/Os With Device Powered Up or Powered Down
- Low and Flat ON-State Resistance ( $r_{on}$ ) Characteristics Over Operating Range ( $r_{on} = 4 \Omega$  Typ)
- Rail-to-Rail Switching on Data I/O Ports
  - 0- to 5-V Switching With 3.3-V  $V_{CC}$
  - 0- to 3.3-V Switching With 2.5-V  $V_{CC}$
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{io(OFF)} = 3.5$  pF Typ)
- Fast Switching Frequency ( $f_{OE} = 20$  MHz Max)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 0.25$  mA Typ)
- $V_{CC}$  Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation

(1) For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number [SCDA008](#).

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface, Bus Isolation, Low-Distortion Signal Gating

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Military ( $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ) Temperature Range
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

 PW PACKAGE  
(TOP VIEW)


### ORDERING INFORMATION

$T_J$	PACKAGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	TSSOP – PW	Tube	U306AM	V62/14606-01XE-T
		Tape and reel		V62/14606-01XE

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION

The SN74CB3Q3306A is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance ( $r_{on}$ ). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3306A provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3306A is organized as two 1-bit switches with separate output-enable ( $\overline{1OE}$ ,  $\overline{2OE}$ ) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When  $\overline{OE}$  is low, the associated 1-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**Table 1. FUNCTION TABLE  
(EACH BUS SWITCH)**

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

### LOGIC DIAGRAM (POSITIVE LOGIC)

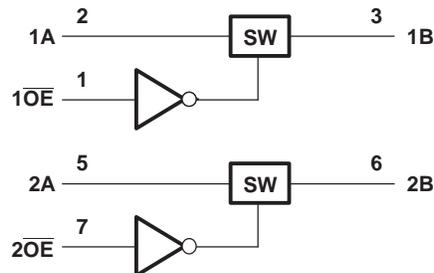
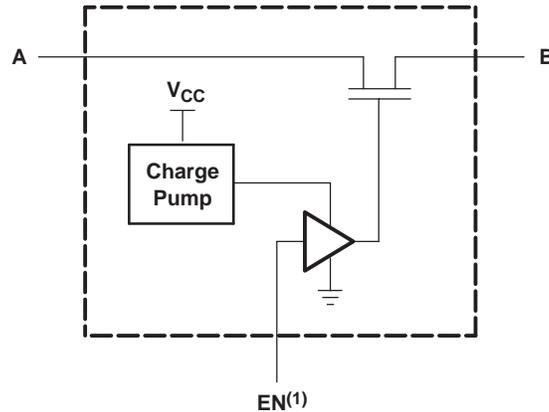


Figure 1. SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_{IN}$	Control input voltage range <sup>(2) (3)</sup>	-0.5	7	V
$V_{I/O}$	Switch I/O voltage range <sup>(2) (3) (4)</sup>	-0.5	7	V
$I_{IK}$	Control input clamp current	$V_{IN} < 0$	-50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$	-50	mA
$I_{I/O}$	ON-state switch current <sup>(5)</sup>		±64	mA
	Continuous current through each $V_{CC}$ or GND		±100	mA
$T_J$	Maximum junction temperature		150	°C
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4)  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
- (5)  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .

**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)</sup>		SN74CB3Q3306A-EP	UNITS
		PW	
		8 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	190.6	°C/W
$\theta_{JcTop}$	Junction-to-case (top) thermal resistance <sup>(3)</sup>	74	
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(4)</sup>	119.4	
$\psi_{JT}$	Junction-to-top characterization parameter <sup>(5)</sup>	12	
$\psi_{JB}$	Junction-to-board characterization parameter <sup>(6)</sup>	117.7	
$\theta_{JcBot}$	Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2.3	3.6	V
$V_{IH}$	High-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	5.5	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2	5.5	
$V_{IL}$	Low-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0	0.8	
$V_{IO}$	Data input/output voltage		0	5.5	V
$T_J$	Operating junction temperature		-55	125	°C

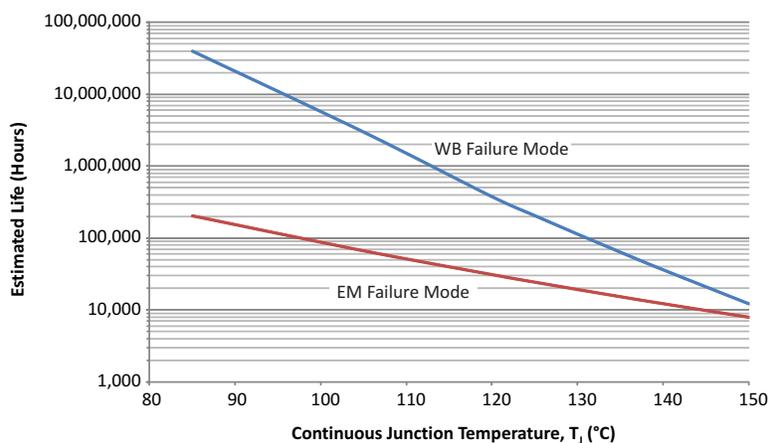
- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP <sup>(2)</sup>	MAX	UNIT	
$V_{IK}$		$V_{CC} = 3.6\text{ V}$ ,	$I_I = -18\text{ mA}$				-1.8	V	
$I_{IN}$	Control inputs	$V_{CC} = 3.6\text{ V}$ ,	$V_{IN} = 0\text{ to }5.5\text{ V}$				$\pm 1$	$\mu\text{A}$	
$I_{OZ}$ <sup>(3)</sup>		$V_{CC} = 3.6\text{ V}$ ,	$V_O = 0\text{ to }5.5\text{ V}$ , $V_I = 0$ ,	Switch OFF, $V_{IN} = V_{CC}$			$\pm 1$	$\mu\text{A}$	
$I_{off}$		$V_{CC} = 0$ ,	$V_O = 0\text{ to }5.5\text{ V}$ , $V_I = 0$				1	$\mu\text{A}$	
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ ,	$I_{IO} = 0$ , Switch ON or OFF,	$V_{IN} = V_{CC}$ or GND		0.25	0.7	mA	
$\Delta I_{CC}$ <sup>(4)</sup>	Control inputs	$V_{CC} = 3.6\text{ V}$ ,	One input at 3 V,	Other inputs at $V_{CC}$ or GND	$T_J = -55^\circ\text{C to }85^\circ\text{C}$		25	$\mu\text{A}$	
					$T_J = 125^\circ\text{C}$		36		
$I_{CCD}$ <sup>(5)</sup>		$V_{CC} = 3.6\text{ V}$ ,	A and B ports open, Control input switching at 50% duty cycle			0.03		mA/ MHz	
$C_{in}$		$V_{CC} = 3.3\text{ V}$ ,	$V_{IN} = 5.5\text{ V}, 3.3\text{ V}, \text{ or }0$			2.5		pF	
$C_{io(OFF)}$		$V_{CC} = 3.3\text{ V}$ ,	Switch OFF, $V_{IN} = V_{CC}$ ,	$V_{IO} = 5.5\text{ V}, 3.3\text{ V}, \text{ or }0$		3.5		pF	
$C_{io(ON)}$		$V_{CC} = 3.3\text{ V}$ ,	Switch ON, $V_{IN} = \text{GND}$ ,	$V_{IO} = 5.5\text{ V}, 3.3\text{ V}, \text{ or }0$		8		pF	
$r_{on}$ <sup>(6)</sup>		$V_{CC} = 2.3\text{ V}$ , TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$ ,	$I_O = 30\text{ mA}$	$T_J = -55^\circ\text{C to }85^\circ\text{C}$		4	8	$\Omega$
					$T_J = 125^\circ\text{C}$			10	
			$V_I = 1.7\text{ V}$ ,	$I_O = -15\text{ mA}$	$T_J = -55^\circ\text{C to }85^\circ\text{C}$		5	9	
		$T_J = 125^\circ\text{C}$				58			
		$V_{CC} = 3\text{ V}$	$V_I = 0$ ,	$I_O = 30\text{ mA}$	$T_J = -55^\circ\text{C to }85^\circ\text{C}$		4	6	
					$T_J = 125^\circ\text{C}$			8	
$V_I = 2.4\text{ V}$ ,	$I_O = -15\text{ mA}$		$T_J = -55^\circ\text{C to }85^\circ\text{C}$		5	8			
		$T_J = 125^\circ\text{C}$			66				

- (1)  $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.
- (2) All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .
- (3) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.
- (4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.
- (5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 4).
- (6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



- (1) See datasheet for absolute maximum and minimum recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- (3) Enhanced plastic product disclaimer applies.

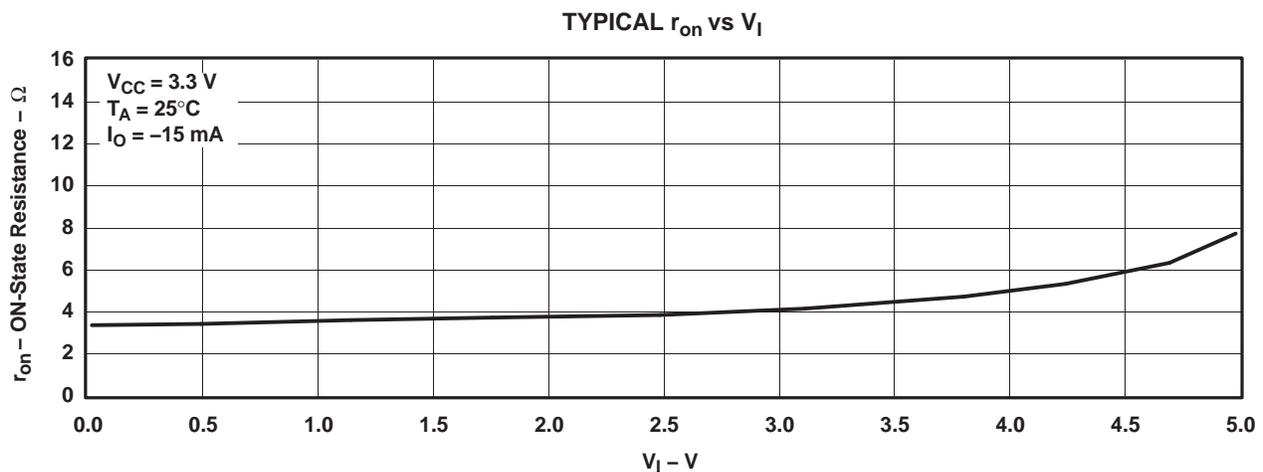
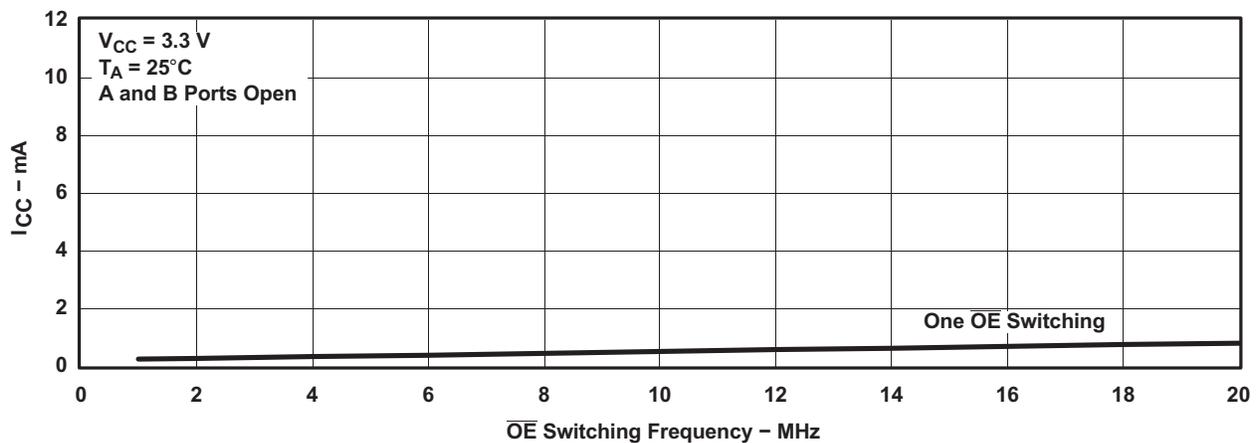
**Figure 2. SN74CB3Q3306A-EP Operating Life Derating Chart**

## SWITCHING CHARACTERISTICS

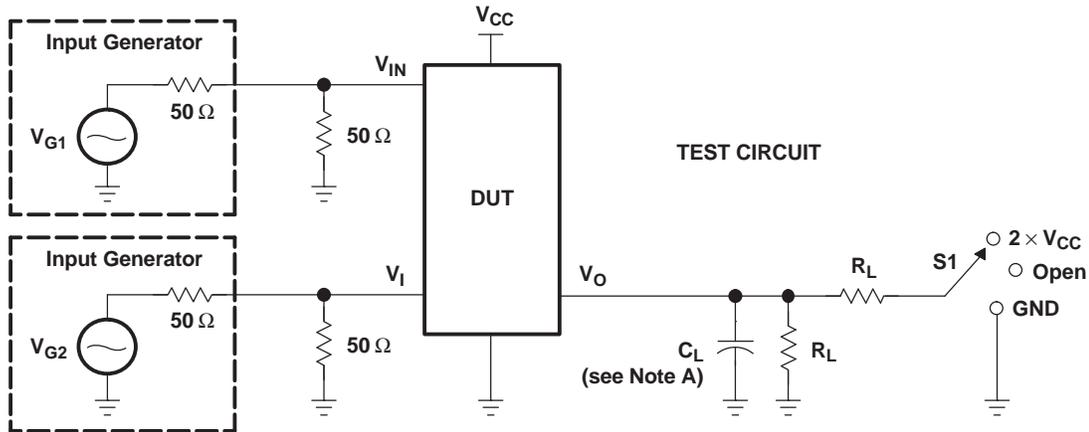
 over recommended operating junction temperature range (unless otherwise noted) (see [Figure 5](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}^{(1)}$	$\overline{OE}$	A or B		10		20	MHz
$t_{pd}^{(2)}$	$T_J = -55^\circ\text{ to }85^\circ\text{C}$	A or B		0.2		0.3	ns
	$T_J = 125^\circ\text{C}$			1.2		2.3	
$t_{en}$	$\overline{OE}$	A or B	1.5	12	1.5	10	ns
$t_{dis}$	$\overline{OE}$	A or B	1	14	1	9	ns

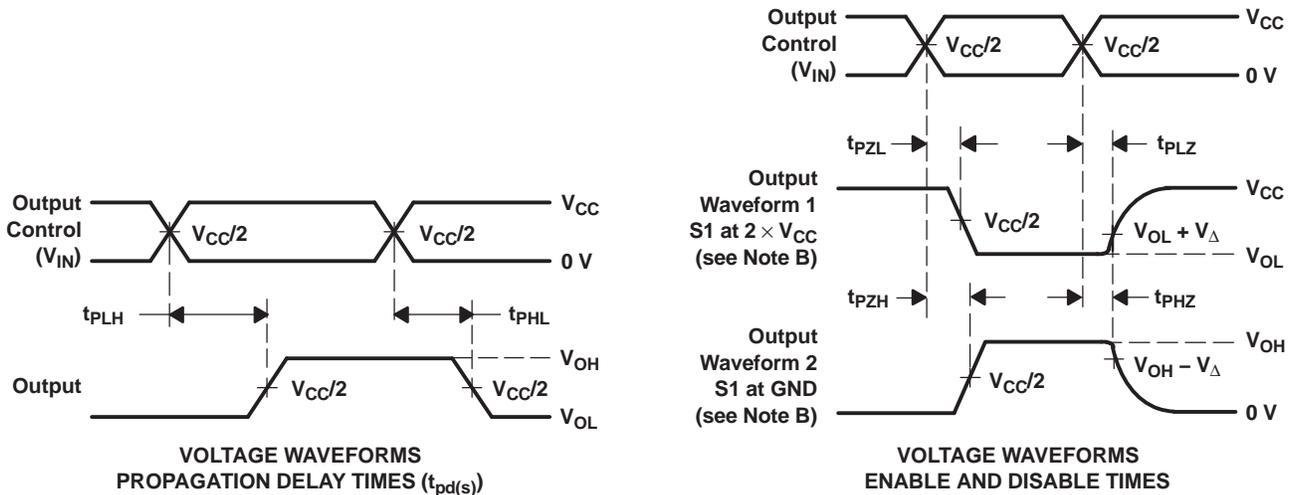
- (1) Maximum switching frequency for control input ( $V_O > V_{CC}$ ,  $V_I = 5\text{ V}$ ,  $R_L \geq 1\text{ M}\Omega$ ,  $C_L = 0$ )  
 (2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).


**Figure 3. Typical  $r_{on}$  vs  $V_I$** 

**Figure 4. Typical  $I_{CC}$  vs  $\overline{OE}$  Switching Frequency**

PARAMETER MEASUREMENT INFORMATION



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>pd(s)</sub>	2.5 V ± 0.2 V	Open	500 Ω	V <sub>CC</sub> or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V <sub>CC</sub> or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	2.5 V ± 0.2 V	2 × V <sub>CC</sub>	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V <sub>CC</sub>	500 Ω	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	2.5 V ± 0.2 V	GND	500 Ω	V <sub>CC</sub>	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V <sub>CC</sub>	50 pF	0.3 V



- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd(s)</sub>. The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - H. All parameters and waveforms are not applicable to all devices.

Figure 5. Test Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CCB3Q3306AMPWEP	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	U306AM	<a href="#">Samples</a>
CCB3Q3306AMPWREP	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	U306AM	<a href="#">Samples</a>
V62/14606-01XE	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	U306AM	<a href="#">Samples</a>
V62/14606-01XE-T	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	U306AM	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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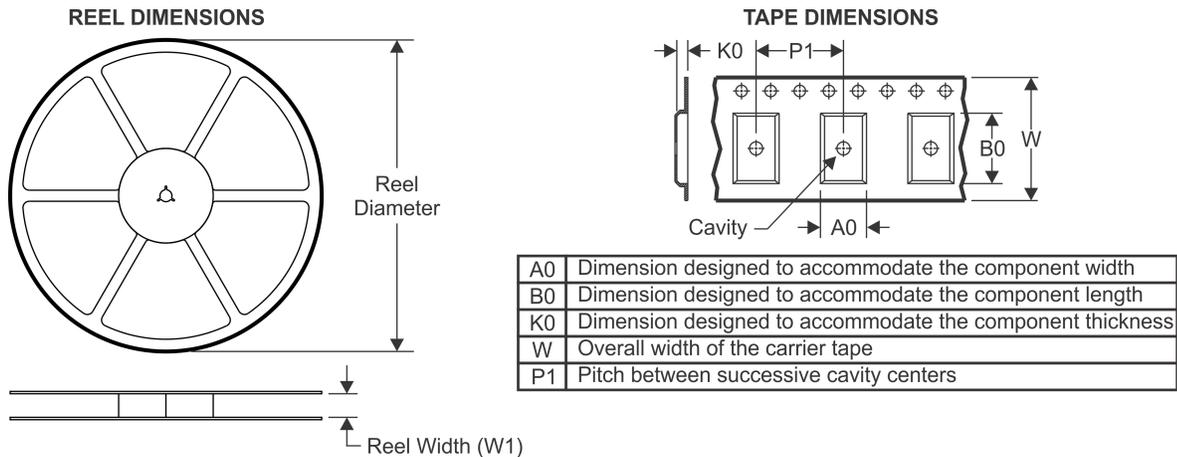
**OTHER QUALIFIED VERSIONS OF SN74CB3Q3306A-EP :**

- Catalog: [SN74CB3Q3306A](#)

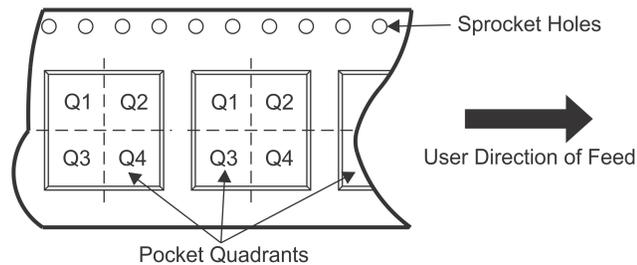
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



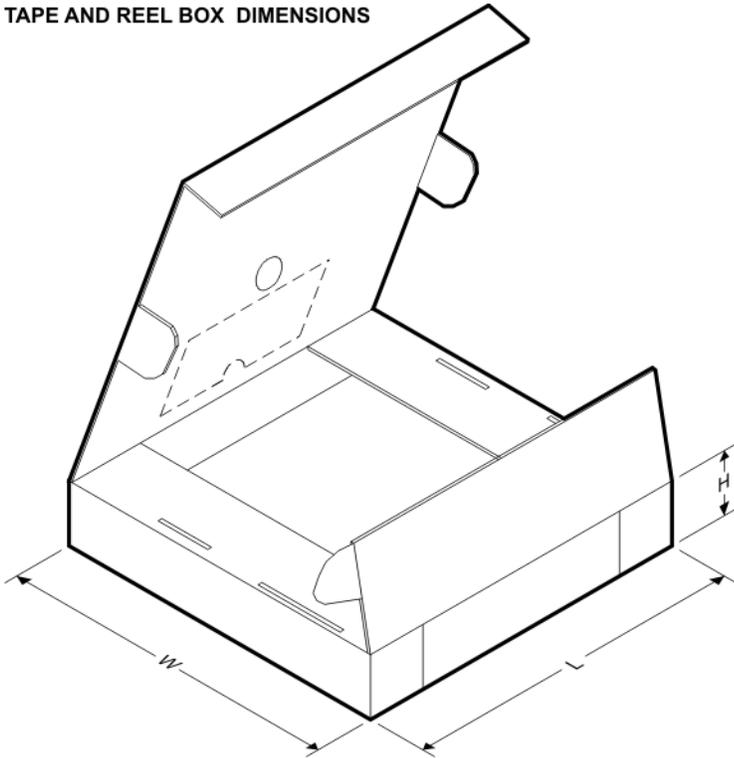
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CCB3Q3306AMPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CCB3Q3306AMPWREP	TSSOP	PW	8	2000	367.0	367.0	35.0

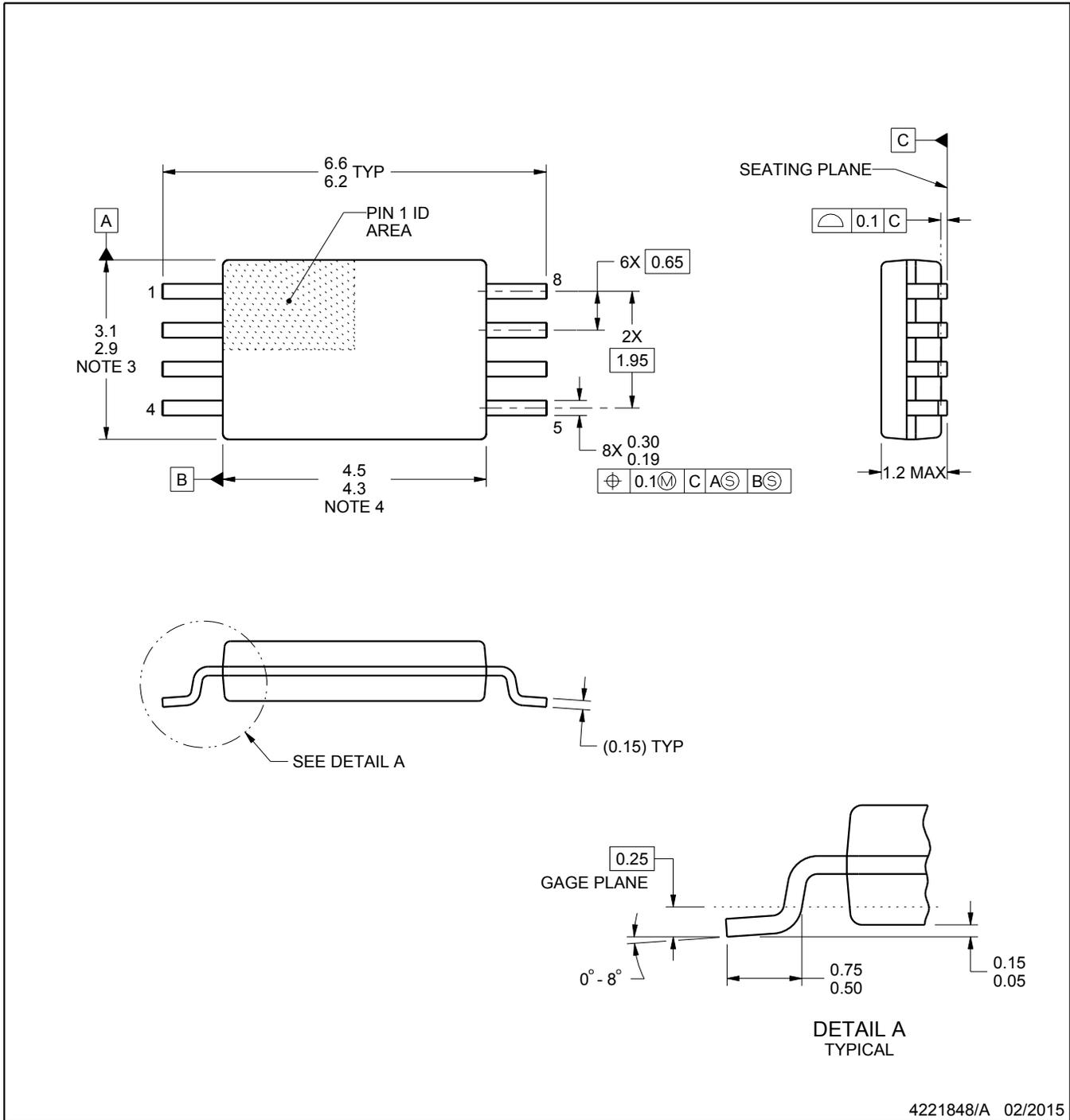
PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

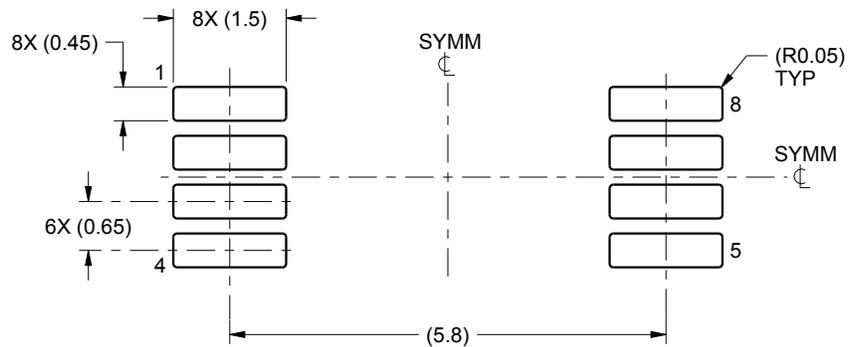
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

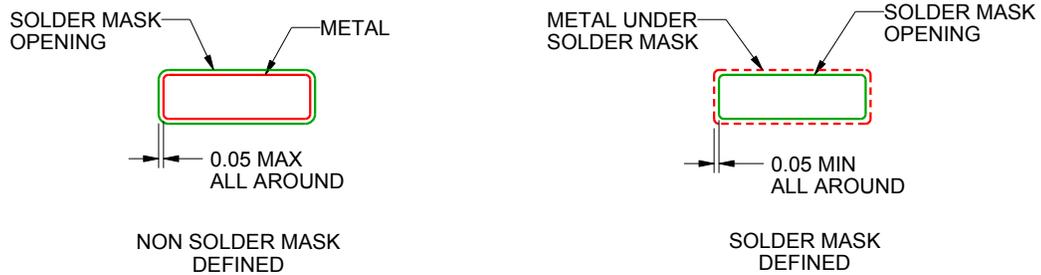
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

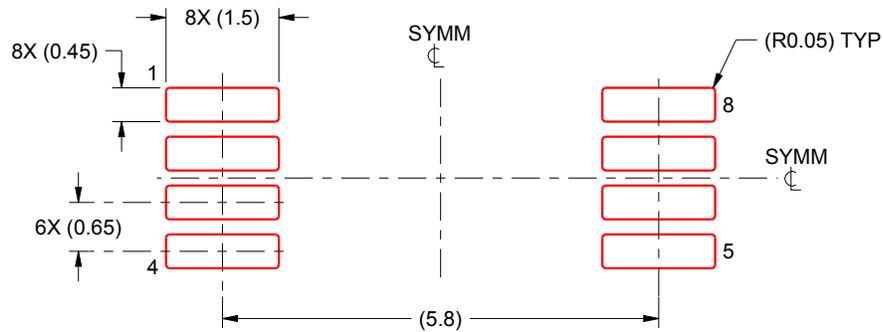
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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