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June 2009

## FDMA6023PZT

# Dual P-Channel PowerTrench® MOSFET -20 V, -3.6 A, 60 m $\Omega$

#### **Features**

- Max  $r_{DS(on)} = 60 \text{ m}\Omega$  at  $V_{GS} = -4.5 \text{ V}$ ,  $I_D = -3.6 \text{ A}$
- Max  $r_{DS(on)}$  = 80 m $\Omega$  at  $V_{GS}$  = -2.5 V,  $I_D$  = -3.0 A
- Max  $r_{DS(on)}$  = 110 m $\Omega$  at  $V_{GS}$  = -1.8 V,  $I_D$  = -2.0 A
- Max  $r_{DS(on)} = 170 \text{ m}\Omega$  at  $V_{GS} = -1.5 \text{ V}$ ,  $I_D = -1.0 \text{ A}$
- Low Profile-0.55 mm maximum in the new package MicroFET 2x2 mm Thin
- HBM ESD protection level > 2.4 kV typical (Note 3)
- RoHS Compliant
- Free from halogenated compounds and antimony oxides



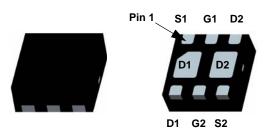
#### **General Description**

This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultraportable applications. It features two independent P-Channel MOSFETs with low on-state resistance for minimum conduction losses. When connected in the typical common source configuration, bi-directional current flow is possible.

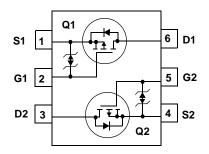
The MicroFET 2X2 Thin package offers exceptional thermal performance for it's physical size and is well suited to linear mode applications.

#### **Applications**

- Battery protection
- Battery management
- Load switch



MicroFET 2x2



## MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parar		Ratings	Units	
$V_{DS}$	Drain to Source Voltage			-20	V
$V_{GS}$	Gate to Source Voltage			±8	V
I <sub>D</sub>	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	-3.6	^
	-Pulsed			-15	Α
Б	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	1.4	١٨/
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1b)	0.7	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Tempe	rature Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance for Single Operation, Junction to Ambient	(Note 1a)	86	
$R_{\theta JA}$	Thermal Resistance for Single Operation, Junction to Ambient	(Note 1b)	173	°C/W
$R_{\theta JA}$	Thermal Resistance for Dual Operation, Junction to Ambient	(Note 1c)	69	C/VV
$R_{\theta JA}$	Thermal Resistance for Dual Operation, Junction to Ambient	(Note 1d)	151	

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
623	FDMA6023PZT	MicroFET 2X2 Thin	7 "	8mm	3000 units

## **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = -250 μA, referenced to 25 °C		-12		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V			-1	μΑ
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$			±10	μΑ

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-0.4	-0.5	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A, referenced to 25 °C		-2.7		mV/°C
		$V_{GS} = -4.5 \text{ V}, I_D = -3.6 \text{ A}$		40	60	
		$V_{GS} = -2.5 \text{ V}, I_D = -3.0 \text{ A}$		49	80	mΩ
	Drain to Source On Resistance	$V_{GS} = -1.8 \text{ V}, I_D = -2.0 \text{ A}$		60	110	
r <sub>DS(on)</sub>		$V_{GS} = -1.5 \text{ V}, I_D = -1.0 \text{ A}$		70	170	11122
		$V_{GS} = -4.5 \text{ V}, I_D = -3.6 \text{ A},$ $T_J = 125 ^{\circ}\text{C}$		58	72	
9 <sub>FS</sub>	Forward Transconductance	$V_{DD} = -5 \text{ V}, \ I_{D} = -3.6 \text{ A}$		15		S

## **Dynamic Characteristics**

(	C <sub>iss</sub>	Input Capacitance	V 40 V V 0 V	665	885	pF
(	C <sub>oss</sub>	Output Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz	115	155	pF
(	C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1911 12	100	150	pF

## **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		13	23	ns
t <sub>r</sub>	Rise Time	$V_{DD} = -10 \text{ V}, I_{D} = -3.6 \text{ A},$	11	20	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$	75	120	ns
t <sub>f</sub>	Fall Time		47	75	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ V to } -4.5 \text{ V}$ $V_{DD} = -10 \text{ V},$	12	17	nC
Q <sub>gs</sub>	Gate to Source Charge	$V_{DD} = -10 \text{ V},$ $I_{D} = -3.6 \text{ A}$	1.4		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	ID = -0.0 A	5.2		nC

## **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				-1.1	Α
$V_{SD}$	Source to Drain Diode Forward Voltage V <sub>GS</sub> = 0 V, I <sub>S</sub> = -1.1 A (Note 2)			-0.7	-1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = -3.6 A, di/dt = 100 A/μs		33	53	ns
Q <sub>rr</sub>	Reverse Recovery Charge	T <sub>F</sub> = -3.6 A, α//αι = 100 A/μs		15	27	nC

## Electrical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

#### Notes

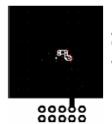
- 1.  $R_{\theta,JA}$  is determined with the device mounted on a 1 in<sup>2</sup> oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta,JC}$  is guaranteed by design while  $R_{\theta,JA}$  is determined by the user's board design.
  - (a)  $R_{\theta JA}$ = 86 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For single operation.
  - (b)  $R_{\theta JA}$  = 173 °C/W when mounted on a minimum pad of 2 oz copper. For single operation.
  - (c)  $R_{\theta JA} = 69 \,^{\circ}\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For dual operation.
  - (d)  $R_{\theta JA}$  = 151 °C/W when mounted on a minimum pad of 2 oz copper. For dual operation.



a) 86°C/W when mounted on a 1in² pad of 2 oz copper.



b)173°C/W when mounted on a minimum pad of 2 oz copper.



c) 69°C/W when mounted on a 1in² pad of 2 oz copper.



d)151°C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0%.
- 3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

## Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

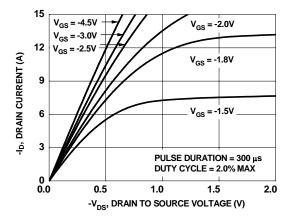


Figure 1. On-Region Characteristics

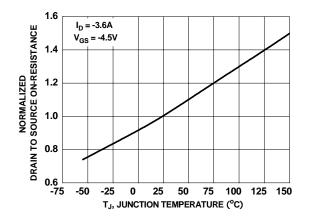


Figure 3. Normalized On-Resistance vs Junction Temperature

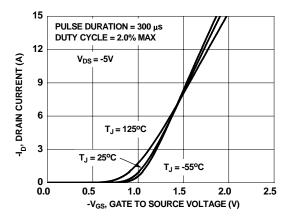


Figure 5. Transfer Characteristics

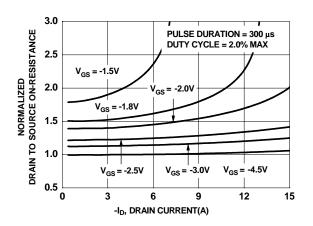


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

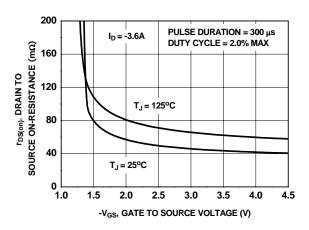


Figure 4. On-Resistance vs Gate to Source Voltage

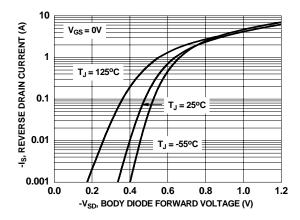


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

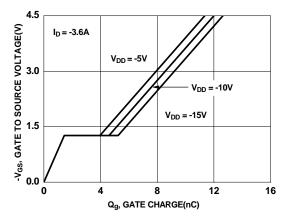


Figure 7. Gate Charge Characteristics

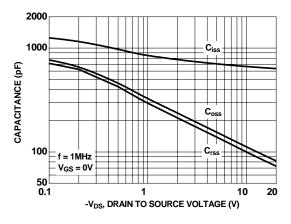


Figure 8. Capacitance vs Drain to Source Voltage

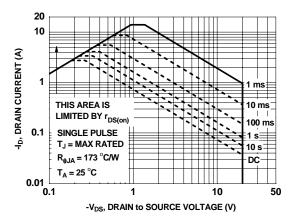


Figure 9. Forward Bias Safe Operation Area

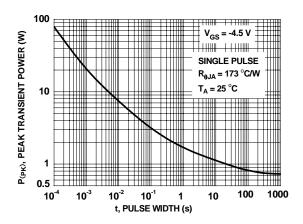


Figure 10. Single Pulse Maximum Power Dissipation

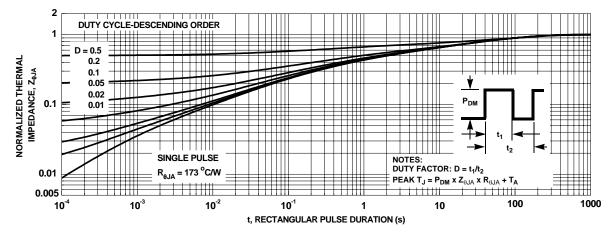
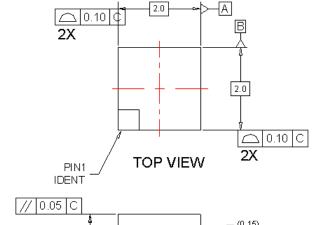
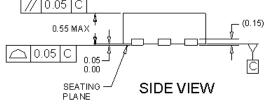
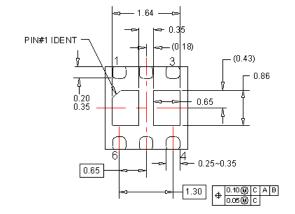


Figure 11. Junction-to-Ambient Transient Thermal Response Curve

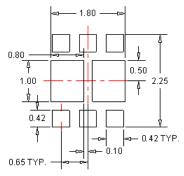
## **Dimensional Outline and Pad Layout**







**BOTTOM VIEW** 



RECOMMENDED LAND PATTERN

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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
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