N-channel 40 V, 1.0 mΩ standard level MOSFET in LFPAK88
26 April 2019 Product data sheet

# 1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a copper-clip LFPAK88 package. This product has been fully designed and qualified to meet beyond AEC-Q101 requirements delivering high performance and reliability.

## 2. Features and benefits

- · Fully automotive qualified to beyond AEC-Q101:
  - -55 °C to +175 °C rating suitable for thermally demanding environments
- LFPAK88 package
  - Designed for smaller footprint and improved power density over older wire bond packages such as D<sup>2</sup>PAK for today's space constrained high power automotive applications
  - Thin package and copper clip enables LFPAK88 to be highly efficient thermally
- LFPAK copper clip technology enabling improvements over wire bond packages by:
  - Increased maximum current capability and excellent current spreading
  - Improved R<sub>DSon</sub>
  - · Low source inductance
  - Low thermal resistance R<sub>th</sub>
- LFPAK Gull Wing leads:
  - Flexible leads enabling high Board Level Reliability absorbing mechanical and thermal cycling stress, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joint
- Unique 40 V Trench 9 superjunction technology:
  - Reduced cell pitch and superjunction platform enables lower R<sub>DSon</sub> in the same footprint
  - Improved SOA and avalanche capability compared to standard TrenchMOS
  - Tight V<sub>GS(th)</sub> limits enable easy paralleling of MOSFETs

# 3. Applications

- 12 V automotive systems
- 48 V DC/DC systems (on 12 V secondary side)
- Higher power motors, lamps and solenoid control
- Reverse polarity protection
- LED lighting
- · Ultra high performance power switching

## 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	-	40	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	[1]	-	-	325	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	-	375	W



Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Static chara	acteristics						
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS}$ = 10 V; $I_{D}$ = 25 A; $T_{j}$ = 25 °C; Fig. 11		0.62	0.88	1	mΩ
Dynamic ch	naracteristics		•				'
$Q_{GD}$	gate-drain charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V; Fig. 13; Fig. 14		-	17	34	nC
Source-dra	in diode					<b> </b>	1
Q <sub>r</sub>	recovered charge	$I_S$ = 25 A; $dI_S/dt$ = -100 A/ $\mu$ s; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V	[2]	-	49	-	nC
S	softness factor	$I_S$ = 25 A; $dI_S/dt$ = -100 A/ $\mu$ s; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; $T_j$ = 25 °C		-	0.8	-	

<sup>[1] 325</sup>A continuous current has been successfully demonstrated during application. practically the current will be limited by PCB, thermal design and operating temperature.

# 5. Pinning information

**Table 2. Pinning information** 

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		D
2	S	source		
3	S	source		G (F)
4	S	source		mbb076 S
mb	D	mounting base; connected to drain	LFPAK88 (SOT1235)	

# 6. Ordering information

**Table 3. Ordering information** 

Type number	Package					
	Name	Description	Version			
BUK7S1R0-40H	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235			

# 7. Marking

### Table 4. Marking codes

Type number	Marking code
BUK7S1R0-40H	7S1R040H

# 8. Limiting values

## Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	40	V

<sup>[2]</sup> includes capacitive recovery

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>GS</sub>	gate-source voltage	DC; T <sub>j</sub> ≤ 175 °C		-10	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	375	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	[1]	-	325	Α
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$ ; Fig. 3		-	1659	Α
T <sub>stg</sub>	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drain	n diode		'	·	•	'
Is	source current	T <sub>mb</sub> = 25 °C	[2]	-	350	Α
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	1659	Α
Avalanche r	uggedness				•	<u>'</u>
E <sub>DS(AL)S</sub>	non-repetitive drain- source avalanche energy	$I_D$ = 120 A; $V_{sup} \le 40$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[3] [4]	-	437	mJ

- [1] 325A continuous current has been successfully demonstrated during application. practically the current will be limited by PCB, thermal design and operating temperature.
- [2] 350A continuous current has been successfully demonstrated during application. practically the current will be limited by PCB, thermal design and operating temperature.
- [3] single pulse avalanche rating limited by maximum junction temperature of 175°C
- [4] refer to application note AN10273 for further information

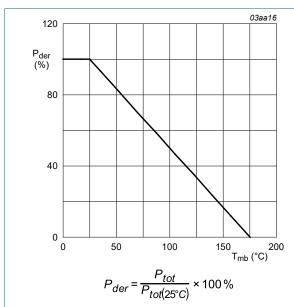
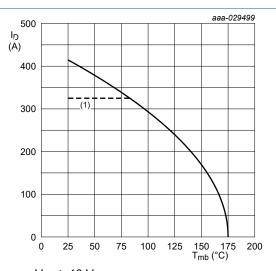


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

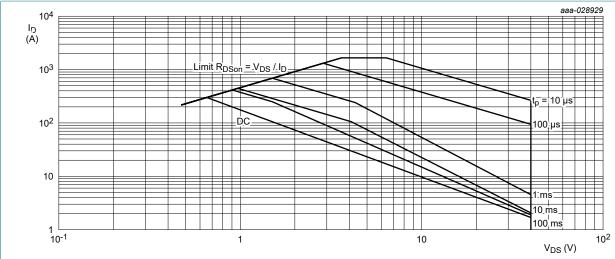


 $V_{GS} \ge 10 \text{ V}$  (1) 325A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature

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 $T_{mb}$  = 25 °C;  $I_{DM}$  is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

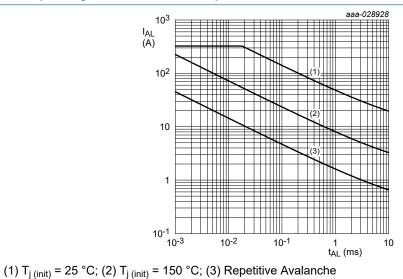
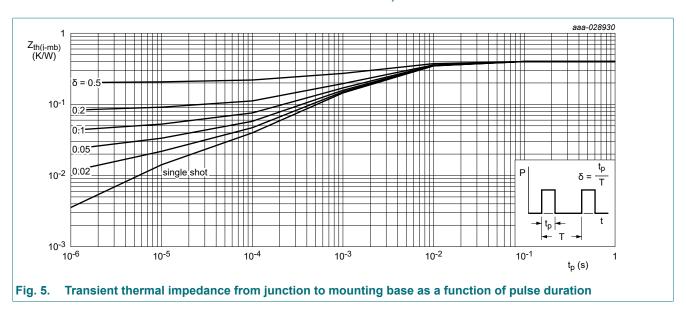


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

## 9. Thermal characteristics

### **Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 5	-	0.35	0.4	K/W



# 10. Characteristics

**Table 7. Characteristics** 

Static characteristics $V_{(BR)DSS} \  \   \begin{array}{l} \text{drain-source} \\ \text{breakdown voltage} \end{array} \  \   \begin{array}{l} I_D = 250 \ \mu\text{A; } V_{GS} = 0 \ \text{V; } T_j = 25 \ ^{\circ}\text{C} \\ I_D = 250 \ \mu\text{A; } V_{GS} = 0 \ \text{V; } T_j = -40 \ ^{\circ}\text{C} \\ \end{array}$	40 - 36	43	-	
breakdown voltage $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 ^{\circ} C$	-		_	
breakdown voltage $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 ^{\circ} C$		40.5		V
L 050 A V 0 V = 00	26	<del>-</del> 0.5	-	V
$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 ^{\circ} C$	30	40	-	V
$V_{GS(th)}$ gate-source threshold $I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = 25$ °C; Fig. 9; voltage	2.4	3	3.6	V
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 10	1	-	-	V
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}; Fig. 10$	-	-	4.3	V
drain leakage current $V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	0.2	1.5	μΑ
$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 ^{\circ}\text{C}$	-	4.7	25	μΑ
$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 ^{\circ}\text{C}$	-	287	1000	μΑ
$V_{GSS}$ gate leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
$R_{DSon}$ drain-source on-state $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ resistance Fig. 11	0.62	0.88	1	mΩ
$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 105 ^{\circ}\text{C};$ Fig. 12	0.87	1.3	1.6	mΩ
$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 125 ^{\circ}\text{C};$ Fig. 12	0.97	1.4	1.75	mΩ
$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 ^{\circ}\text{C};$ Fig. 12	1.2	1.8	2.2	mΩ
$R_G$ gate resistance $f = 1 \text{ MHz}; T_j = 25 \text{ °C}$	0.4	0.9	2.3	Ω
Dynamic characteristics	'			•
$Q_{G(tot)}$ total gate charge $I_D = 25 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V};$	-	98	137	nC
Q <sub>GS</sub> gate-source charge Fig. 13; Fig. 14	-	27	40	nC
Q <sub>GD</sub> gate-drain charge	-	17	34	nC

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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz;		-	7373	10322	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 15</u>		-	1578	2209	pF
C <sub>rss</sub>	reverse transfer capacitance			-	295	649	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 10 \text{ V};$		-	23	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5 \Omega$		-	19	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	59	-	ns
t <sub>f</sub>	fall time			-	26	-	ns
Source-dra	in diode	,					
V <sub>SD</sub>	source-drain voltage	V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <u>Fig. 16</u>		-	0.76	1	V
t <sub>rr</sub>	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$		-	43	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 20 V	[1]	-	49	-	nC
S softness factor	softness factor	$I_S$ = 25 A; $dI_S/dt$ = -100 A/ $\mu$ s; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; $T_j$ = 25 °C		-	0.8	-	
		$I_S$ = 25 A; $dI_S/dt$ = -500 A/ $\mu$ s; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; $T_j$ = 25 °C		-	0.7	-	

### [1] includes capacitive recovery

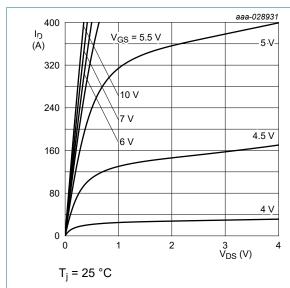


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

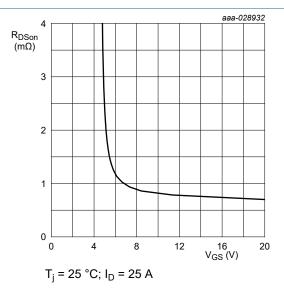


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

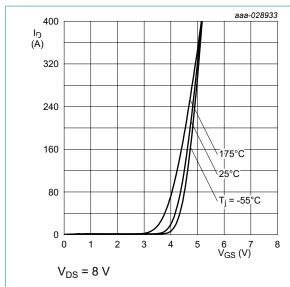


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

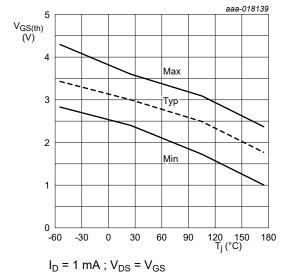


Fig. 10. Gate-source threshold voltage as a function of junction temperature

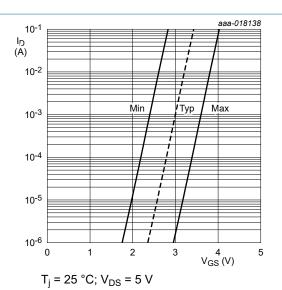


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

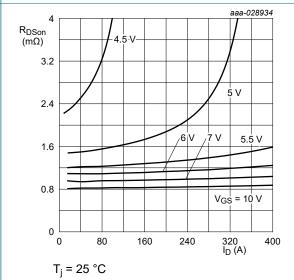


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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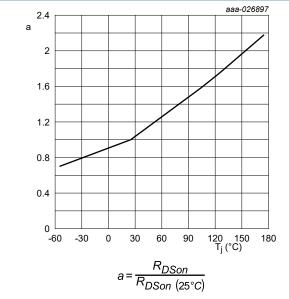


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

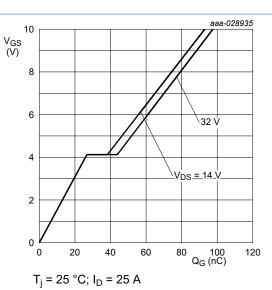


Fig. 13. Gate-source voltage as a function of gate charge; typical values

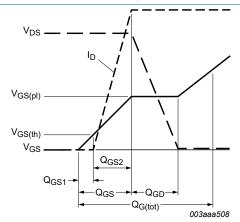


Fig. 14. Gate charge waveform definitions

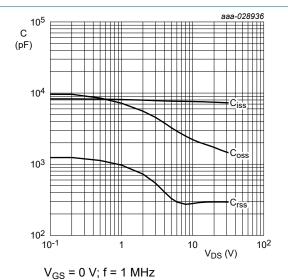


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical

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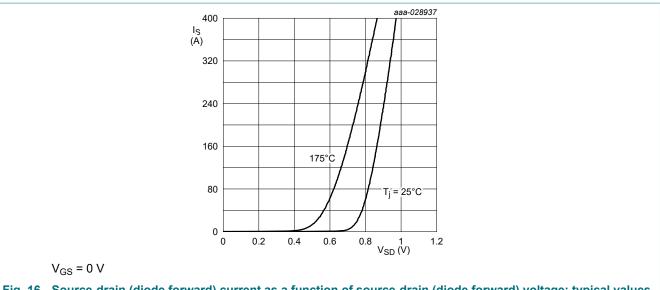


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

# 11. Package outline

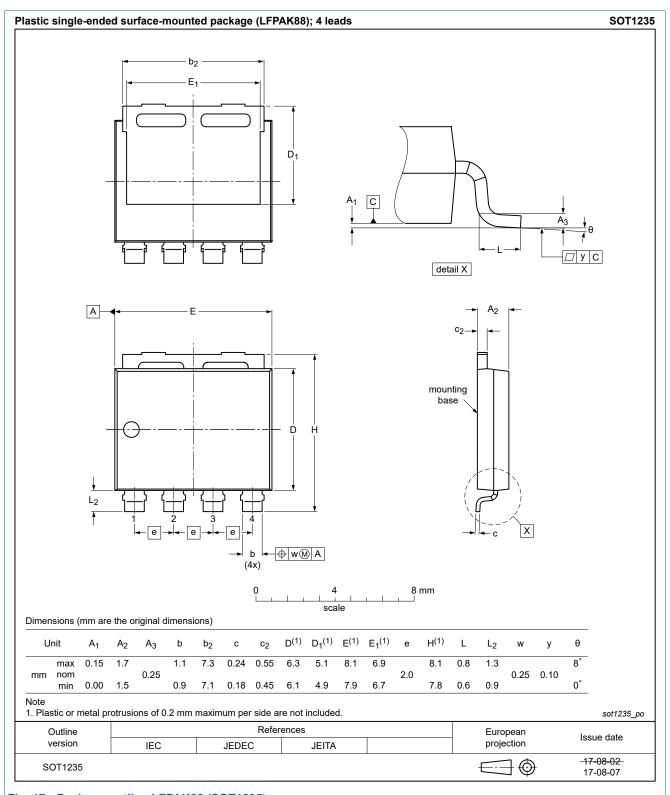
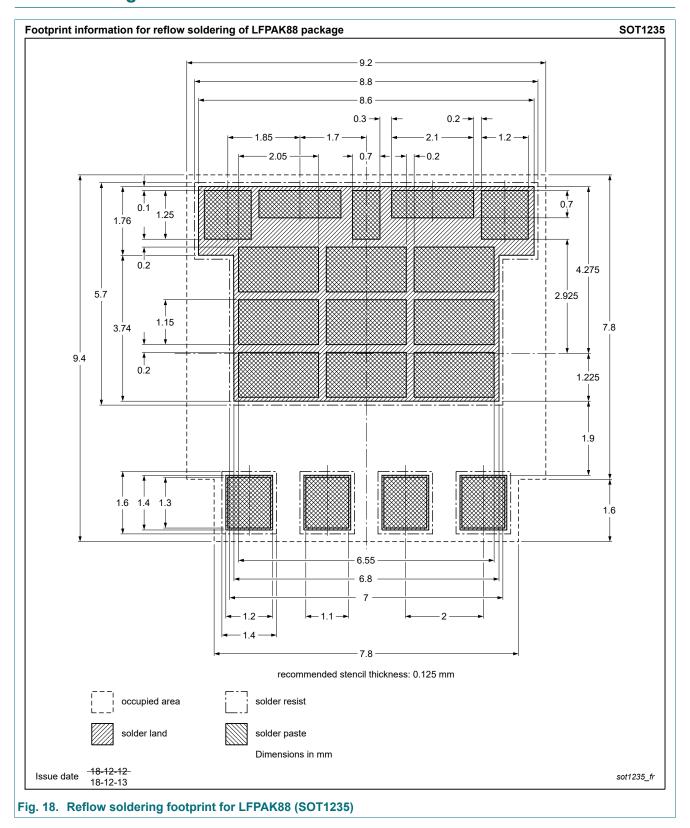


Fig. 17. Package outline LFPAK88 (SOT1235)

# 12. Soldering



# 13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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For more information, please visit: http://www.nexperia.com For sales office addresses, please send an email to: salesaddresses@nexperia.com Date of release: 26 April 2019

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многоканальный

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